FPGA-TDC and its applications

Amplifier, Digitizer and Readout of PMTs, MA-PMTs, MCP-PMTs, SiPMs and LGADs based on FPGA-TDCs

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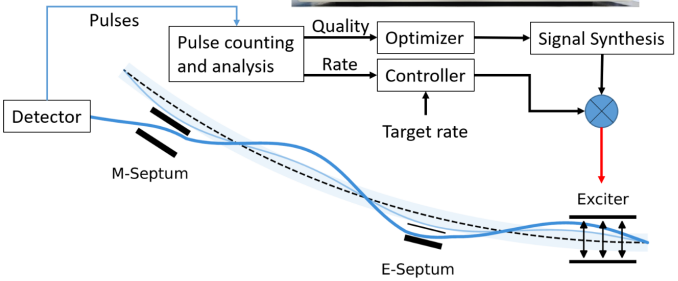
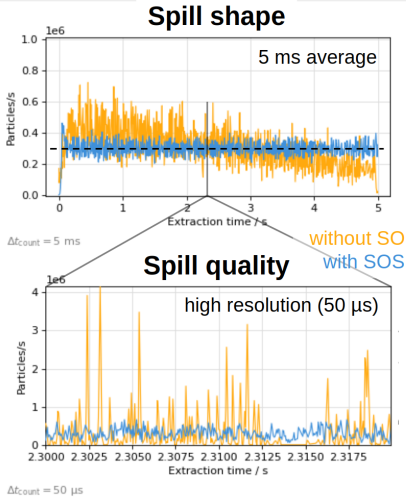
Outline

Presentation agenda

How it works: implemented in GNU Radio (CPU) and in FPGA

- Feedback improves spill shape
- New signals improve spill quality

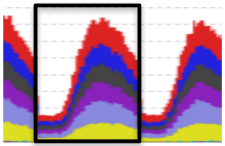




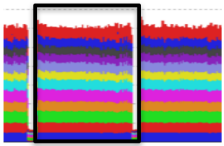
Result for HADES I

- SOS Feedback improves macro spill shape
- HADES reported
  - → Immediately 40% more statistics due to DC beam (geometric factor)
  - → Up to factor 2 due to absence of cycle-to-cycle fluctuations

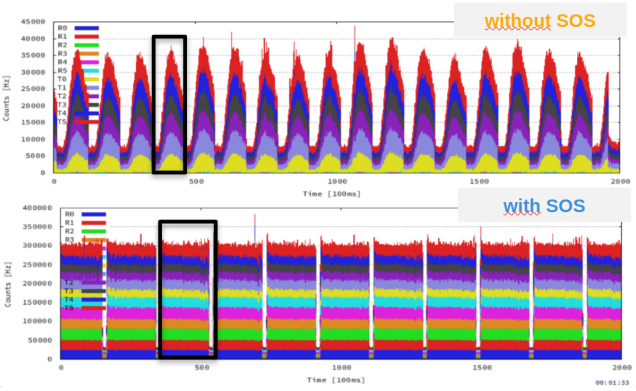
without SOS



with SOS

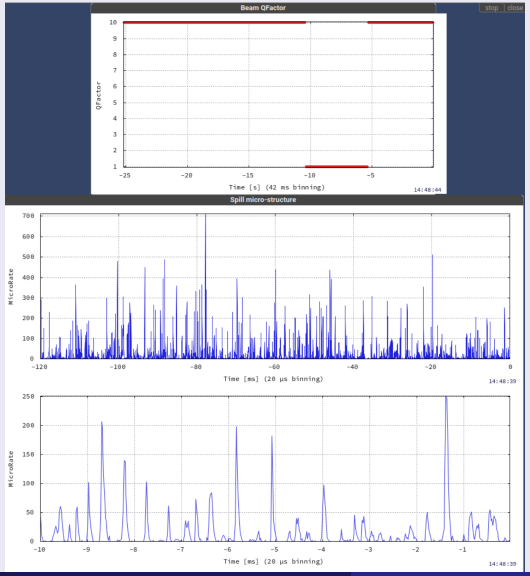


HADES Data Rate

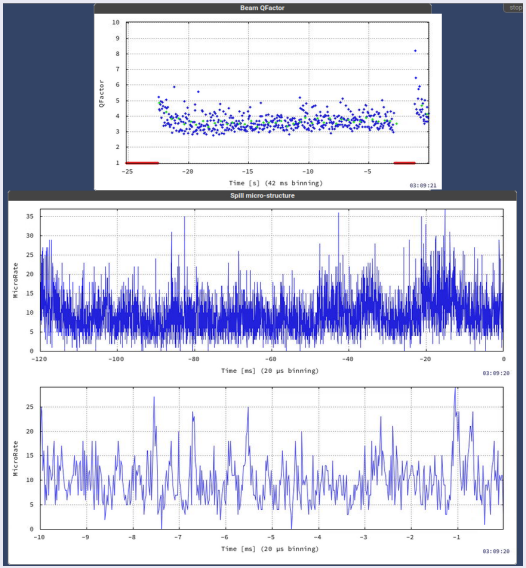


Spill Optimization System (SOS), micro-Spill results

Bad micro-spill-quality



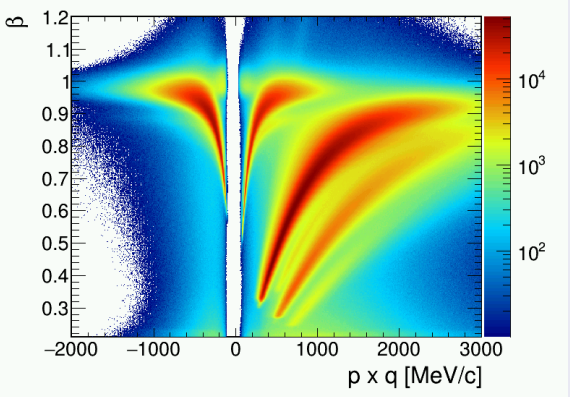
Very good micro-spill-quality



Presentation agenda

Time Measurements in Particle Physics: Why?

Time of Flight (ToF) applications for particle identification



"Live" plot of a HADES measurement campaign @GSI.

Other "trivial" applications of time measurements

- Arrivial time to separate events (free running data acquisition)
- Pile-up (>1 reaction in integration time of detectors) rejection

Time measurements are used in every experiment!

Time Measurements: How?

How to obtain the time measurement

- Oscilloscope (ADC) gives the best representation of the original signal and best possiblilties for offline processing and correction
- ADCs for precise time measurement draw "a lot" of power, are expensive and additional massive data processing necessary → heat, price, space
  - possible to use efficiently if time interval is short (selective trigger)

Typical photomultiplier signals on oscilloscope

Time Measurements with TDC

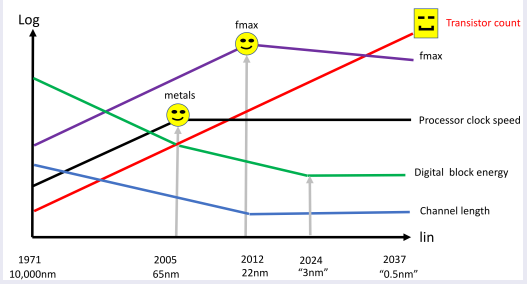
- If the number of channels increase and a very good time precision is needed
  - Signal discrimination (threshold) and time difference measurement is a feasible and effective option
- Amplitude measurement: direct Time over Threshold (ToT)
  - not linear and limited dynamic range
- Time measurement can also be used for precise charge measurement!
  - example will come...

Consequence

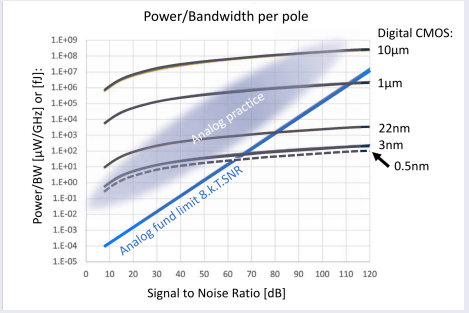
- Use time measurement for all detectors in the system
- A very flexible, precise, low power, small and cheap Time to Digital (TDC) converter is needed

Backing from Electronics Research

Asymptotic Moore's law



Power analog vs. digital

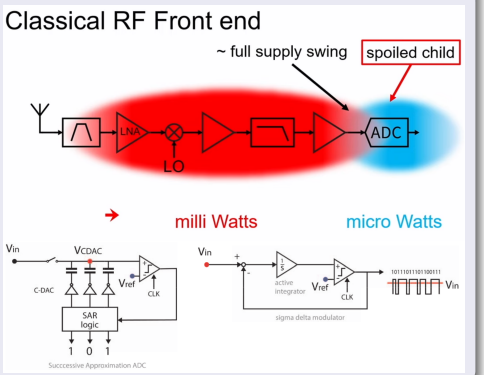


New ideas to improve efficiency

- very recent talk from Bram Nauta (University of Twente)
- "Racing down the slopes of Moore's law", Keynote speech, IEEE International Solid-State Circuits Conference, ISSCC 2024
- DOI: 10.1109/ISSCC49657.2024.10454417

Backing from Electronics Research II

SAR-ADCs and sigma-delta ADCs



"We see that the dissipation of the ADC (microwatts) is several orders-of-magnitude smaller than that of the milliwatts of the receiver circuits preceding the ADC."

Conclusion

"We should wonder why we are designing power-hungry front-ends with active linear gain at all to finally drive an ultra-low power comparator in an ADC. Maybe we should consider directly driving a comparator in an ADC from the small input signal of the chain."

Presentation agenda

Motivation for this type of electronics / Why this effort?

- Quite common task in particle physics / medical applications: precise (≈10ps - 100ps RMS) time measurement for
  - Photon detection:
    - PMTs, MA-PMTs, MCP-PMTs, SiPMs
  - particle detection
    - LGAD ("new")
- Flexible electronics for many types of sensors
  - no community ASIC
    - to be able to change very fast to the special demands
    - should be easily available from a commercial vendor
- overall goal: System price. Not the best possible performance.
  - cheap and off the shelf components
    - FPGA-TDCs for digitization ("small" frontend FPGAs)
    - amplifiers (cell phones)

Further motivation for building TDCs with an FPGA

- flexibility, all-in-one chip (discriminator, TDC, DAQ), FPGA needed anyhow
- channel price "automatically" drops with new FPGA generations
  - factor of 5 in performance/price increase in 5 years
  - game-changer: FPGA/TDC/DAC/Discriminator are not the price determining part of the system anymore!
  - enables the use of FPGAs "everywhere" in the front-end
- new processes (in consumer electronics) improves radiation tolerance by a factor of ∼100 (e.g. FD-SOI - STMicroelectronics)

Radiation		Experimental radiation test data	FDSOI28 SER gain w.r.t. BULK 28nm
Atmospheric neutrons (<800MeV)	Sea-level	Neutron-SER < 10FIT/Mb	100×
Alpha particles (@0.001cph/cm2)	Sea-level	Alpha-SER < 1 FIT/Mb	1000×
	Sea-level	RHBD microprocessor immunity	100×
	Sea-level	Ultra low alpha wafer counting	~
Thermal neutron (<25meV)	Sea-level	Thermal-SER < 2 FIT/Mb	20×
Muons	Sea-level	Peak error rate 10x lower than Bulk	>10×
Heavy ions (≤60MeV/(mg/cm²))	space	Asymptotic error X-section=10^{-10} cm²/bit	100×
Low energy protons (<10MeV)	space	Error cross-section < 10^{-14} cm²/bit	1000×
Gamma rays (10KeV)	space	VTH shift <1mV/krad (till 100krad)	~

Presentation agenda

How can an FPGA be used as an TDC?

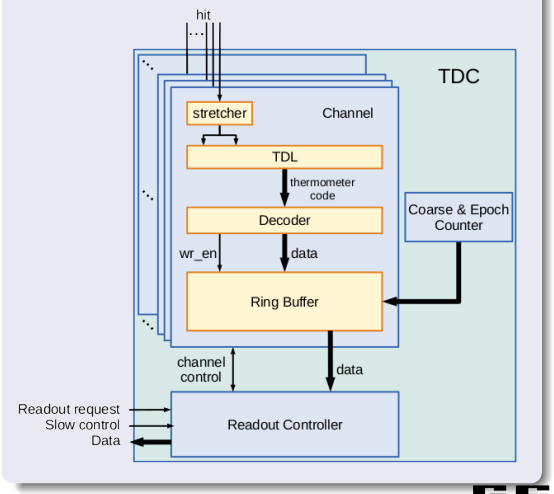
- We "misuse" digital FPGAs in the asynchronous and analogue domain
  - an FPGA is more than a digital device $\rightarrow$ go deep in FPGA architecture
  - use intrinsic delays for time measurements, pulse stretching and signal delays
  - use LVDS-input buffers for signal discrimination

Basic Operation of an FPGA-TDC

Features

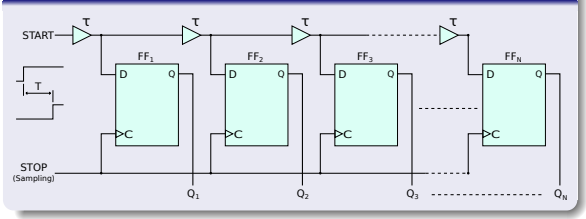
- Coarse & Epoch counters for long measurement range
- Tapped Delay Line for fine time interpolator
- Stretcher for measuring the trailing edge in the same channel
- Decoder: thermocode $\rightarrow$ binary
- Ring buffer for the latest hit signals

TDC-architecture

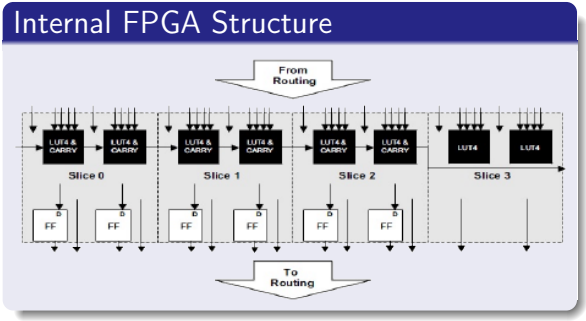


Fine Time Interpolation

Tapped Delay Line

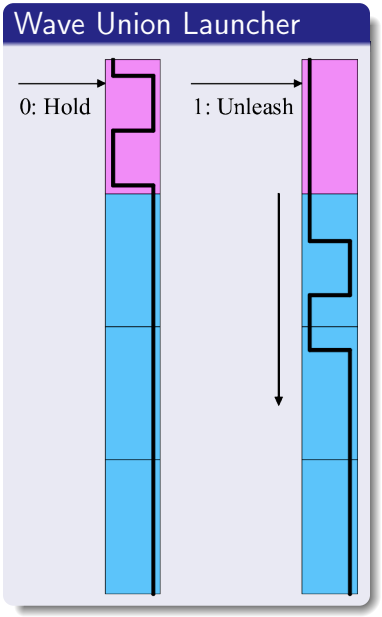


Internal FPGA Structure



- Propagation of the start signal is sampled with the stop signal
- Suits well with the FPGA architecture
- Carry chain for delay line $\rightarrow$ small bin width
- Clock signal as common stop signal $\rightarrow$ minimal skew
- Coarse & Epoch counters $\rightarrow$ $\sim$45 minutes measurement range

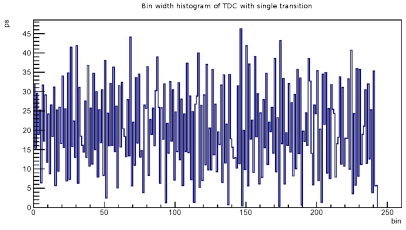
FPGA-TDC: Further improvements

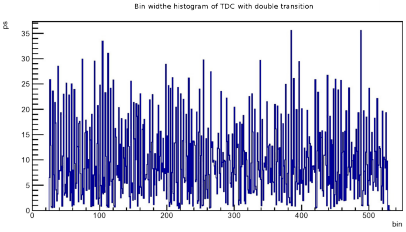


- Non-uniform intrinsic delays → Ultra wide bins
- the precision of the TDC is reduced
- Wave Union Launcher [Jinyuan Wu]:
  - send many transitions to the delay line, when a hit signal arrives, thereby increase the number of measurements on the delay line and even out ultra wide bins (UWB)

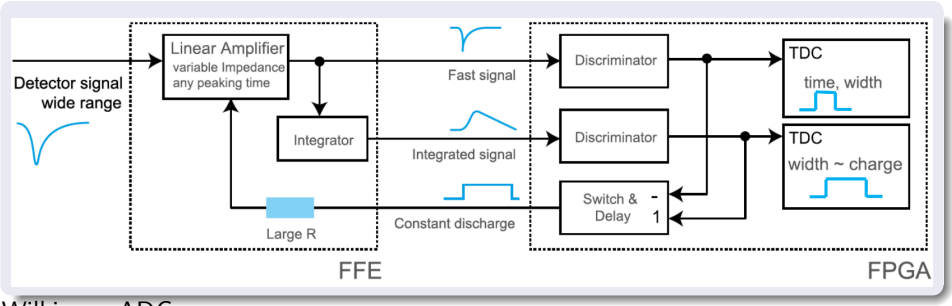
FPGA-TDCs: Bin Width (DNL)

- Non-linearities caused by non-uniform intrinsic delays
- UWBs increase non-linearities
- WUL averages the locations of the transition on the delay line, thus dividing the UWBs
- Max bw: 45ps $\rightarrow$ 35ps
- Avg bw: 20ps $\rightarrow$ 10ps
- Calibration of the TDC further decreases the non-linearity





FPGA-TDC: Charge Measurement

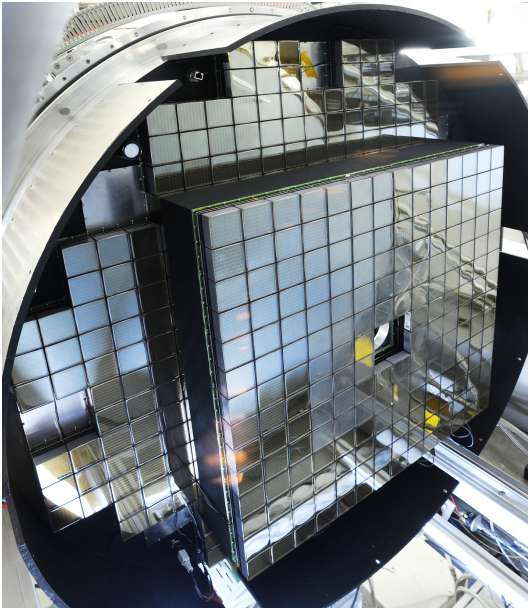


Modified Wilkinson ADC:

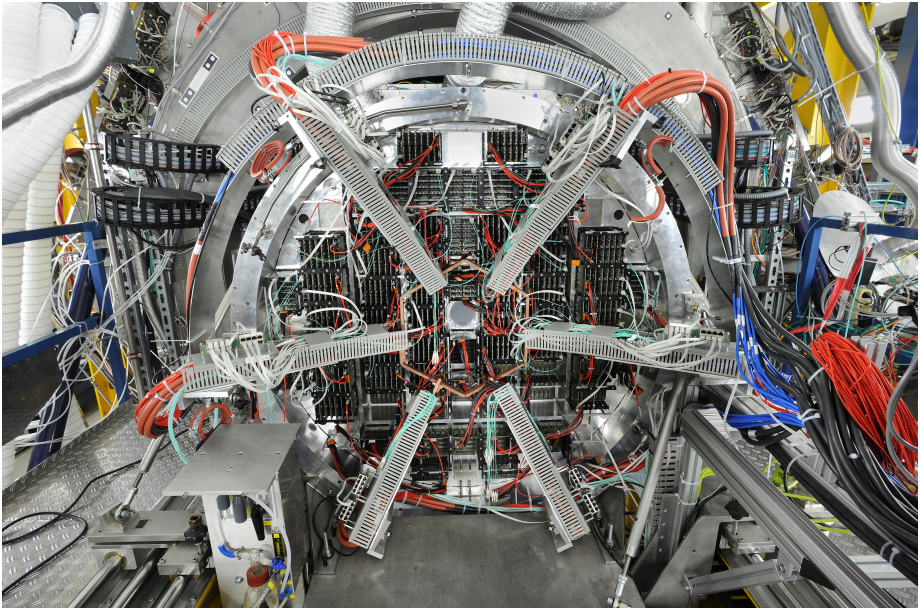
- "Come-and-Kiss"-principe: Commercial of the shelf and keep it small and simple.
- Input signal is integrated with a capacitor
- Capacitor is discharged using a constant current source triggered by the input signal
- first version of system: charge precision: 0.22%
- improved version: Flexible (very high dynamic range)

Presentation agenda

HADES RICH Detector: 428 PMTS, each 64 channels



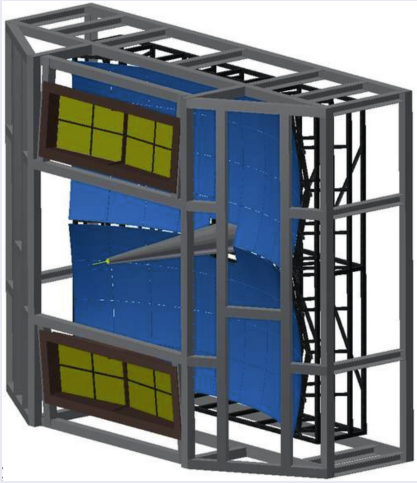
HADES RICH Detector: DiRICH Electronics for 27k channels



Future Applications: CBM RICH + PANDA RICH

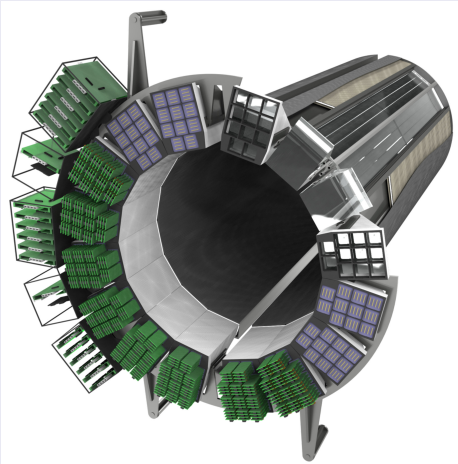
CBM-RICH

- 60k channels are in production now



PANDA Barrel DIRC

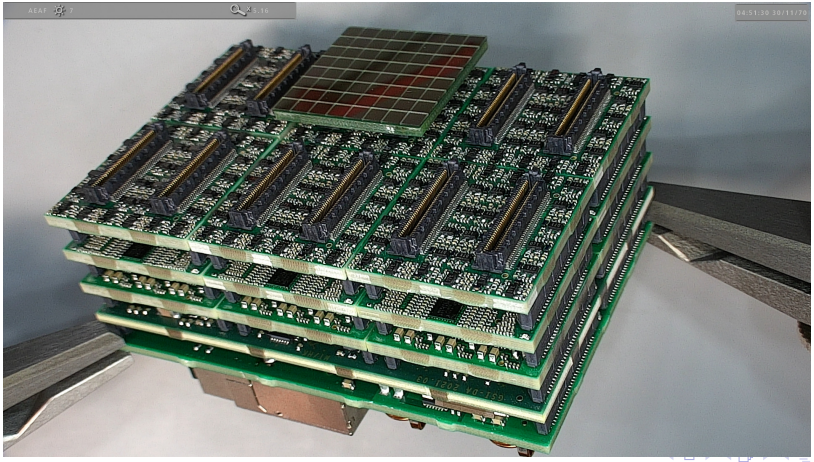
- 17k channels for PANDA



Presentation agenda

Next Step: Getting Smaller => The FaRICH System

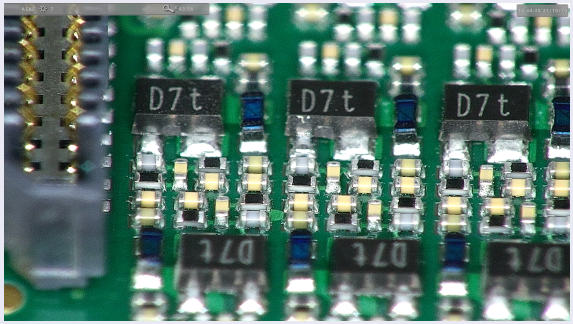
- SiPMs are smaller than PMT based sensors
  - fitting electronics is needed
- 1/10th of the volume compared to the DiRICH-System
- 5.5cm x 8cm: 384 Channels, 10ps RMS TDC, complete DAQ integrated



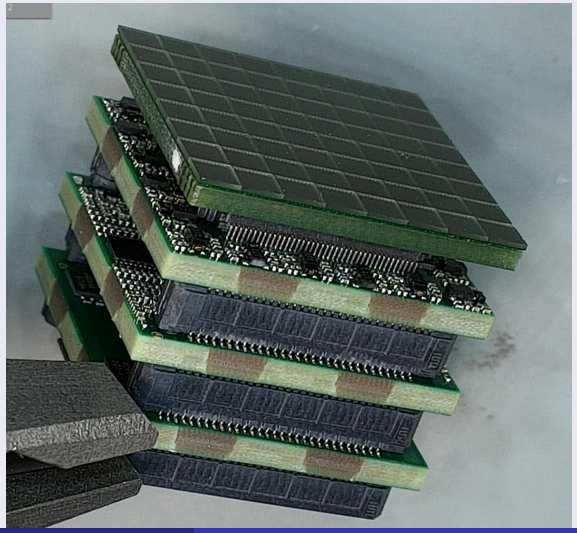
Next Step: Getting Smaller => The FaRICH System

- per sensor only 27mm x 27mm: only possible with

small components, densely populated



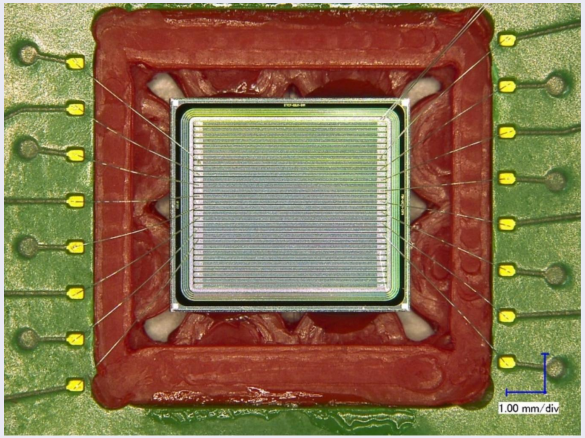
small connectors and laser cutting



One step more: Particle detection with LGAD

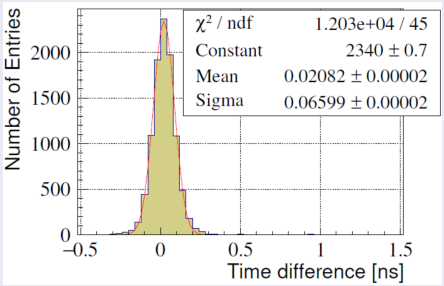
LGAD Sensor

- Low Gain Avalanche Detector
- for example for beam detectors to determine T0: e.g. in HADES



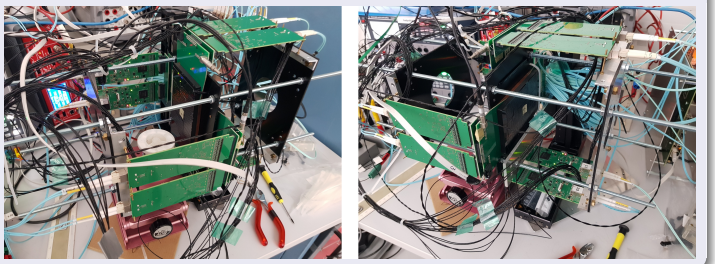
LGAD time measurement

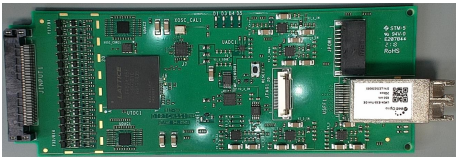
- very good timing performance
- 8000 electrons signal



LGAD readout system: DiRICH5s1: e.g. for 4d Tracking

DiRiCH5s based readout





- useful for small signals, as no cables, but very flexible for positioning, as no backplane
- "First experimental time-of-flight-based proton radiography using low gain avalanche diodes", Felix Ulrich-Pur et al., DOI 10.1088/1361-6560/ad3326

Presentation agenda

lessons learned from existing DAQ systems

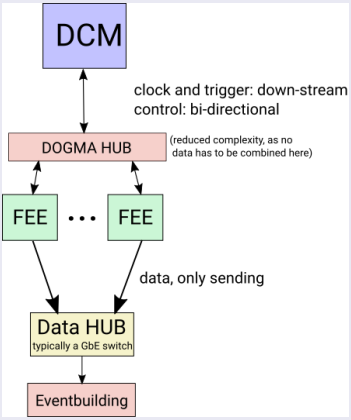
- operating 2500 FPGAs in the acceptance of the detector
  - SEU is an issue
  - reaction to failures
  - large system and 10ps RMS time distribution by copper is an issue
  - only write FPGA gate-ware where absolutely necessary: KISS
    - missing manpower makes this a necessity
- many other DAQ systems are very specialized for a specific application
  - not really usable for other applications

Requirements to new DAQ

- multi-purpose and scalable!
- system recovery of FEE should be done automatically, by design, not added by external software layers
- Eventbuilding can just continue in case of errors
  - breaking former requirements!
- Precise timing can be transmitted via optics
- achievable by a small team!

new DAQ evolution

DAQ overview



DAQ features

- don't reinvent the wheel: use Ethernet as much as possible
  - benefit from all features in it, e.g. back-pressure with pause frames, controls also use Ethernet
  - fully scalable for data transport and controls!
- additional serial link for clock and time-synchronisation and trigger (included trigger-less operation), preferable via optics ($\rightarrow$ galvanic isolation)
  - timing with <10ps RMS precision
  - FEE is automatically integrated/synchronized into DAQ
  - to be vendor independent and safe (very bad experience using SERDES out of vendor specs): Normal I/Os are used!
    - simple and robust in implementation, guaranteed fixed latency, but data-rate very limited (which is not needed).

"DOGMA" implementation: lessons learned

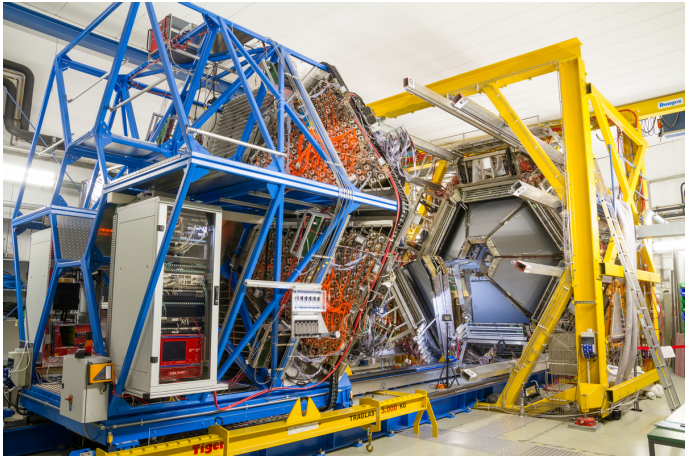
- duty cycle encoding scheme to transfer clock always at the same time for low jitter
- optical links need DC balance
  - 8b10b encoding has running disparity, which will deteriorate the resulting clock
- a 3b8b encoding is now used, which ensures DC-balance at each symbol, while keeping the clock edge always at the same position
  - result: the clock is transmitted with ∼10ps RMS jitter, and with jitter cleaner with ∼6ps RMS
- the rest is work, no research...
- additional features:
  - free steaming is included
  - trigger queues can be implemented
  - triggers can be generated by FEE and propagated to the central trigger system

Presentation agenda

Summary

- The presented FPGA-TDCs (with its associated DAQ) is a mature platform (hardware and software) useful for many applications
  - based on the "come-and-kiss" principle
  - avoid hard to acquire ASICs
  - due to modern commercial components (small, cheap, low-power) now closer to the ASIC domain
- Quite different forms of the hardware have been built. All are "incarnations" of the same concept but each is tailored for different applications, more to come...
- improvements: in the future radiation tolerant FPGAs (FD-SOI) will be used
- evolution of DAQ-system implemented: as simple as possible while still fulfilling the requirements of large and small DAQ-systems

Summary II



- The HADES detector uses only TDCs for analog to digital conversion, including the Electromagnetic Calorimeter.

Summary

- Thank you for your attention!

empty on purpose. . .

Backup