Versatile FPGA-based DAQ system using synchronous Aurora links and AXI infrastructure

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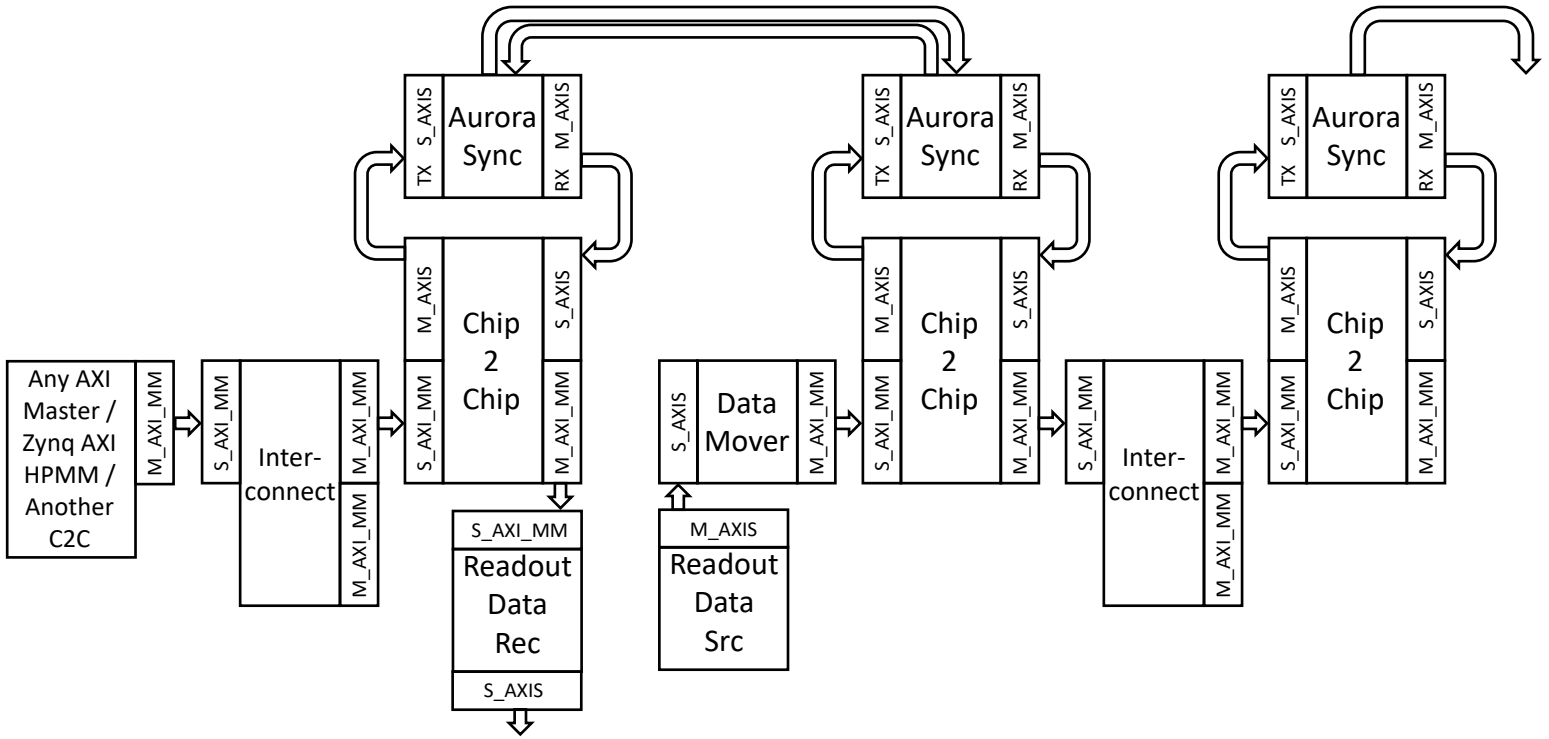
The key concepts

- Primary application – PET imaging
- Scalable, hierarchical architecture
  - Small/medium scale
  - Master, Concentrators, Endpoints model
- Continuous/triggerless readout
  - Triggering readout at fixed rate
- Single link communication
  - Synchronization, data transport, control and monitoring
- Easy to reuse and to expand firmware
  - Standardized protocols and interfaces

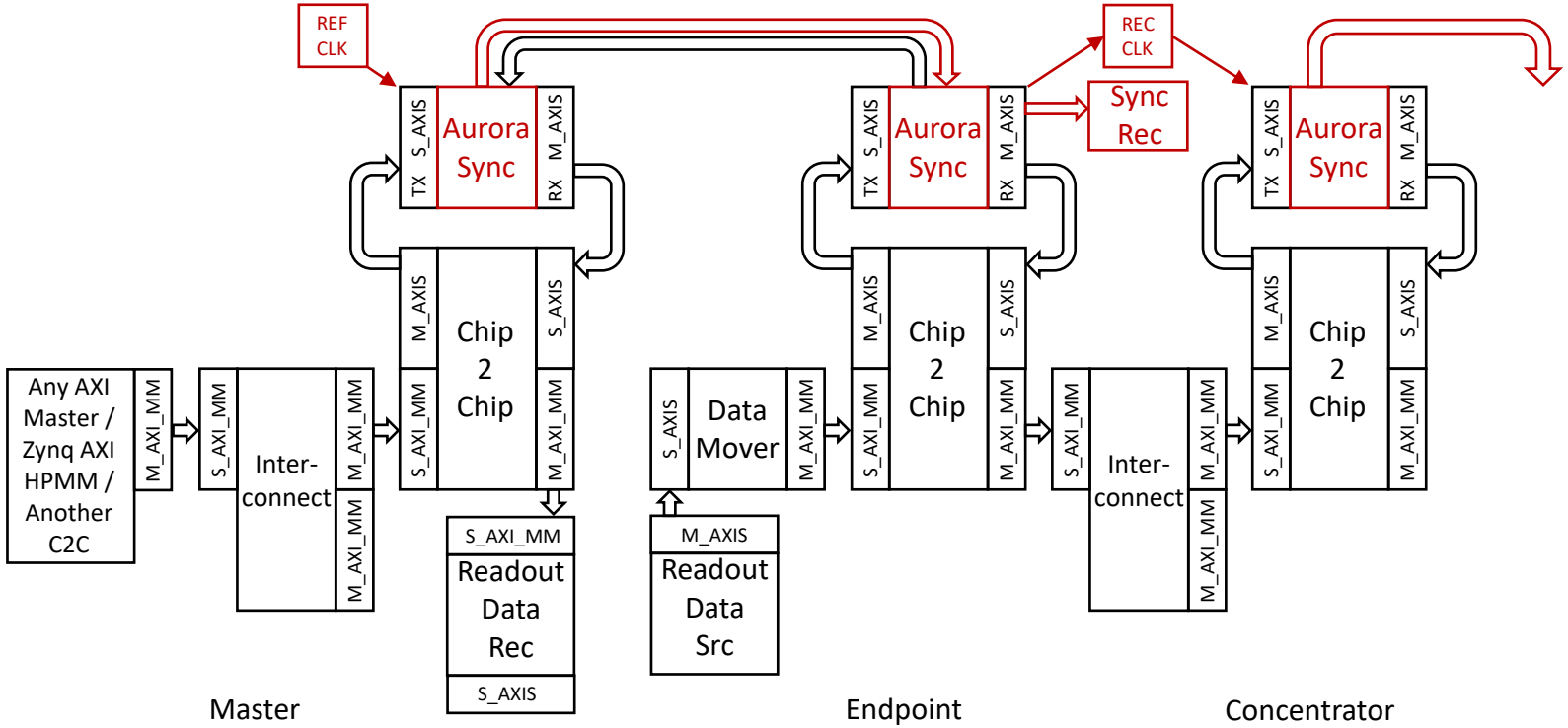
System interconnections

- AXI Master – Slave model at the core
  - In-chip logic components connectivity
  - Device-device communication
  - Addressing scheme
- AXI Stream natural for Aurora
- Aurora with AXI Chip2Chip as a bridge for device-device comm.
  - Transfer between Memory-Mapped and Stream domains and back
- Quick system setup, efficient prototyping



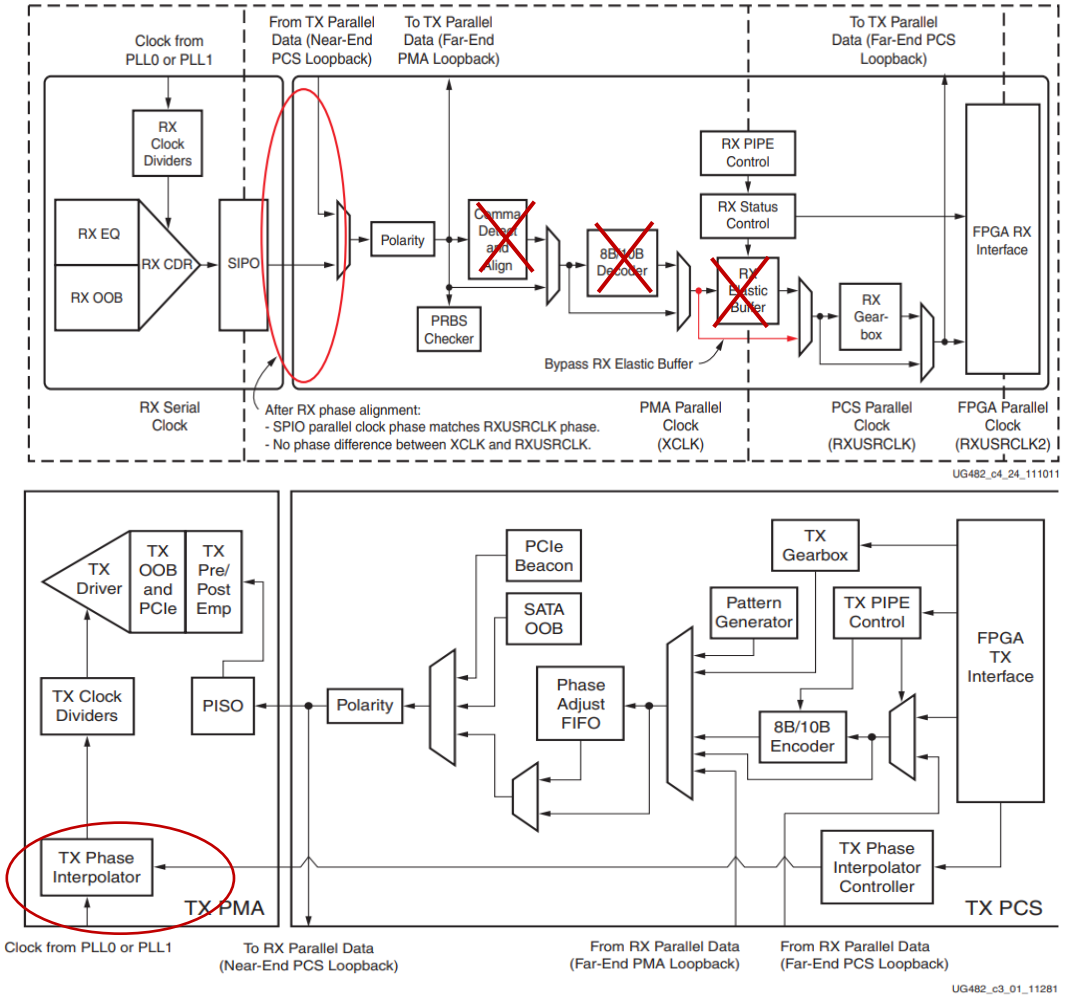
System Architecture

- System Master
  - Source of the common clock
    - Synchronous Aurora Master links in TX channels
- Endpoint
  - Single Aurora Slave interface
  - Recovered clock and synchronization pulse extraction
- Data Concentrator
  - Endpoint
  - A number of Aurora Master links
    - Synchronized to the recovered clock



Aurora Sync

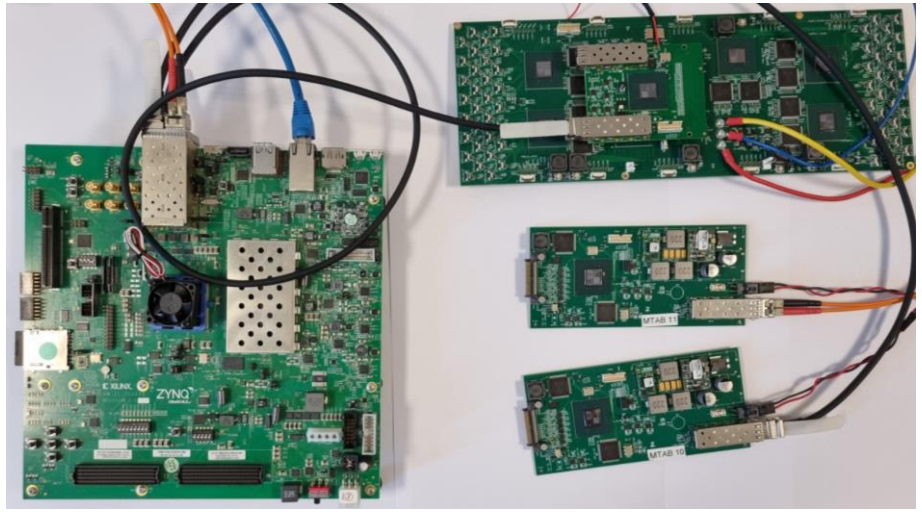
- Aurora 8b/10b as a core component
- Modifications to generic GT:
  - RX on Aurora Slave
    - RX path on RX recovered clock
    - No elastic buffer
    - Custom 8b/10b decoder
    - Custom comma alignment with manual RX slide
  - TX on Aurora Master
    - TX Phase Interpolator for alignment to RX rec. clock
    - PICXO as DPLL to control the TX PI
    - No external jitter cleaners or clock fan-outs
    - No common MGTREF clock between quads
    - Individual, local MGTREF clocks
- Adjustable link speed
- Reference clock distribution
- Unused bit of Aurora stream 32b data word
  - Used for injected serial transmission
  - First bit as a synchronization pulse
  - Following bits decoded as sync words (e.g. readout counter, etc.)
- Implemented and evaluated on GTP, GTX, GTH, GTY at 4 and 5 Gbps

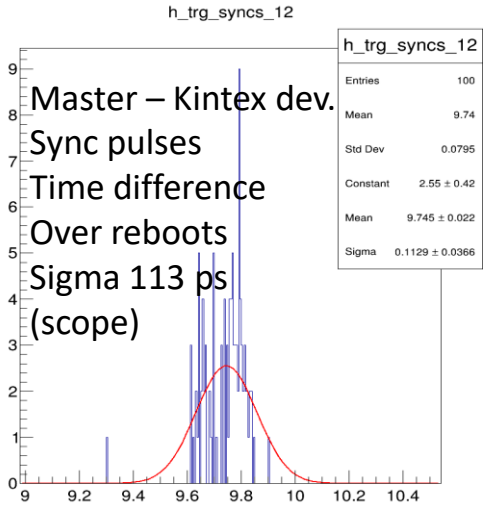


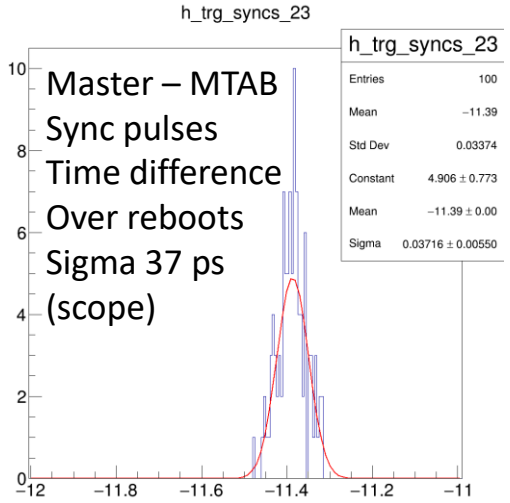
https://docs.amd.com/v/u/en-US/xapp589-VCXO

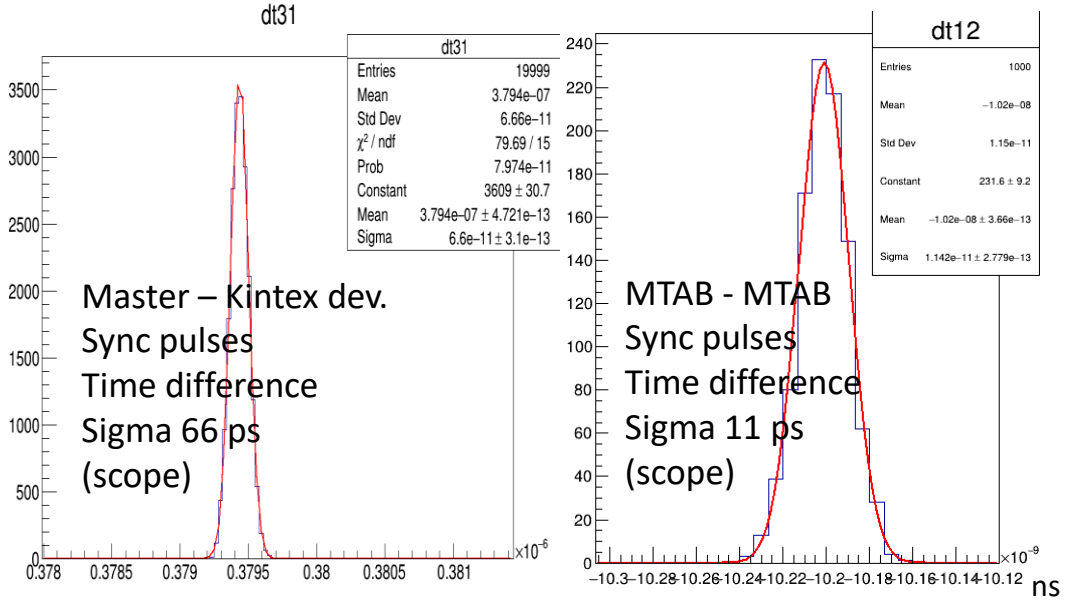
Aurora Sync

- Stable jitter of rec. clock in distributed system
  - Varies between hardware components
  - Jitter increases with number of hops
- Fixed time offsets between Endpoints
  - Repetitive over reboots
  - Fixed for a set of bitfiles
  - Requires single calibration run to compensate





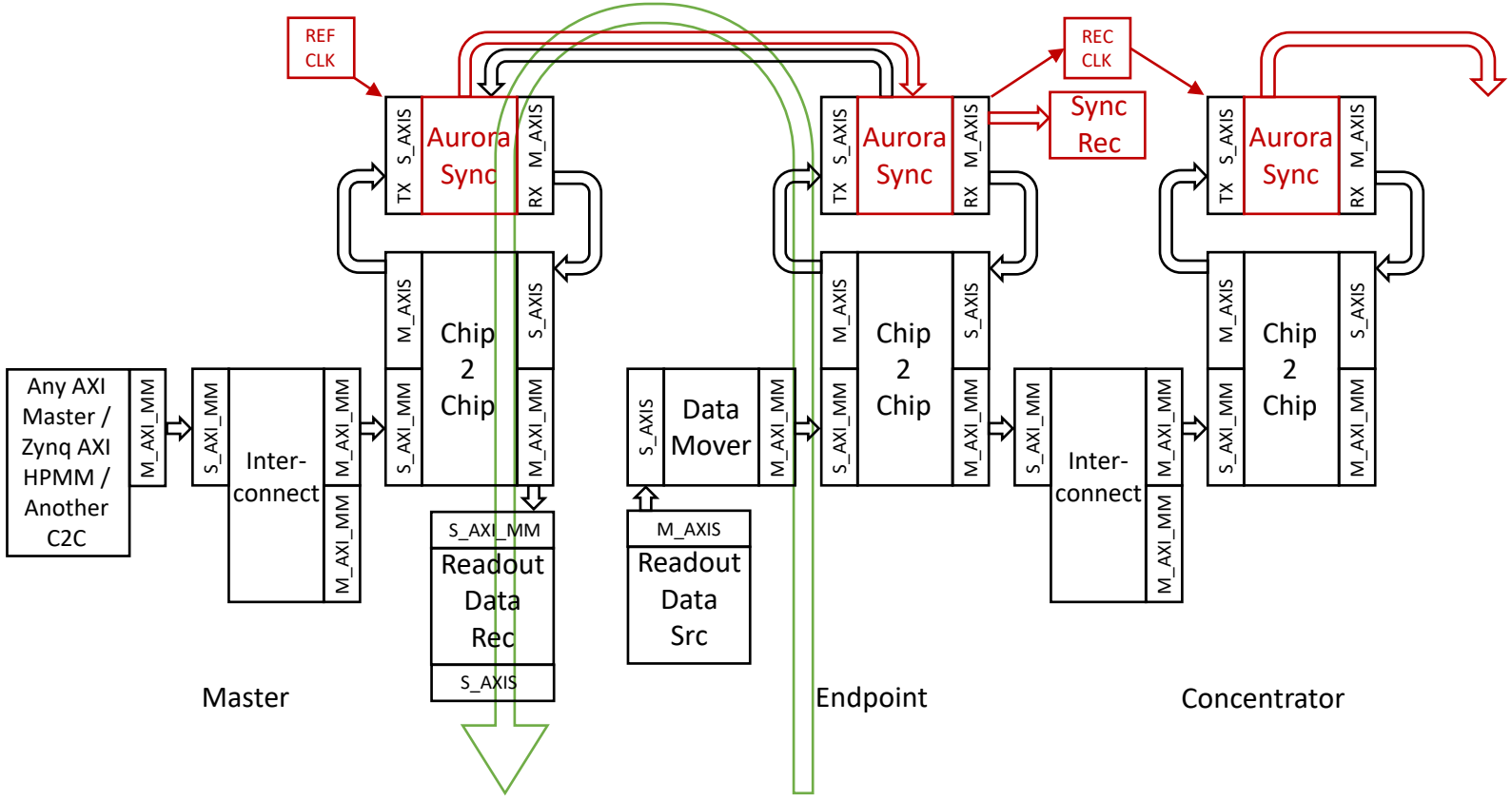




Measured with scope probes on LEDs
Actual, intrinsic jitter expected to be lower

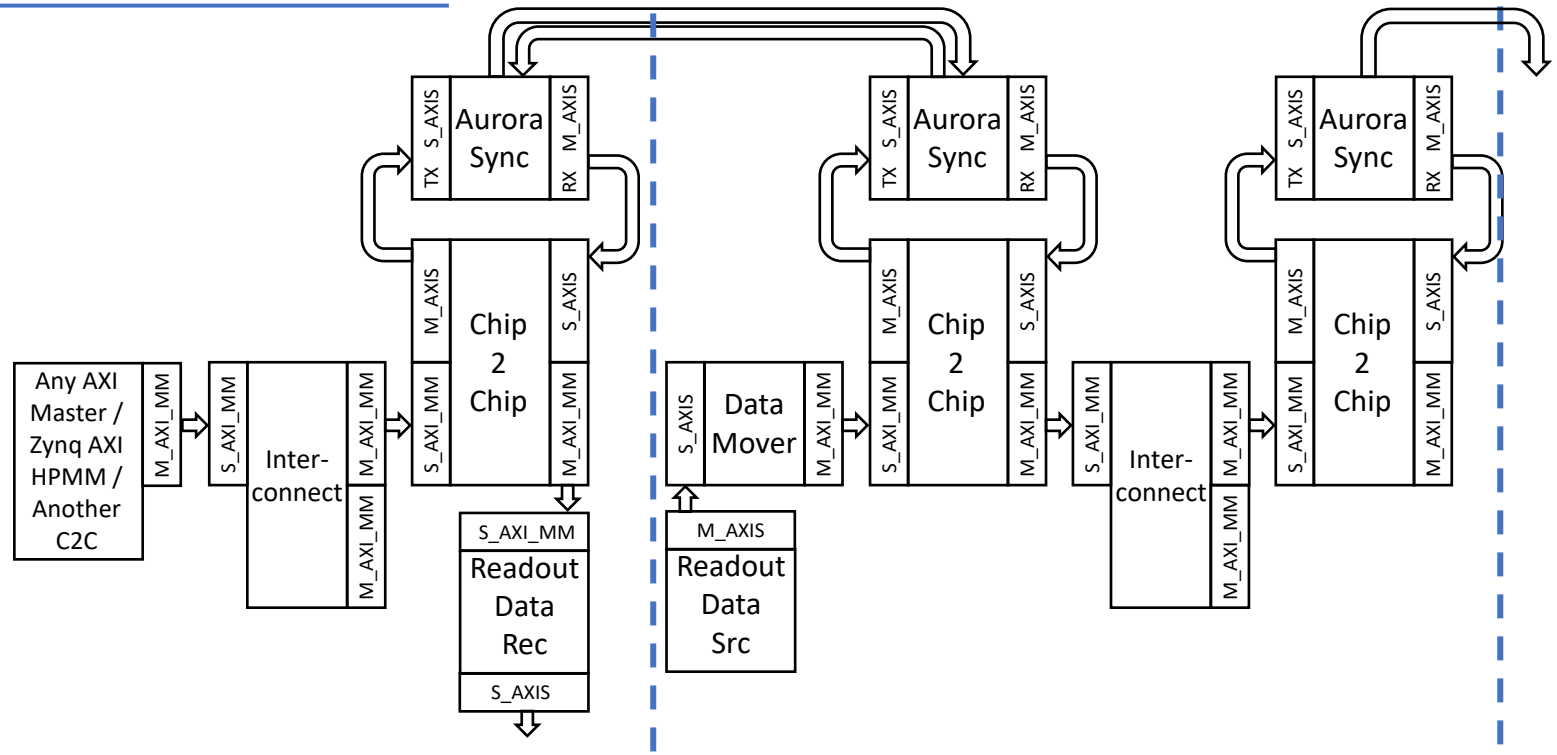
Data transport

- Endpoints continuously buffer measurement data in FIFOs
- Endpoints transfer data to Parent upon reception of SYNC pulse
  - Data Mover converts AXIS to AXIMM
  - Non-synchronous channel
- Parent (Concentrator)
  - Converts AXIMM to AXIS and stores payload in FIFO
  - Aggregates data from all active outgoing links (Data Funnel – round-robin)
    - Timing must be balanced
  - Adds headers and creates AXIS
  - Aggregated packet can be forwarded further to Concentrator Parent
  - Or exported out of the system e.g. Ethernet
- Multiple regions to implement data preprocessing
  - Single Endpoint data or multiple combined
  - AXI interfaces make it easy to implement algorithmics with HLS



Control and Monitoring

- Convenient AXI addressing
- With Zynq as a Master
  - All AXI MM components mapped into Petalinux memory space (32b addressing)
  - Hierarchical address assignment
    - Each link (Chip2Chip) receives a sub-address space
    - Each component is addressable by its location in the system
    - AXI address masking for unified bitfiles
    - Adjustable for particular setup
  - ZeroRPC Python server running on Master
  - Set of Python libraries representing components
  - Easily integrable with control systems



Endpoint:
All remaining sub-address space for local components e.g.:
Comp1: 0xA111_0xA111_FFFF
Comp2: 0xA112_0xA112_FFFF
…

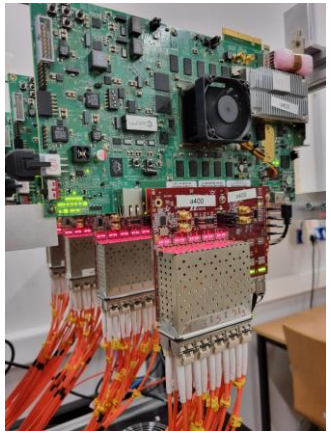
Master:
Each outgoing Chip2Chip has an assigned address range e.g.:
Link 1: 0xA100_0000 – 0xA1FF_FFFF
Link 2: 0xA200_0000 – 0xA2FF_FFFF
…

Concentrator:
Each outgoing Chip2Chip has an assigned sub-address range e.g.:
Link 1: 0xA110_0000 – 0xA11F_FFFF
Link 2: 0xA120_0000 – 0xA12F_FFFF
Reserved local sub-address space for other components e.g.:
Others: 0xA1F0_0000 – 0xA1FF_FFFF

Hardware platforms

ZCU102 dev. board as
- System Master
- Data Concentrator

VU108 dev. board as a
Data Concentrator



MTAB as TDC Endpoint
(M. Kajetanowicz)
XC7A200
65 ch. High-res TDC

SADC as ADC Endpoint
(P. Marciniewski)
2x KC7K160
64 ch. 14b 80MSps ADC

PANDA uTCA
Data Concentrator
(P. Marciniewski)
XCKU15P
70x GT channels over 5x Firefly

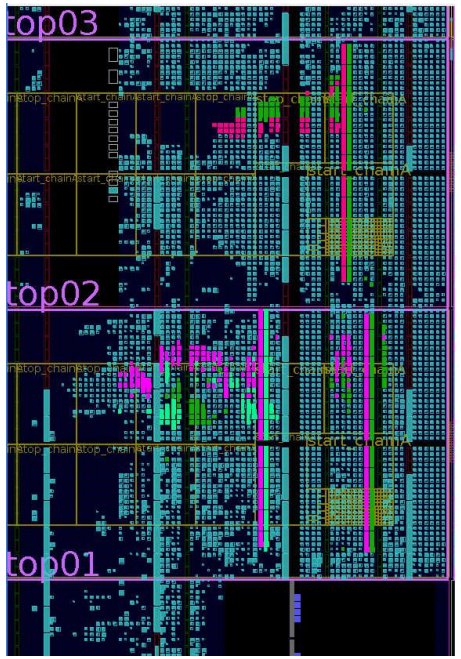
TB-PET as
- multi-TDC Endpoint
- Data Concentrator

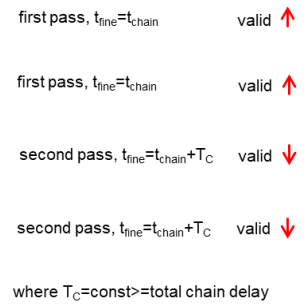
(M. Kajetanowicz)
6x XC7A200 as 65 ch. High-res TDC
1x XC7A200 as Data Concentrator

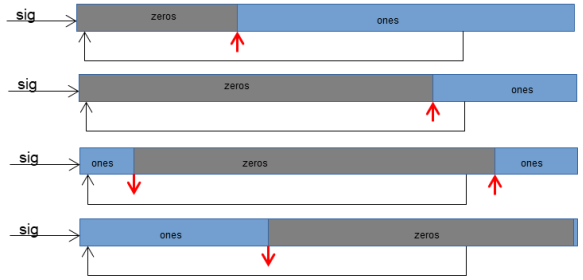
AC701 and KC705 dev.
boards as generic Endpoints

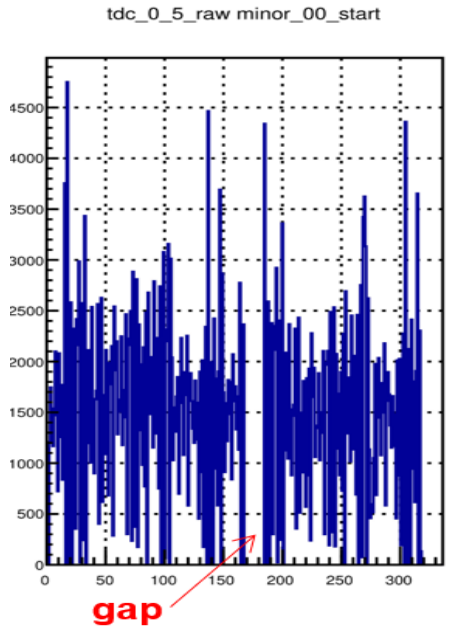
Example complete setup

- System Master
  - ZCU102
- 4x Data Concentrators
  - VCU108
- 48x MTAB TDC
  - Artix7-200
  - 64 + ref channel Tap-Delay TDC
    - 200 MHZ coarse clock
    - Carry Logic blocks chain
      - 70 blocks required to cover 5ns
      - Clock region limitations –> folded chain of 42 blocks (168 taps)
      - Separate chains for leading/trailing edges
      - Offline non-linearity correction
    - Signal digitization with LVDS buffers
  - Aurora Sync Endpoint

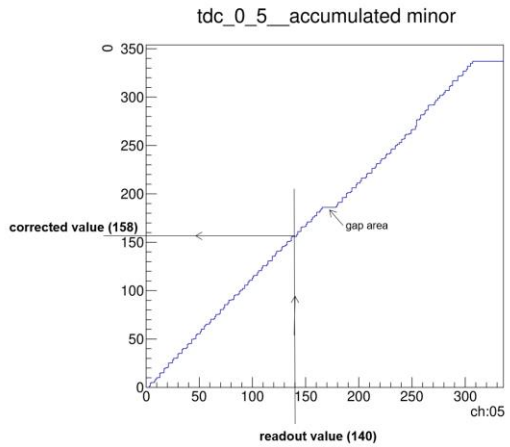




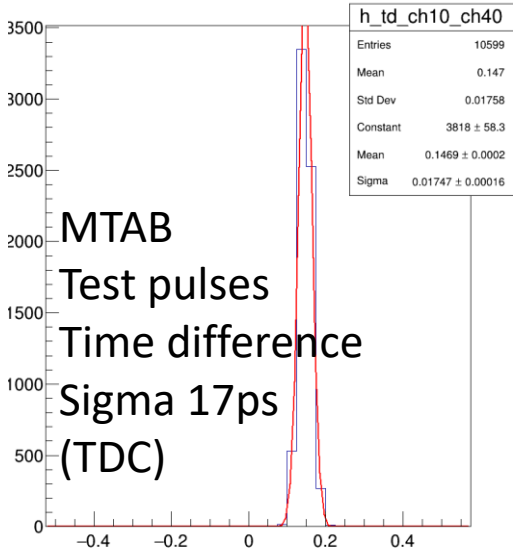




TDC developed by Piotr Kapusta

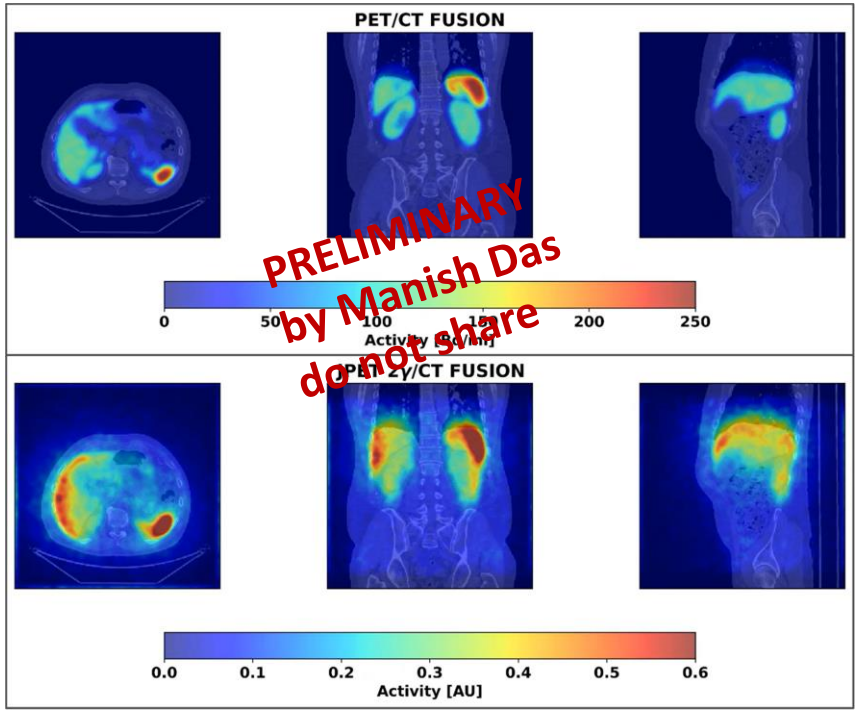


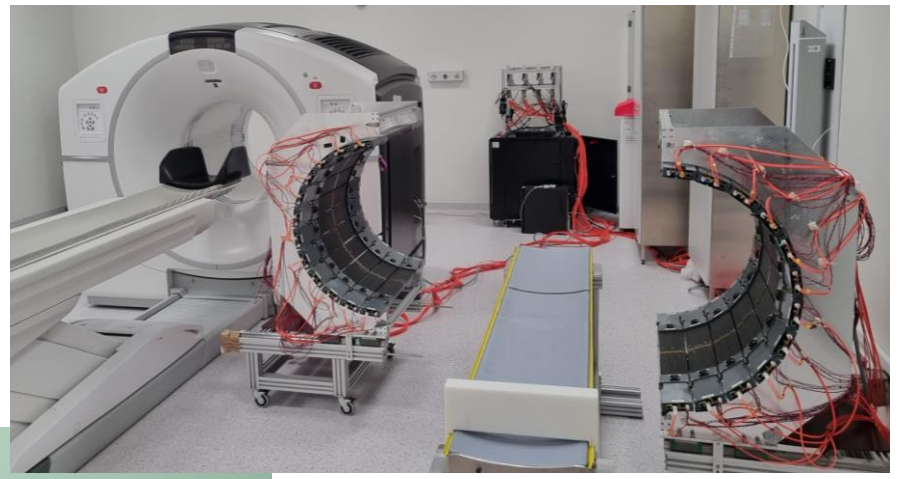
Board developed by Marcin Kajetanowicz



Example complete setup

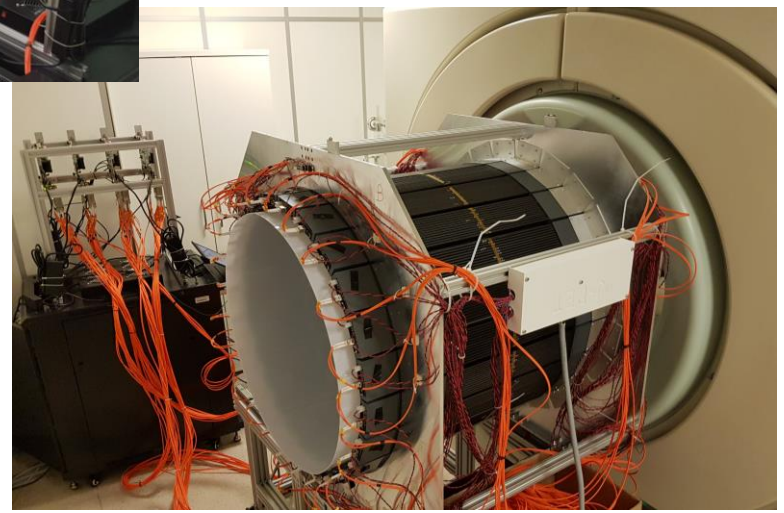
- PET scanner
  - 24 modules of plastic scintillators with Hamamatsu SiPMs
  - Total of 2496 TDC channels
  - 20 kHz SYNC rate
- Stable operation in multiple data taking campaigns
  - Short measurements
  - Multi-week measurements





The University Hospital, Kraków 2024

CCB IFJ PAN, Kraków 2021



Banacha Hospital, Warszawa 2022

Summary

- A complete DAQ solution has been developed
  - Out-of-the-shelf or custom hardware components
    - Generic transceiver and clocking design
  - Easily extensible with new hardware
    - Ready to use components for Xilinx GT families
    - No external PLL required
    - Single data link
  - Complete set of firmware components for:
    - Synchronous channel
    - Measurement data transport
  - Complete set of software components for:
    - High-level, Python based control and monitoring
- System successfully deployed and evaluated with the J-PET scanner
  - Data transport infrastructure + the MTAB TDC platform as Endpoint
- System successfully migrated to custom components for the PANDA experiment
  - Custom Data Concentrator with 70 links + SADC platform as Endpoint
  - Evaluation required