Chiral-Belle Compton eDet Work Update

Chiral Belle SKB e- Polarization Upgrade Working Meeting
December 2023

Michael Gericke

For the U. Manitoba Belle II / ChiralBelle Group

With work mainly done by:

Nafis Niloy (U. Manitoba)

Shefali Prabhakar (U. Manitoba)

Laheji Mohammad (U. Manitoba)

Kristofer Isaac (U. Manitoba)

Omar Hassan (U. Manitoba)

Some figures borrowed from:

Andre Schoening (U. Heidelberg)

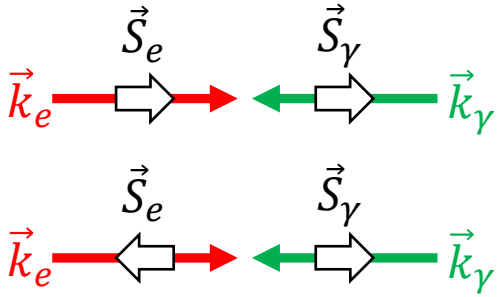
Heiko Augustin (U. Heidelberg)

Alena Weber (KIT)

Outline

- Proposed eDet overview
- Formal overview of the HVMAPS operational principle
- Key HVMAPS performance parameters (present version of the chip)
- Detector development status (MOLLER/JLab Hall A) and adaptability for SKB
- Chip status (including possible upgrades)
- Open questions

Proposed eDet Overview:



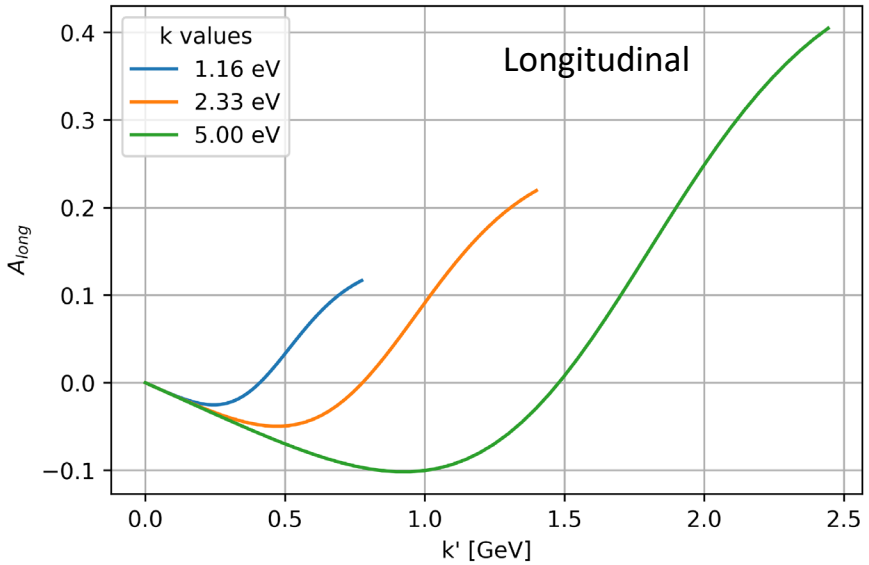
n^+ counts in this mode

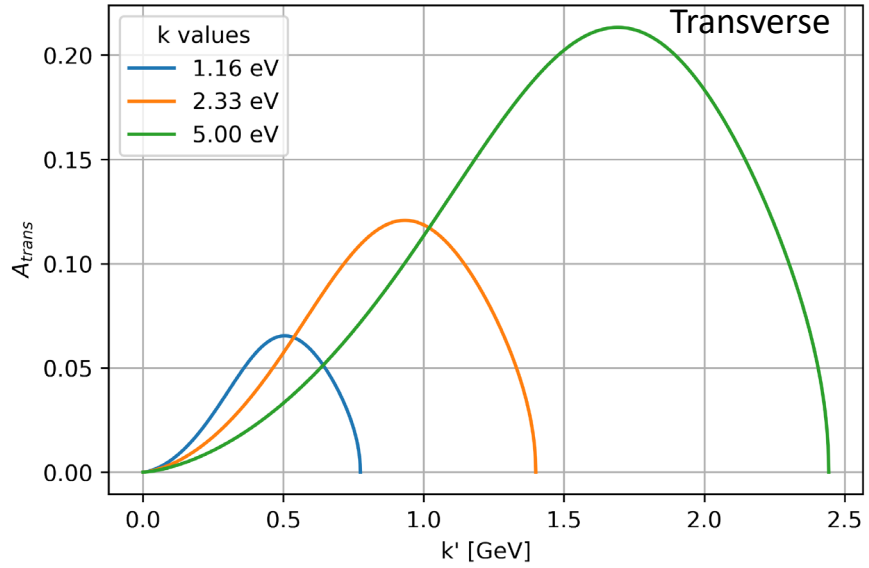
n^- counts in this mode

- Measure the number counts in each mode over equal time periods
- For the experimental asymmetry from detector measurements:

$$A_{exp} = \frac{n^+ - n^-}{n^+ + n^-} = P_\gamma P_e A_l$$

- P_γ : Photon polarization (from laser)
- A_l : Theoretical Compton asymmetry (precisely known)
- P_e : Electron (beam) polarization:



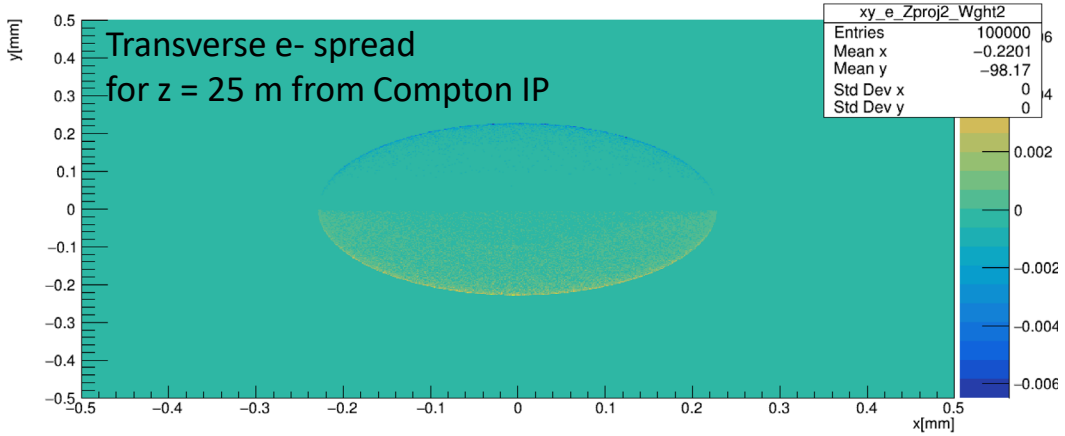


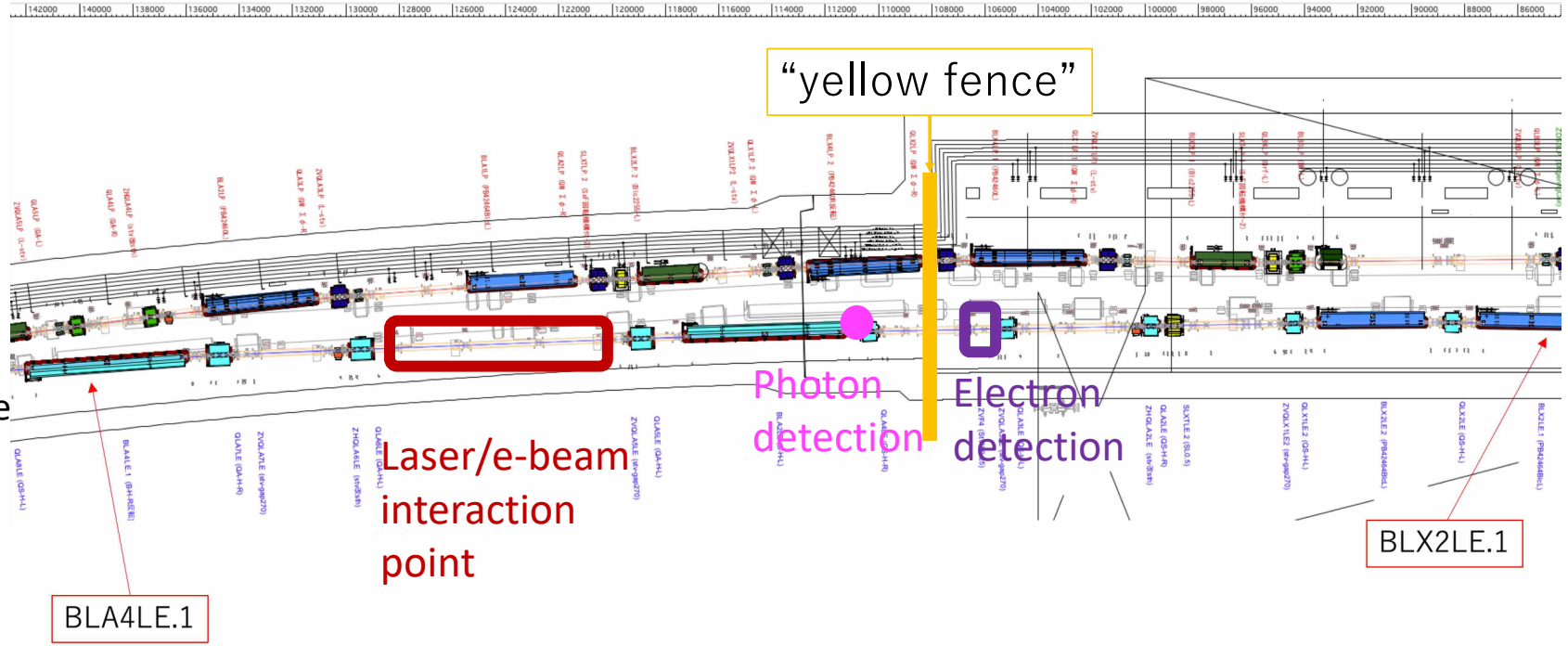
Proposed eDet Overview:

- Have to measure the polarization as a function of scattered photon and/or electron energy
- For the electrons – energy is related to recoil momentum
- Measure scattered electron energy by deflection in magnetic field (beam line field ?)
  - Higher photon energy $\rightarrow$ lower electron energy
  - Lower electron energy $\rightarrow$ more bending away from primary beam
- Need to build a detector that can accurately measure electron deflection (distance away from primary beam at some specified distance)
- Either strip or pixel detector located close to the un-scattered (laser off) beam trajectory
- Multiple detectors along 25 m beamline stretch

Proposed eDet Overview:

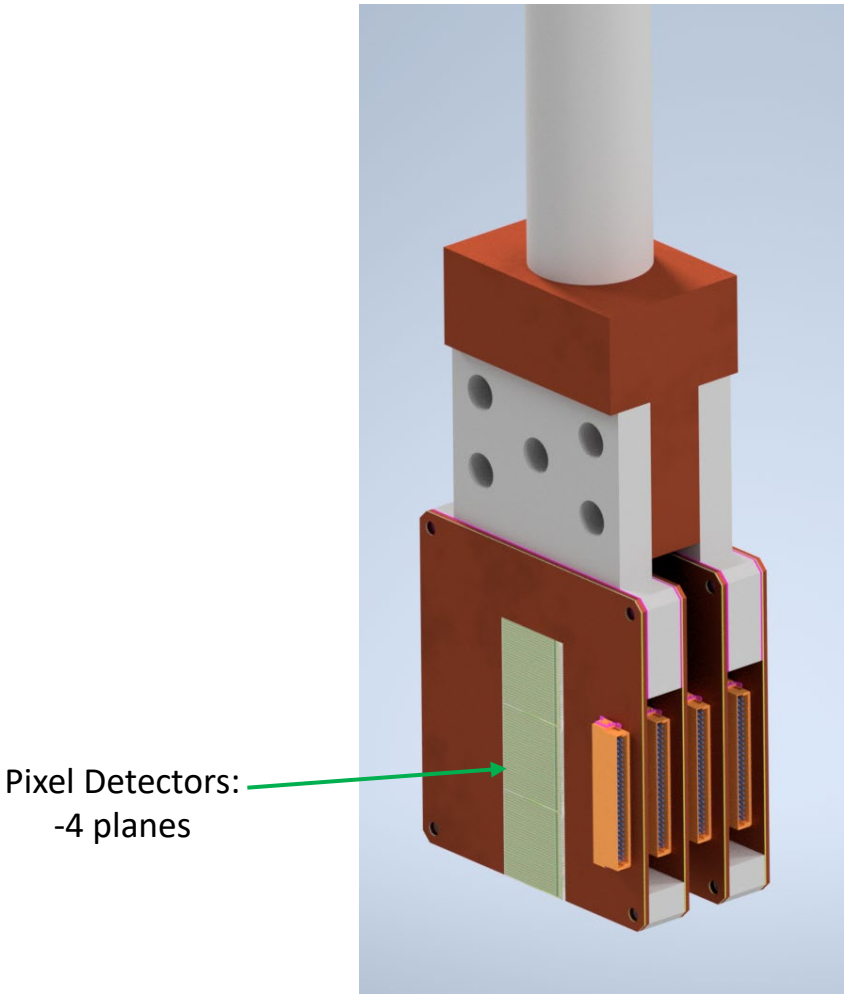
- eDet at $z = 25\ m$ produces very small spread in x/y over very few pixels
- Would require an additional dispersive magnet with a fairly high field to improve this (probably not in the cards)
- Maybe put small Be windows at selected locations with detectors at those locations
  - Pixel detectors not normally needed for this, but
  - Could have a couple of planes at several locations to improve S/N and background rejection
  - Would require more simulations





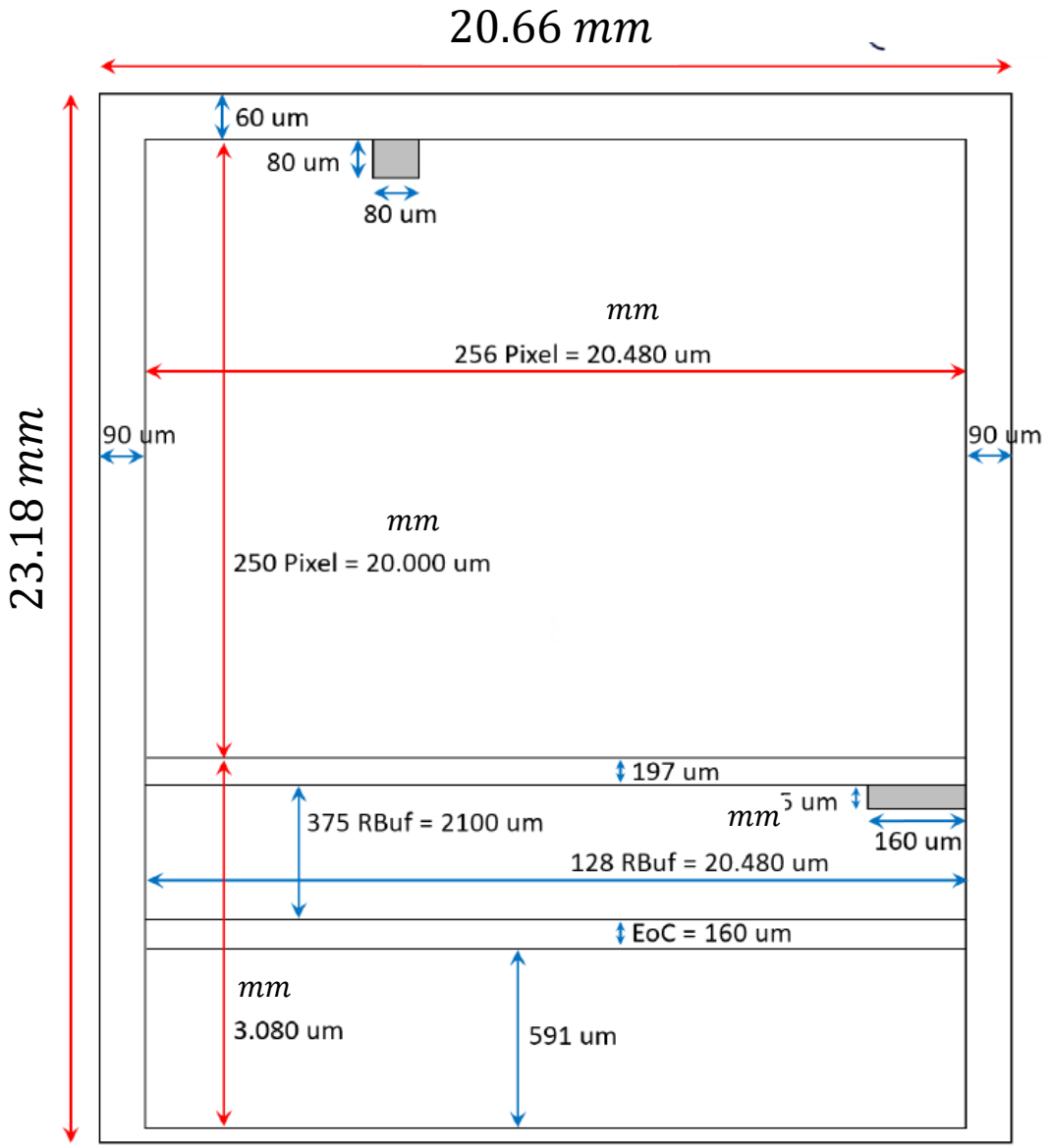
Proposed eDet Overview:

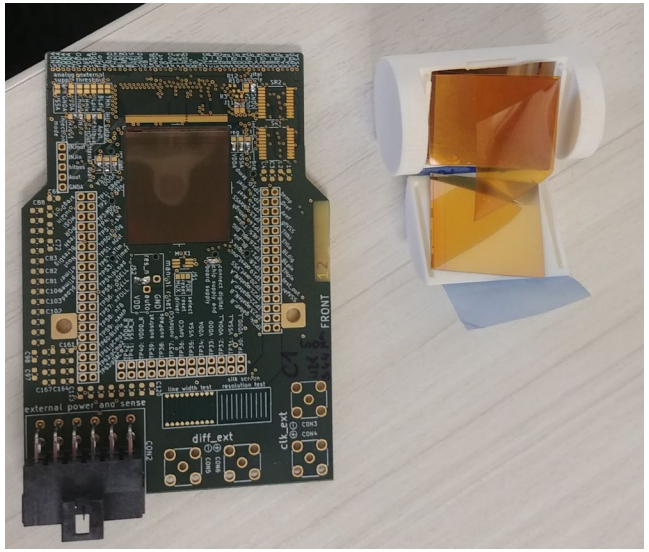
- Have to use existing beam line dipoles to analyze the electron energy / hit rate correlation
- It would not be in a straight line-of-sight to Compton IP
- Have to model transport or measure transverse polarization
- Possibly implement several small thin Beryllium windows in beampipe to allow electrons to exit primary beam vacuum at selected locations
- Position resolution of the eDet could be used to do tracking of the scattered beam electrons and reduce background and improve S/N
- Detectors could be located in air, right in front of the Be windows
- Current design for JLab Hall-A aims for 4 planes – could have one of these at each location



Operational principle:

- The final size of the individual chips is ~20 mm by 23 mm
- 64000 pixels per chip ($80\ \mu m \times 80\ \mu m$)
- Several of them are to be combined to form a plane of whatever size is needed

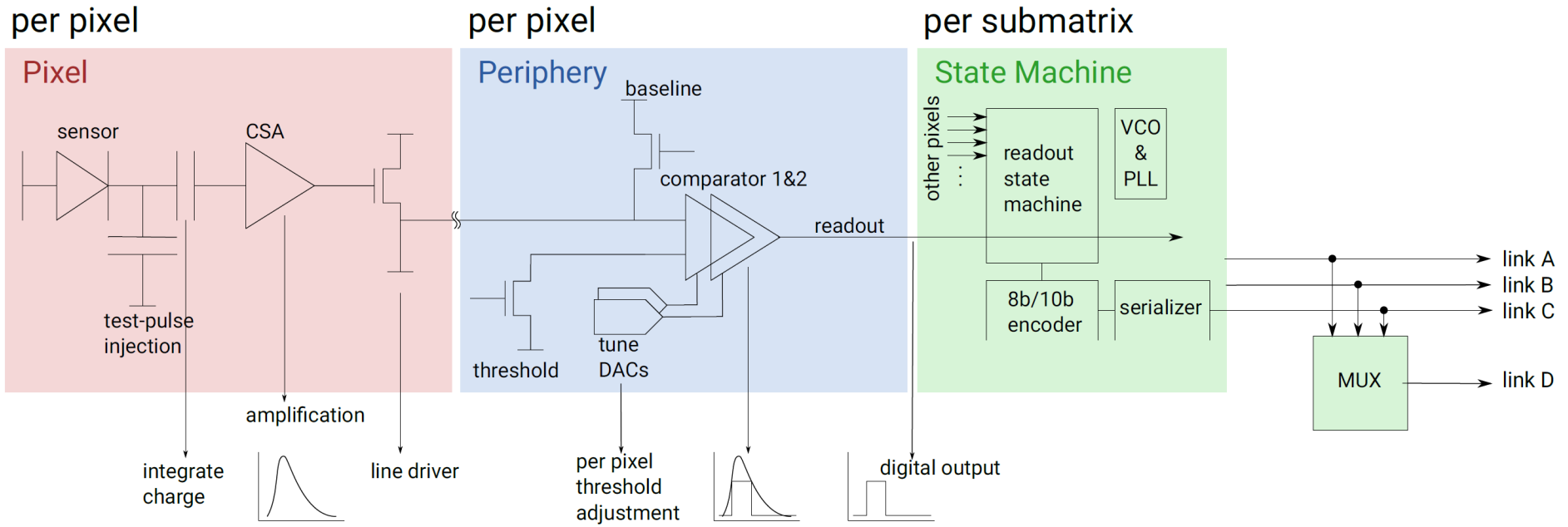




Summary of HV-MAPS operation (with figures by Heiko Augustin, Alena Weber, and Andre' Schoening – U. Heidelberg)

- There are three distinct areas of the chip:

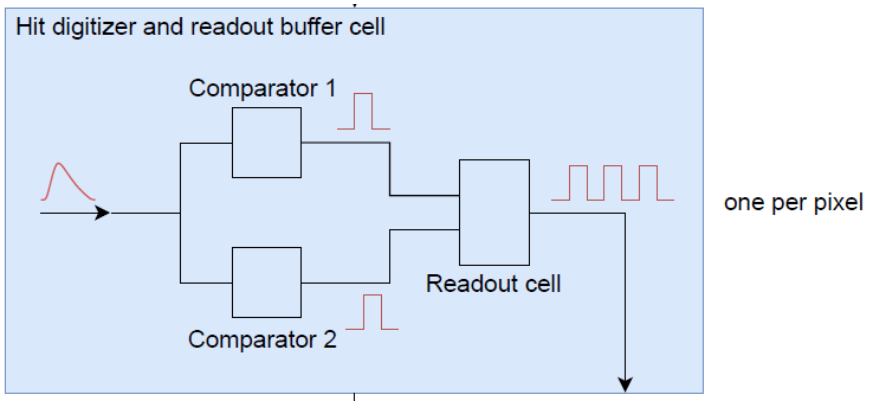
  1. The pixel area, in which each of the 64000 pixels include an amplifier and a line driver to connect the pixel to the periphery
  2. The mirror pixel area at the chip periphery, which includes two tunable ToT comparators
  3. Three state machines at the chip periphery and a mux for data transfer

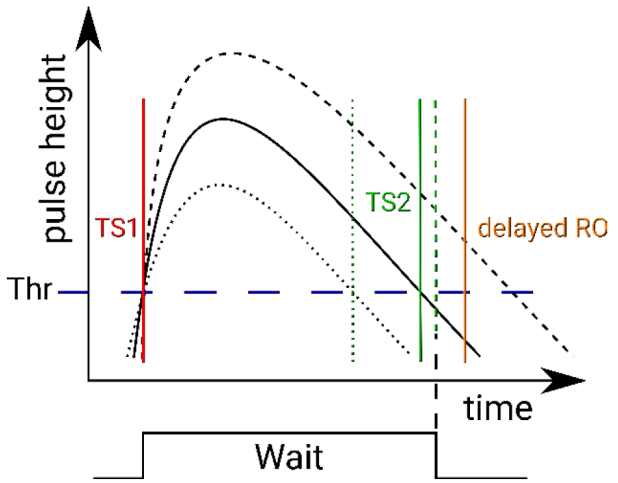


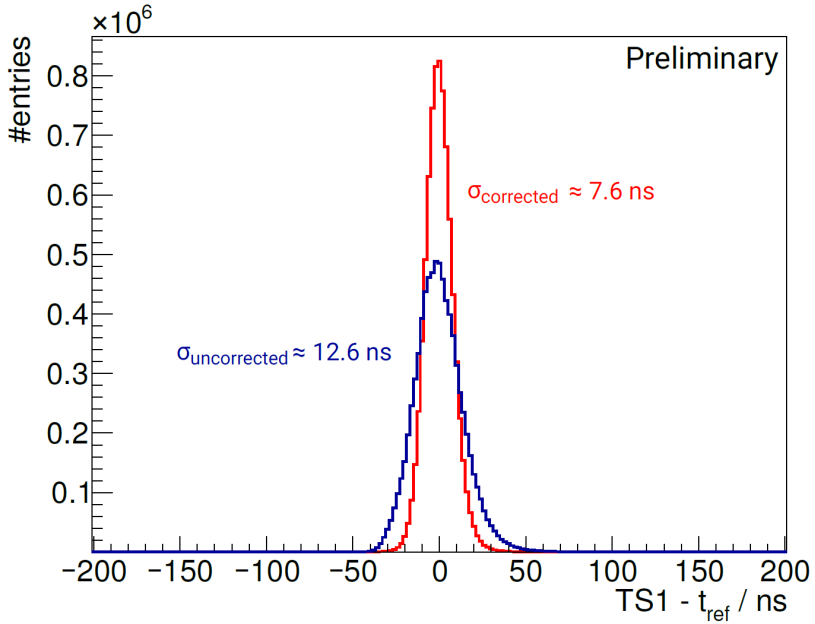
Summary of HV-MAPS operation

- Signal digitization and time stamp generation:

1. Each pixel drives the amplified hit signal to a dedicated readout buffer at the chip periphery
2. The two comparators for each pixel are part of the readout buffer circuitry
3. The readout buffer generates two timestamps. The first one sets the hit latch. The second one establishes the ToT proportional to the collected charge and reduces time-walk effects.
4. The buffer stores an 8b pixel row address and the two timestamps (TS1 = 11b and TS2 = 5b)

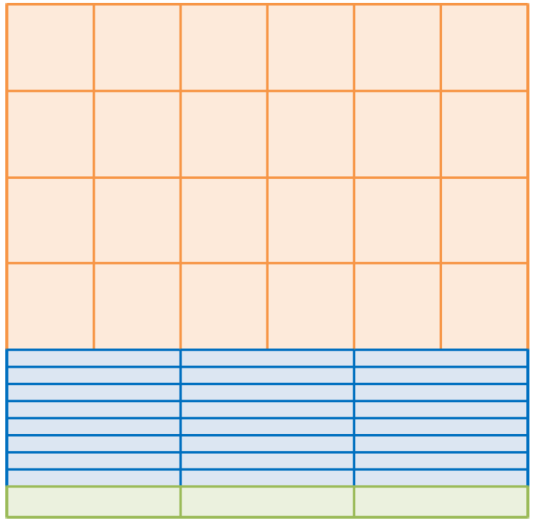


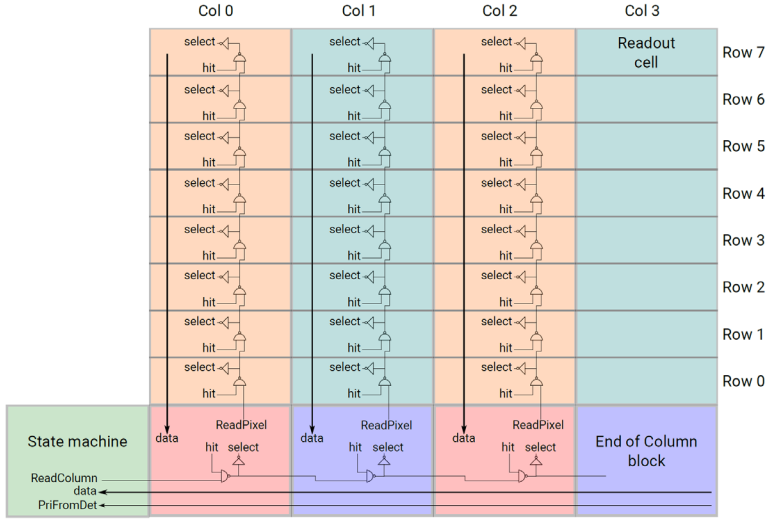




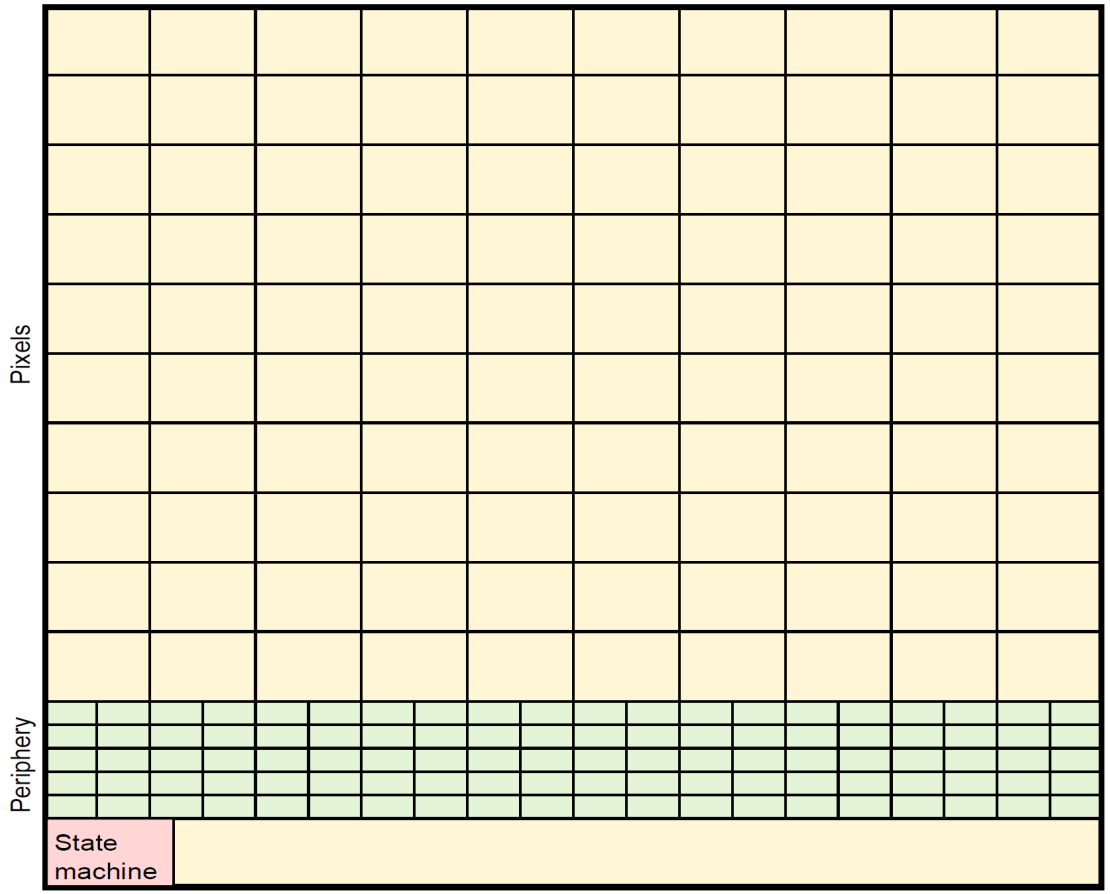
Summary of HV-MAPS operation

- Chip event readout organization:
  1. The chip is readout in column-drain and row readout sequence. There are 250 rows and 256 columns
  2. Pixels buffers with hits are transferred to an EoC (End of Column) cell, selected by a priority logic.
  3. If a pixel buffer hit state is transferred to the corresponding EoC, the buffer is cleared and the pixel is sensitive to new hits again.
  4. The EOC contains an 8b column address and collects the full 32b hit information
  5. The priority chain within a column is based on pixel position and hit time
  6. The state machine generates signals to transfer the pixel hit information to the EoC and transfer the 32 bit EoC data to the serializer
  7. The 32b data words are byte serialized and 8b/10b encoded





Summary of HV-MAPS operation

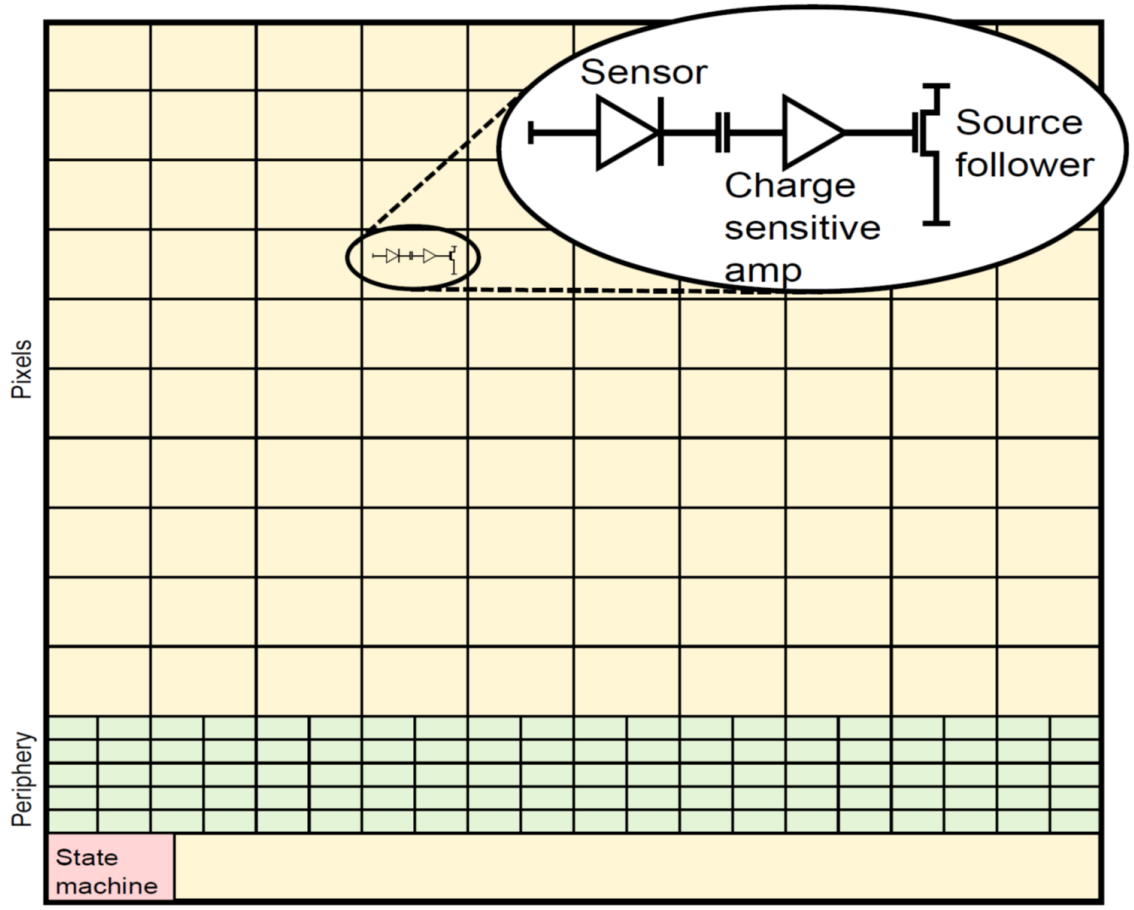


Pixel area

Pixel buffer area

Readout logic

Summary of HV-MAPS operation

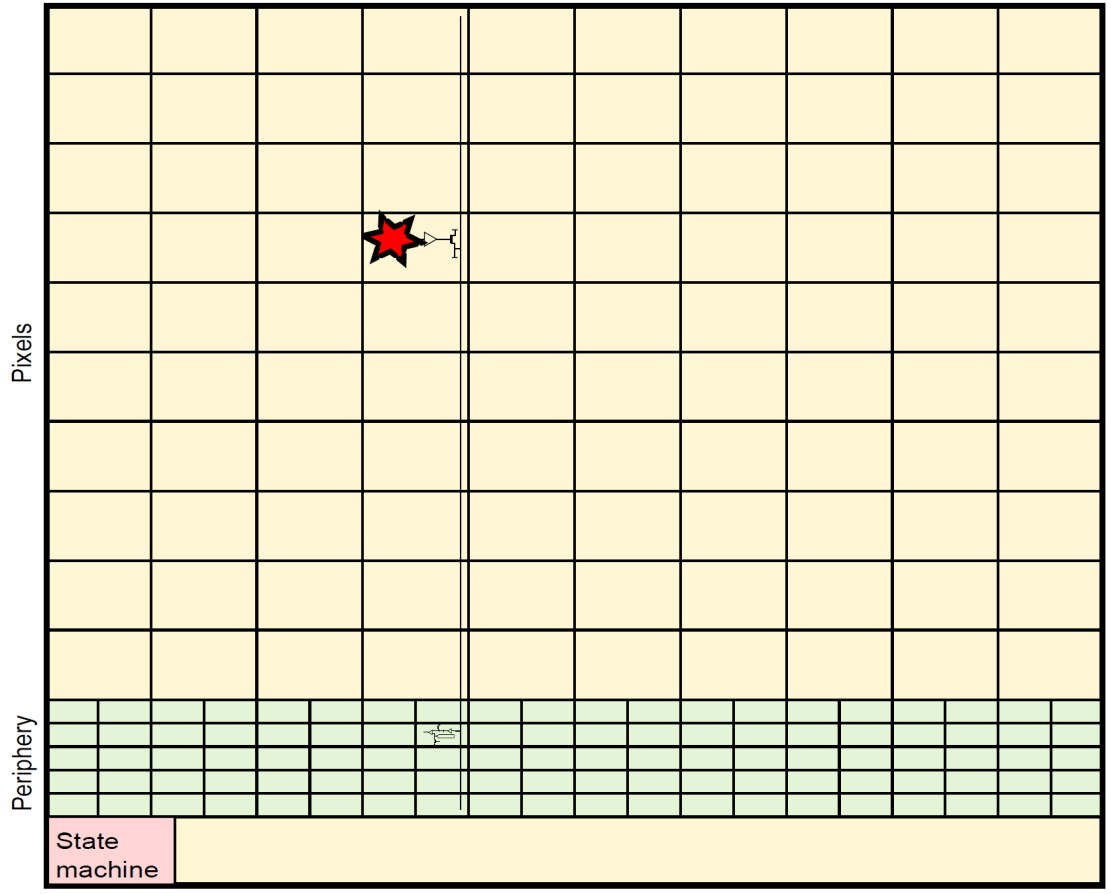


Pixel area

Pixel buffer area

Readout logic

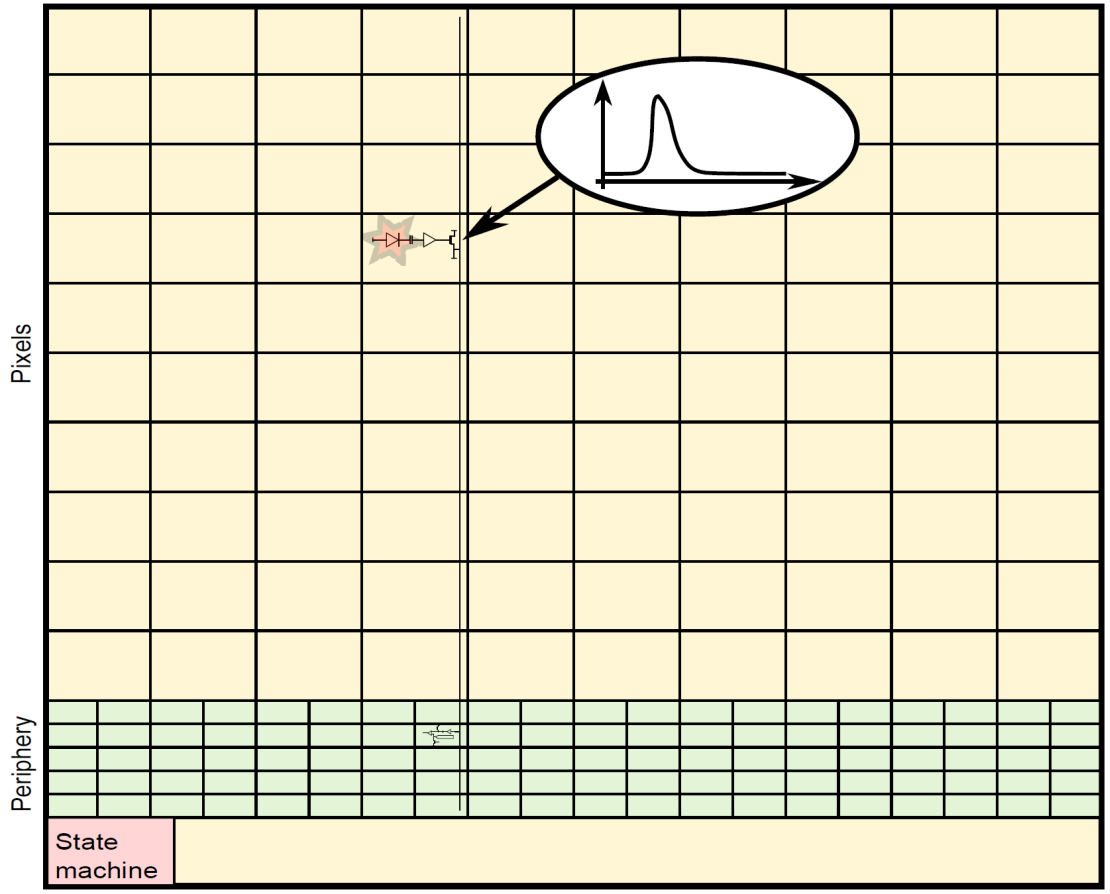
Summary of HV-MAPS operation



Event Sequence:

- **Signal**

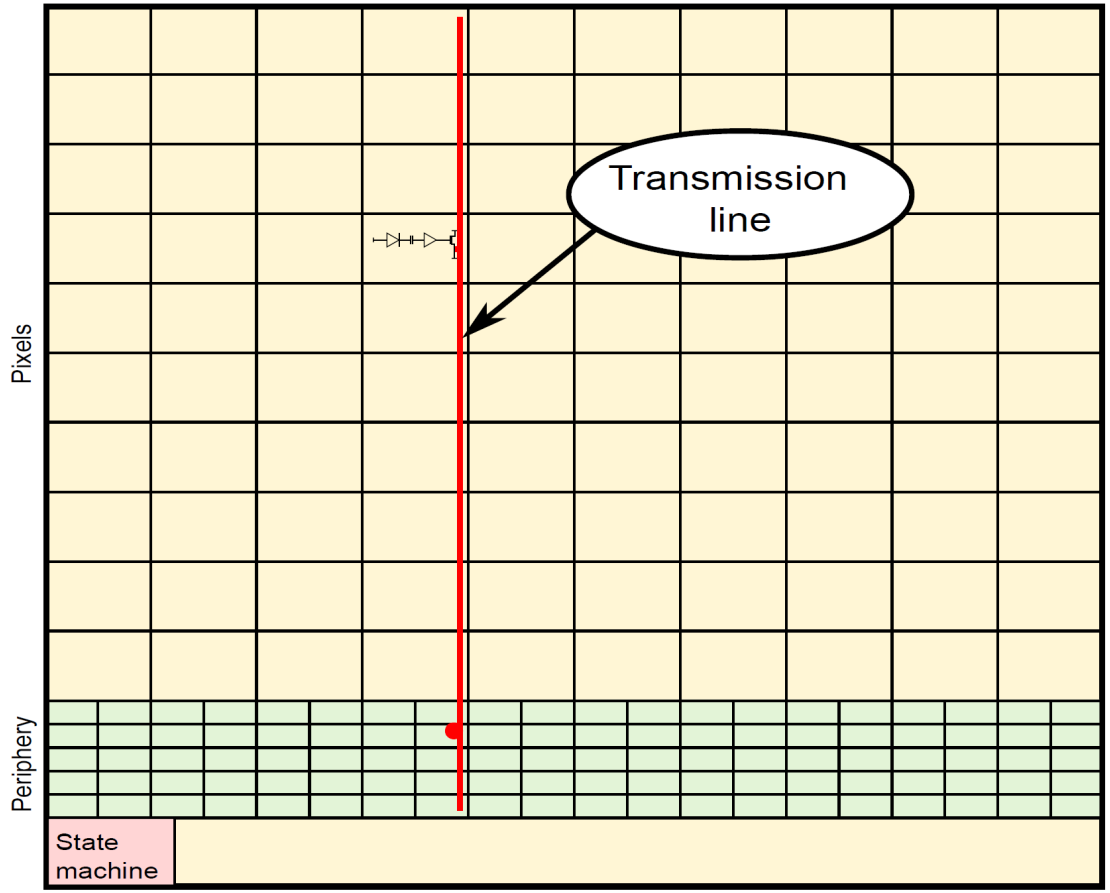
Summary of HV-MAPS operation



Event Sequence:

- **Signal**
- **Amplification**

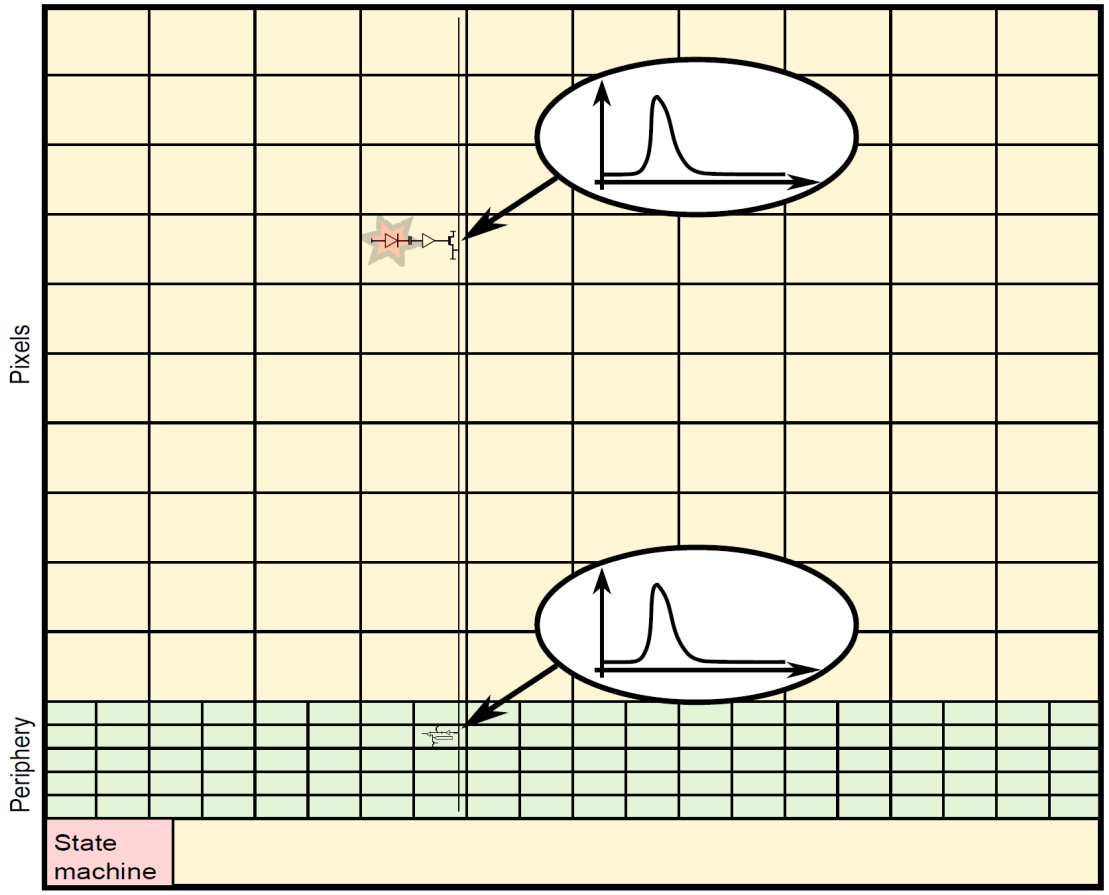
Summary of HV-MAPS operation



Event Sequence:

- **Signal**
- **Amplification**
- **Transmission to periphery**

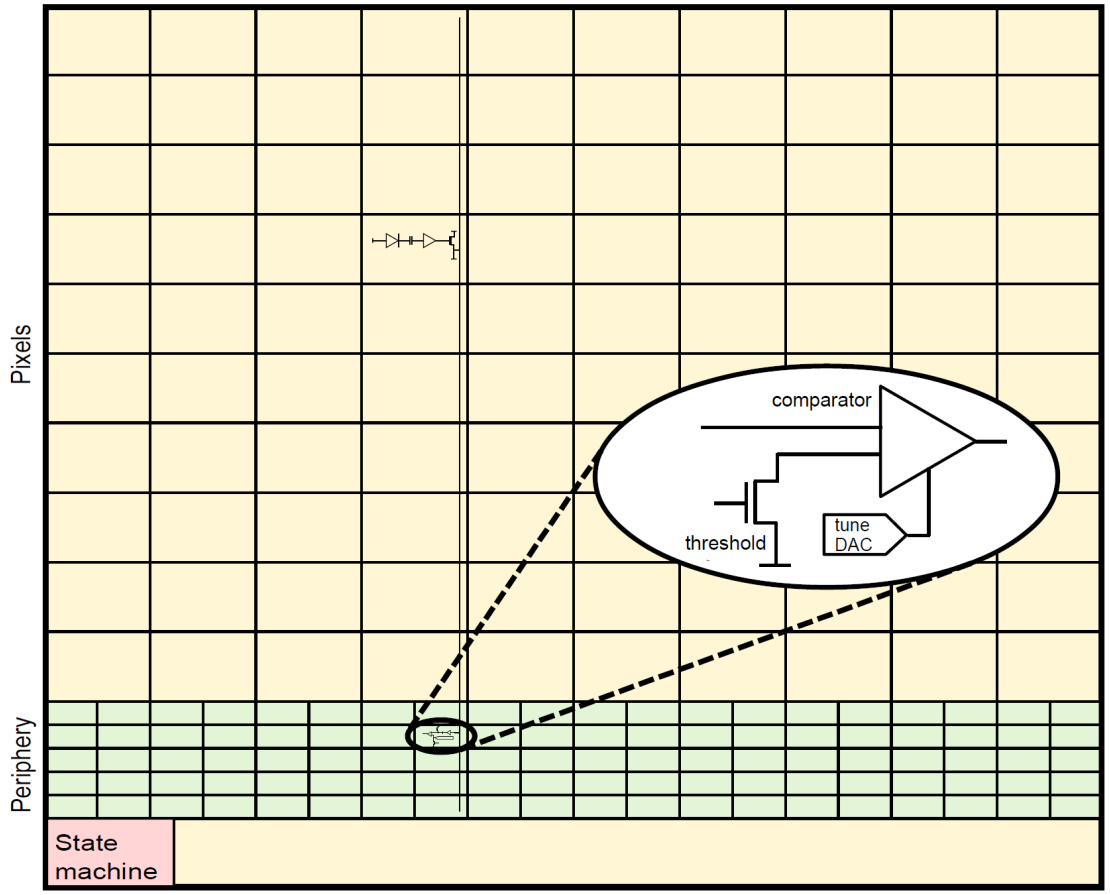
Summary of HV-MAPS operation



Event Sequence:

- **Signal**
- **Amplification**
- **Transmission to periphery**
- **Storage in the buffer (pixel cleared for next event)**

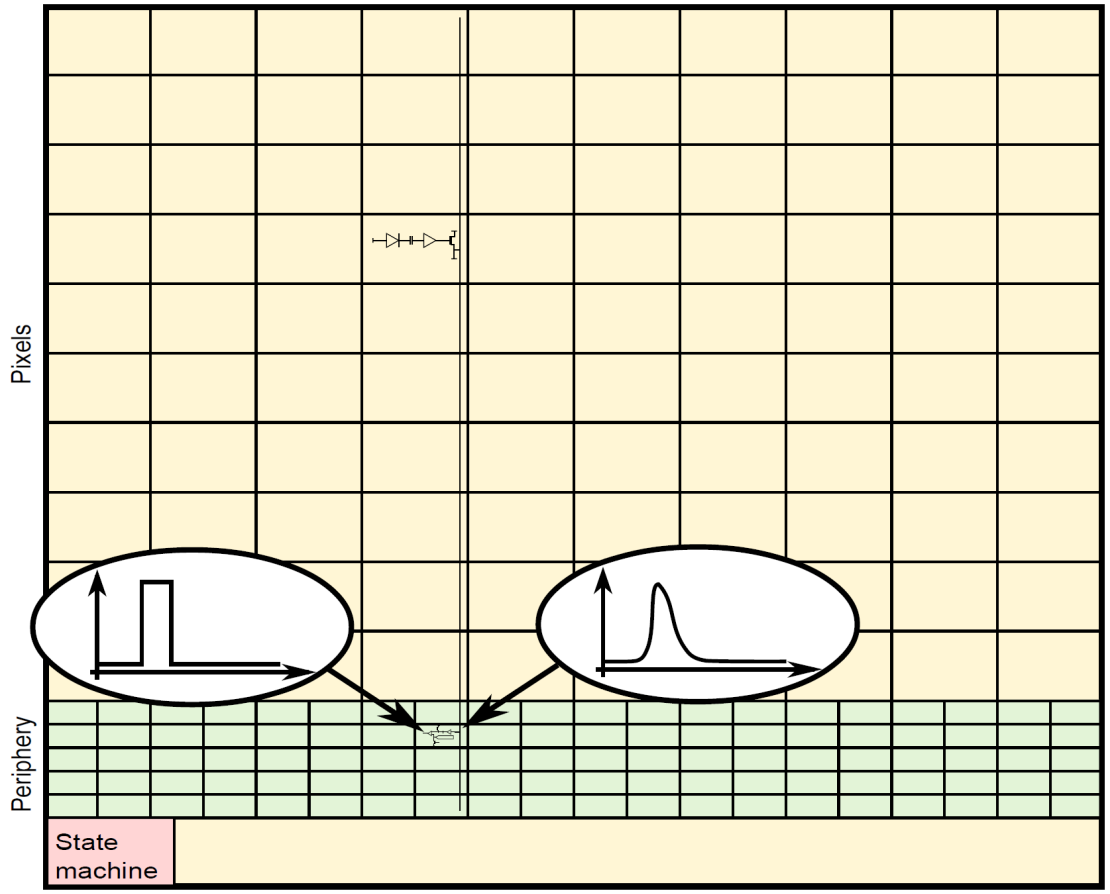
Summary of HV-MAPS operation



Event Sequence:

- **Signal**
- **Amplification**
- **Transmission to periphery**
- **Storage in the buffer (pixel cleared for next event)**
- **Digitization of the hit**

Summary of HV-MAPS operation



Event Sequence:

- **Signal**
- **Amplification**
- **Transmission to periphery**
- **Storage in the buffer (pixel cleared for next event)**
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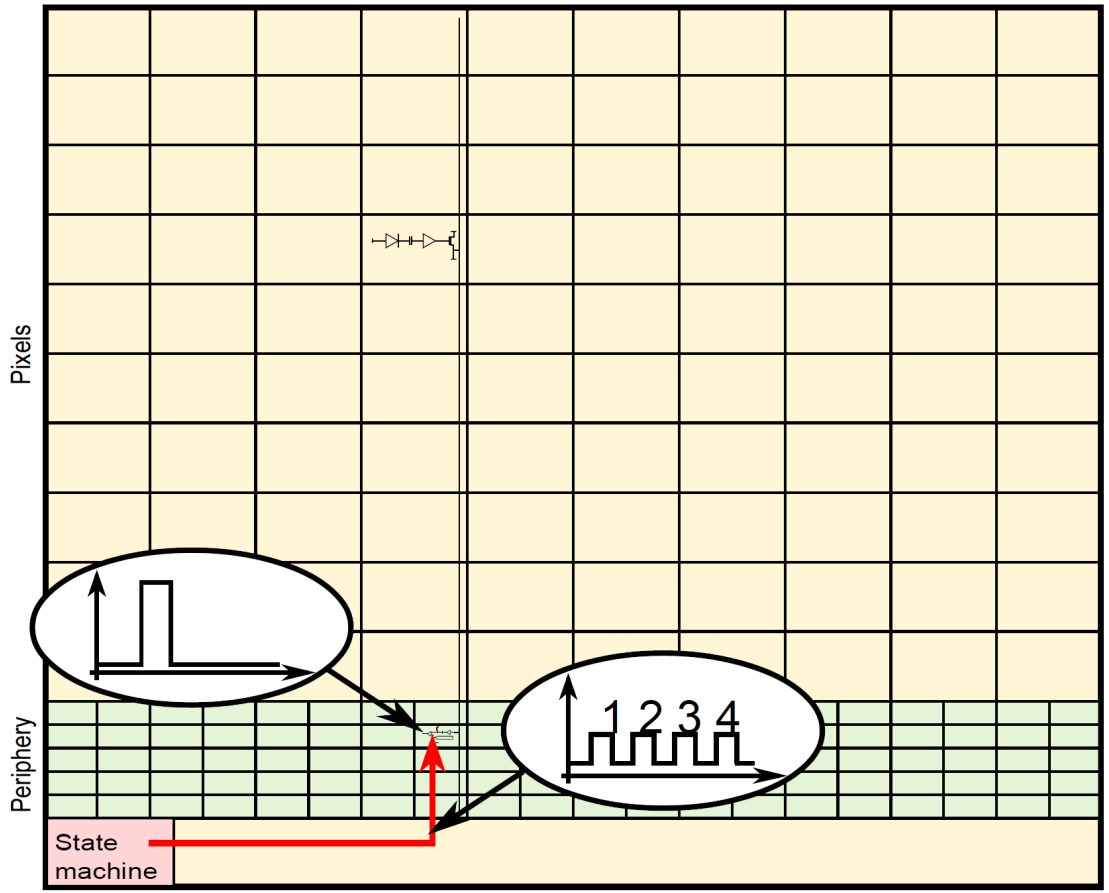
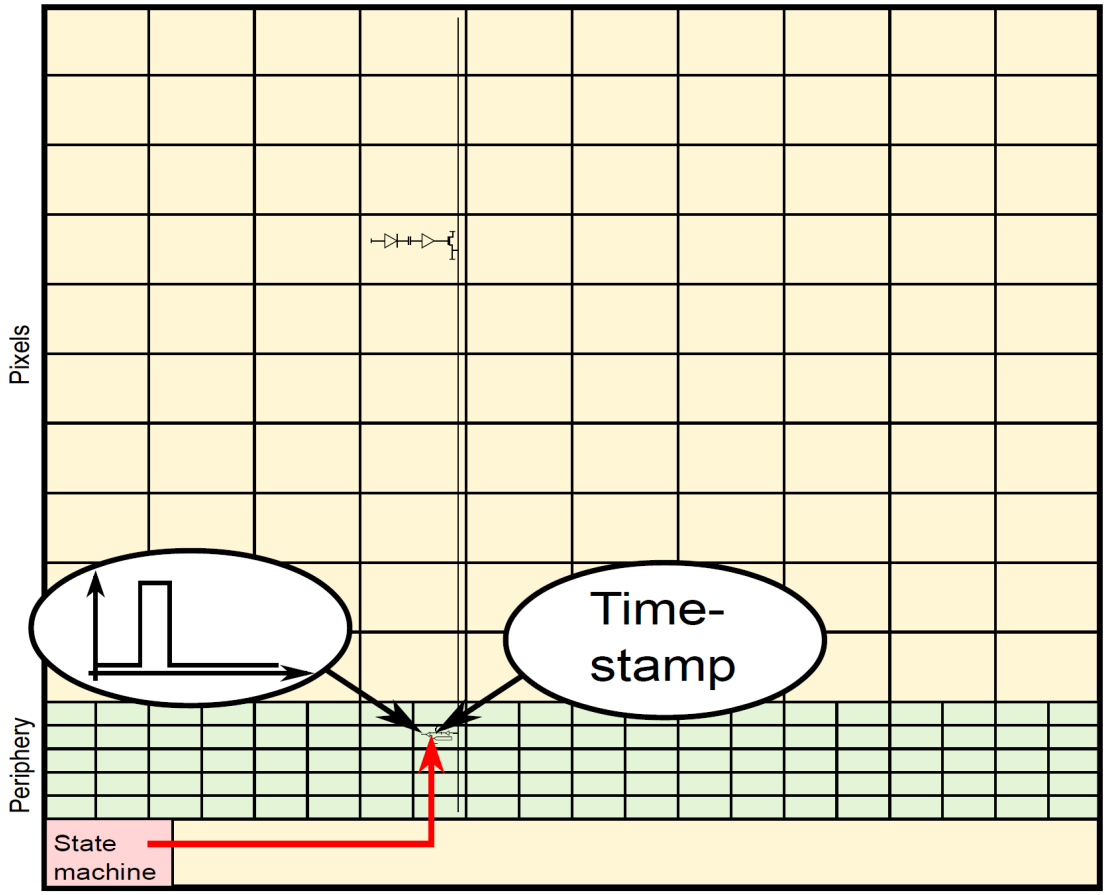
Summary of HV-MAPS operation



Event Sequence:

- Signal
- Amplification
- Transmission to periphery
- Storage in the buffer (pixel cleared for next event)
- Digitization of the hit
- Scalar generated from clk

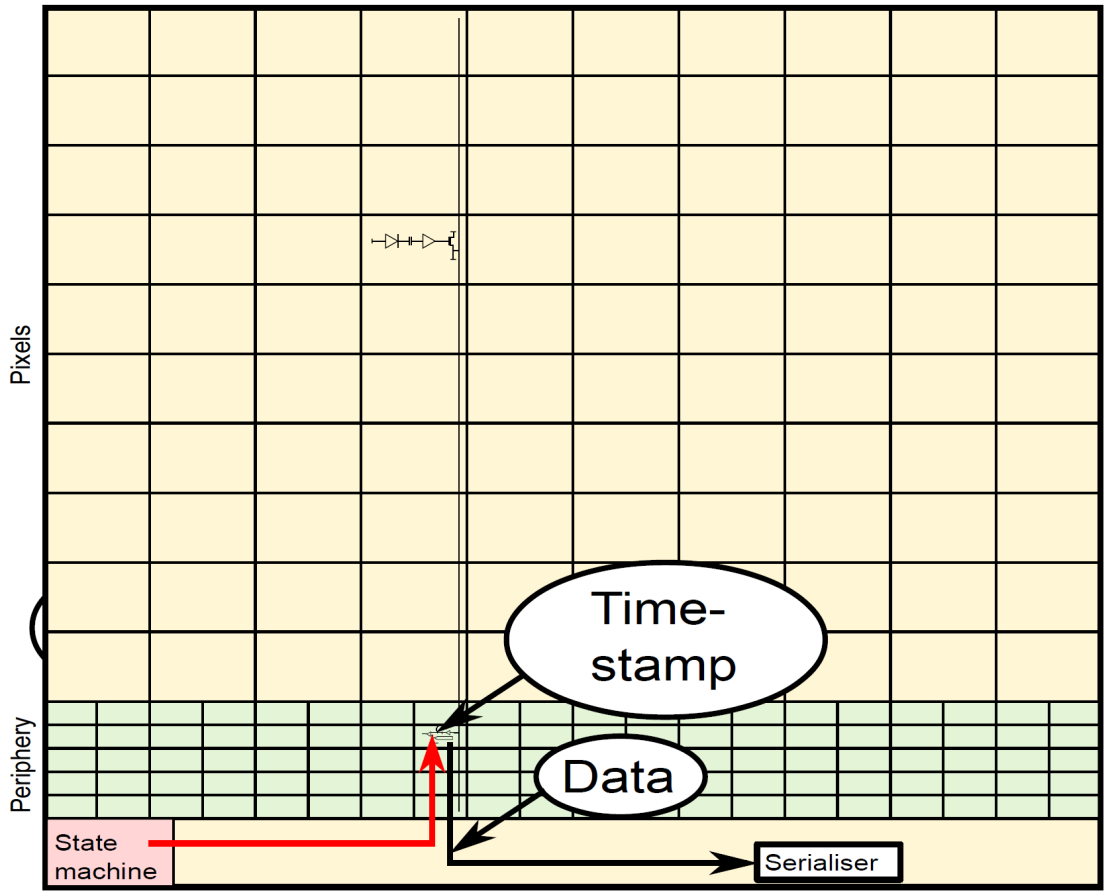
Summary of HV-MAPS operation



Event Sequence:

- Signal
- Amplification
- Transmission to periphery
- Storage in the buffer (pixel cleared for next event)
- Digitization of the hit
- Scalar generated from clk
- Timestamp generation

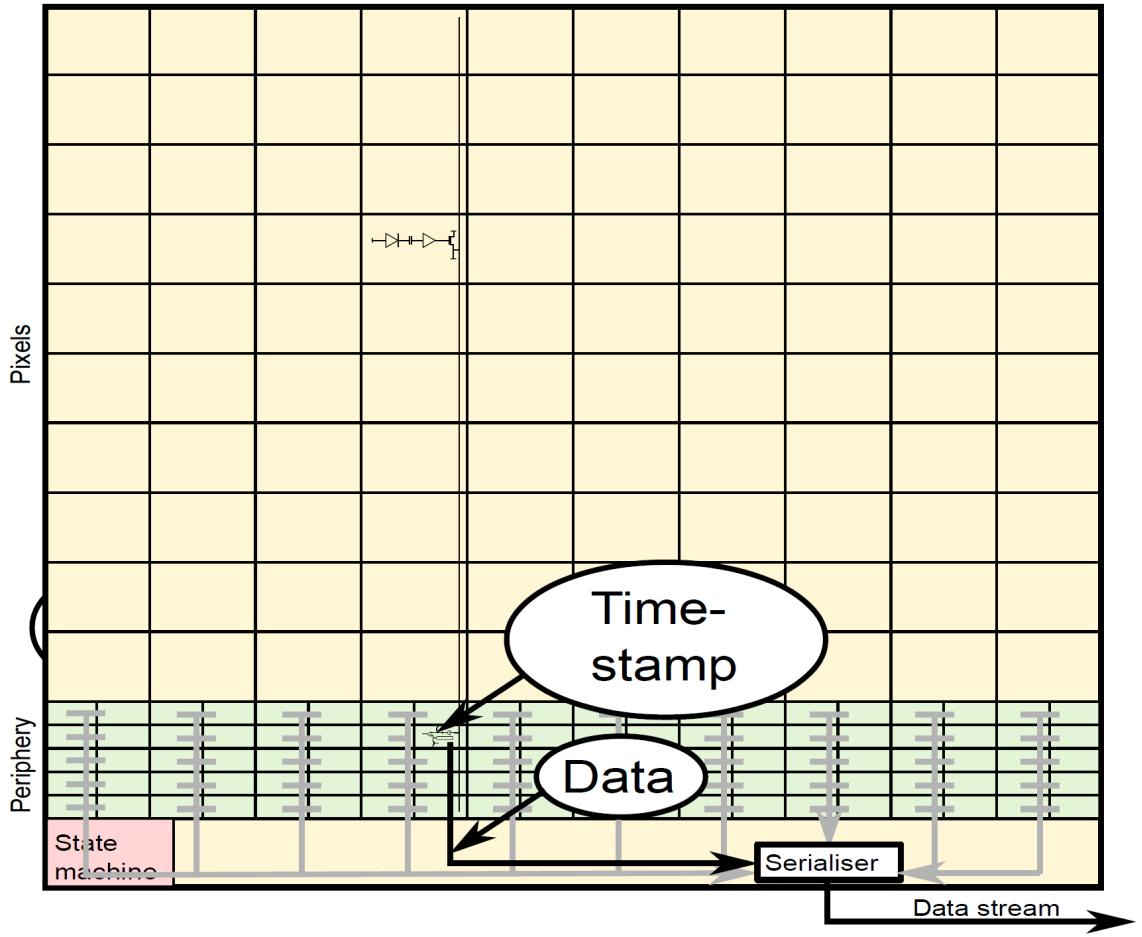
Summary of HV-MAPS operation



Event Sequence:

- Signal
- Amplification
- Transmission to periphery
- Storage in the buffer (pixel cleared for next event)
- Digitization of the hit
- Scalar generated from clk
- Timestamp generation
- Hit/pixel address and timestamp sent to serializer

Summary of HV-MAPS operation

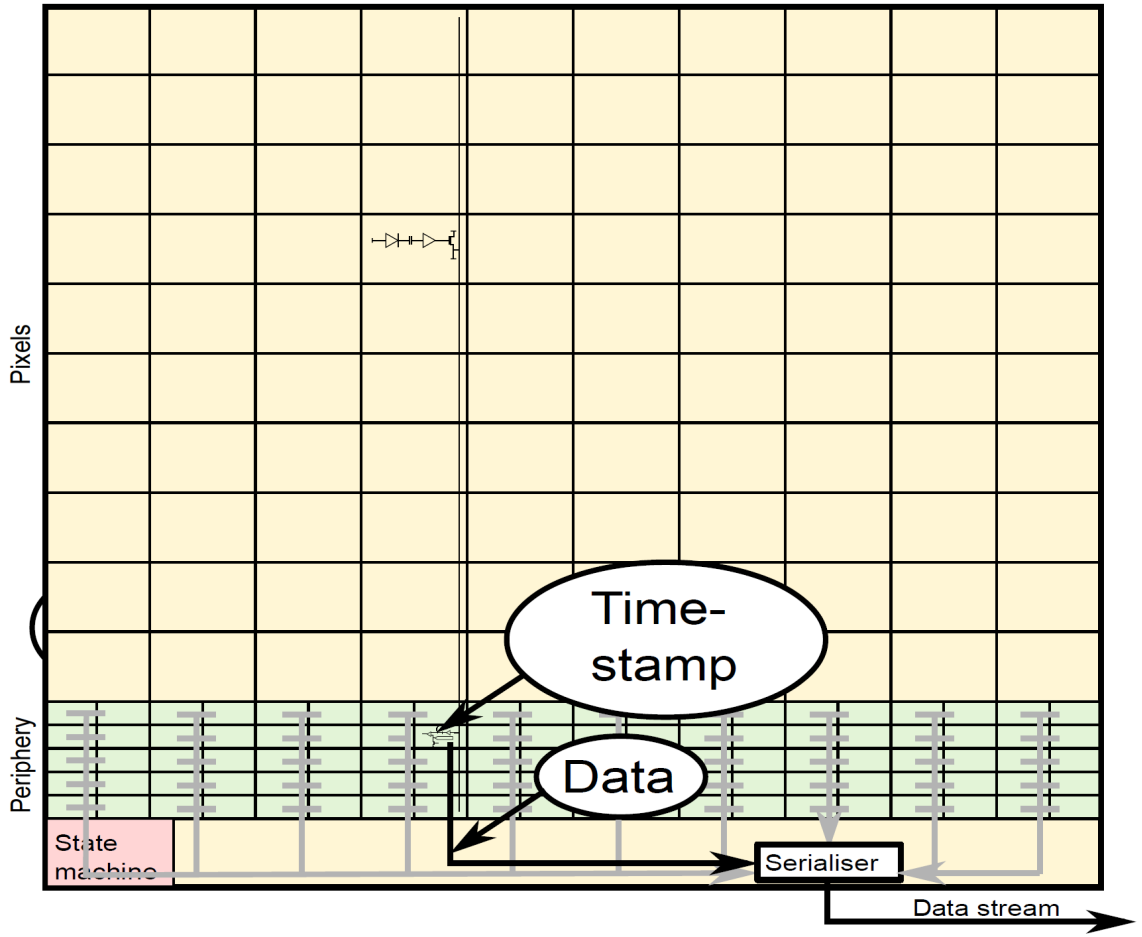


Event Sequence:

- **Signal**
- **Amplification**
- **Transmission to periphery**
- **Storage in the buffer (pixel cleared for next event)**
- **Digitization of the hit**
- **Scalar generated from clk**
- **Timestamp generation**
- **Hit/pixel address and timestamp sent to serializer**
- **Data sent to readout board**

Maximum readout rate is 33 MHz per link with a maximum of 3 links per chip.

Summary of HV-MAPS operation



Minor modifications to final chip:

- **Match the on-chip clk to the CERN readout chip frequency**
- **A simple AND with a GATE link before each pixel buffer to turn on/off the readout – timed to choice to reduce pixel occupancy**

These changes are relatively simple and underway.

Need to resubmit for one more engineering run

Then go to chip production – hopefully at the end of the year

Readout Setup

We need to design and prototype a readout board that incorporates 4 lpGBT chips and 1 VTRx+, plus bias and LV power supply distribution.

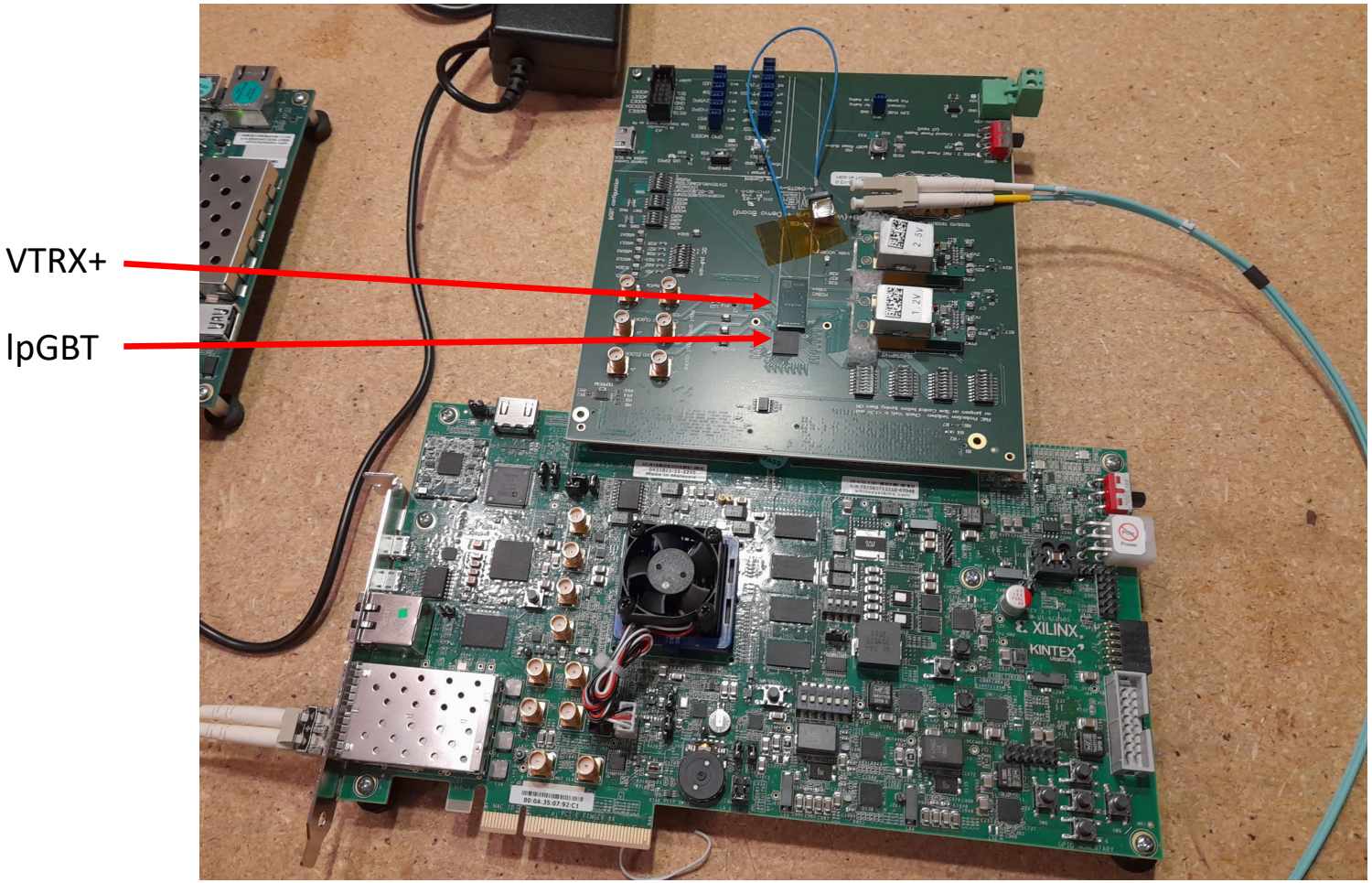
Starting point: The bord schematics/design is available to us from CERN.

We can remove quite a few of the test/diagnostic components and want to make the board smaller for the ring 5 detectors, while incorporating 4 lpGBTs rather than 1.

Development is ongoing:

We have access to an engineer at Carleton Univ. through the Canadian SAP Major Resources Support network

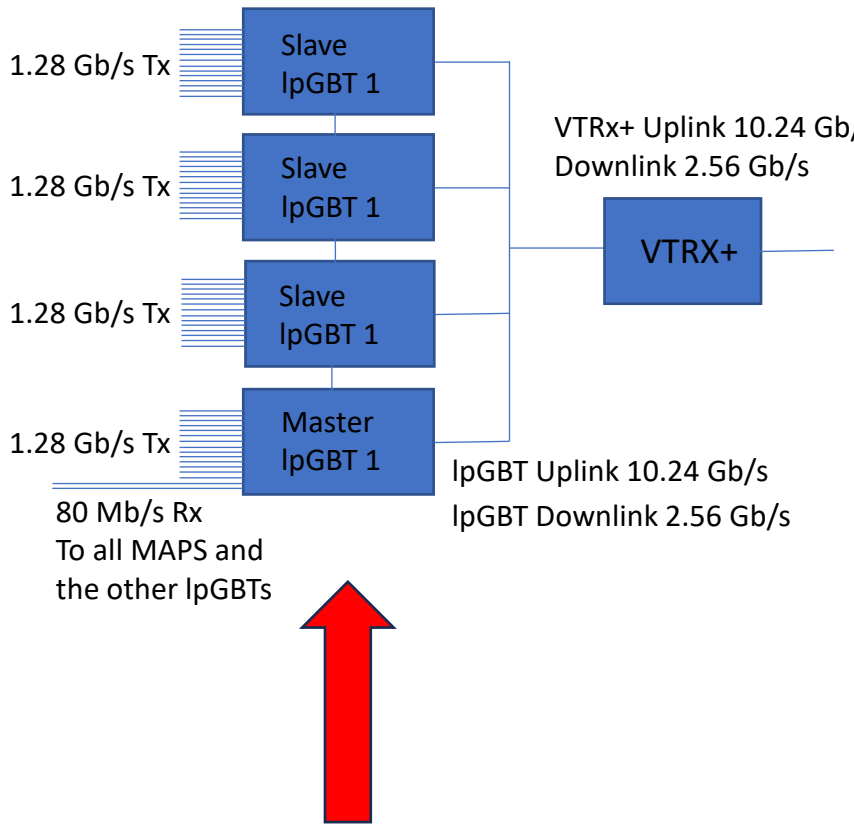
To be mostly completed by end of June



Readout Setup:

- We want 3 lpGBTs in slave mode and 1 lpGBT as master
- Slow-Control the lpGBTs via the of the down/uplink data stream from the back-end FPGA . This field allows to read and write the internal registers if the chip operates as a Transceiver (master).
- The VTRX+ has 4 uplinks (10.24 Gb/s) and one downlink (2.56 Gb/s) so we can read out
- Need to determine if we need the FEASTMP DC/DC converters or can run via remote power control
- We can use the Samtec ASP-134486-01 FMC connector (female)
- Maximum board width 100 mm
- Maximum board length 200 mm
- Mounting holes can be relocated within the lower 50 mm of the board.

- **Maximum hit readout rate per chip presently at ~90 Mhits / per second**

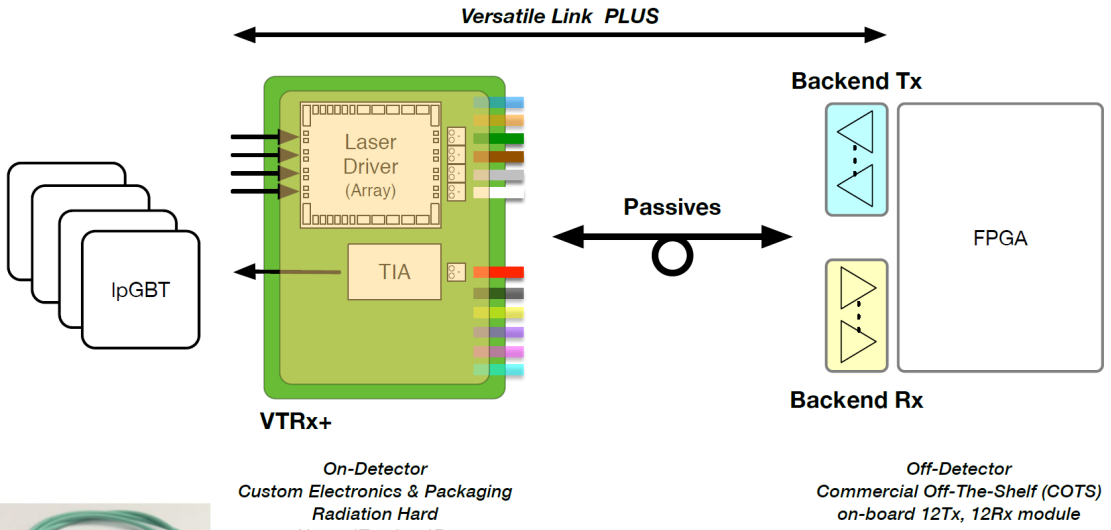


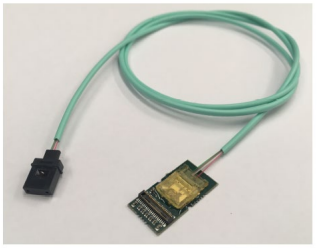
Present design for the readout board at the layout stage.

Back-end DAQ:

- Need an array of commercial FPGA boards like the Xilinx kcu105
- Or something like the Arista 48/96 LS fiber switch

From VTRX+ CERN Manual





Hardware

Description		Price	Qty	Ext. Price
DCS-7130-48LS-F	**Arista 7130 Series 48L with UltraScale VU7P-2 FPGA, front-to-rear air, 2xAC v2**	$31,027.07	1	$31,027.07
SVC-7130-48LS-1M-NB	**1-Month A-Care Software & NBD Hardware Replacement/Same Day Ship for 7130-48LS**	$294.55	60	$17,673.00
DCS-7130-96LS-F	**Arista 7130 Series 96L with UltraScale VU7P-2 FPGA, front-to-rear air, 2xAC v2**	$51,041.78	1	$51,041.78
SVC-7130-96LS-1M-NB	**1-Month A-Care Software & NBD Hardware Replacement/Same Day Ship for 7130-96LS**	$483.06	60	$28,983.60
SFP-10G-SR-P	**Arista 10GBASE-SR SFP+ (Short Reach)**	$74.80	48	$3,590.40
TARIFF FEE	**Logistics Fee**	$8,258.66	1	$8,258.66
FREIGHT.	**Shipping & Handling**	**$150.00**	**1**	**$150.00**
			Subtotal:	**$140,724.51**

Quote Summary	Amount
Hardware	$140,724.51
Subtotal:	**$140,724.51**
Estimated GST:	**$7,036.22**
Estimated PST:	**$9,850.71**
Total:	**$157,611.44**

Main detector low voltage cables and power supplies

2. HVMAPS

- 84 modules with 28 chips per module. Need three different LV connections for each module ($2V, 1.2V, 2.5V$) and one "HV" connection ($\lesssim 100\ V$) for bias
- LV powers the chip itself and the readout electronics

Per Module:

- Chip supply voltage: $V_{chip} = 2V\ @\ 0.5A\ \times\ 28$ (parallel)
- Readout lpGBT: $V_{lpBGT} = 1.2V\ @\ 0.27A \times 4$
- Readout VTRX+: $V_{VTRX} =\ 1.2V\ @\ 0.045A + 2.5V\ @\ 0.080A$
- Bias: $V_{bias} =\ 100V\ @\ 0.02A$
- Largest power: $P_{chips} \simeq 34\ W$ (includes ~20% safety factor)
- Total power: $P_{tot} \simeq 38\ W$ (includes ~20% safety factor)

Cables:

- Voltage drops:
  - Flexprint to R5 readout: $\Delta V \sim 0.15V\ @\ 3.5\ A$
  - R5 readout to segment patch panel: $\Delta V \sim 0.16V\ @\ 3.5\ A$ AWG 18 (VDD + GND = 24 cables/segment)
  - Segment patch panel to GEM hut: $\Delta V \sim 0.56V\ @\ 1.75\ A$ AWG 15 (Split VDD and GND into two AWG 15 = 48 cables)
  - GEM hut floor to PS unit: $\Delta V \sim 0.12V\ @\ ?\ A$ AWG ? (Depends on PS unit we choose)
  - Total: $\Delta V \leq 1V$ (Depending on PS unit we chose)

Main detector low voltage cables and power supplies

2. HVMAPS

PSU Series

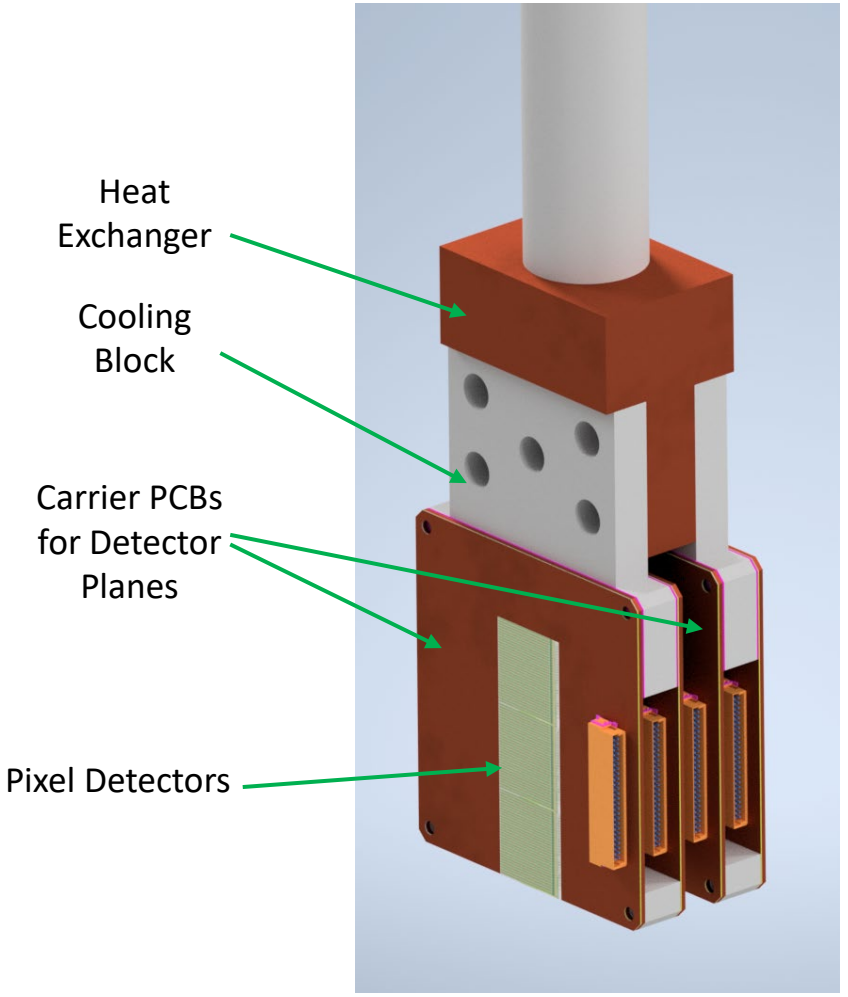
- Single channel high current

SPECIFICATIONS	
MODEL	PSU 6-200
OUTPUT RATINGS	
Rated Output Voltage (*1)	6V
Rated Output Current (*2)	200A
Rated Output Power	1200W
RIPPLE AND NOISE(*5)	
CVp-p(10 ~ 20MHz) p-p (*6)	60mV
CVrms(5Hz ~ 1MHz) r.m.s. (*7)	8mV
CCrms(5Hz ~ 1MHz) r.m.s.(*12)	400mA
LOAD REGULATION	
Voltage(*4)	2.6mV
Current(*11)	45mA
LINE REGULATION	
Voltage(*3)	2.6mV
Current(*3)	22mA

Recent work updates and status:

- Compton e-Detector design for in-vacuum operation:
  - 4 pixel detector planes
  - HVMAP pixel detectors
  - 3 $2 \times 2\ cm^2$ chips per plane (TBD based on profile)
  - $80 \times 80\ \mu m$ pixels
  - Original chip design based on ATLASPix & MuPix (designed at KIT, Heidelberg, Mainz)
  - Specific modifications for probably required for ChiralBelle (faster chip/readout)

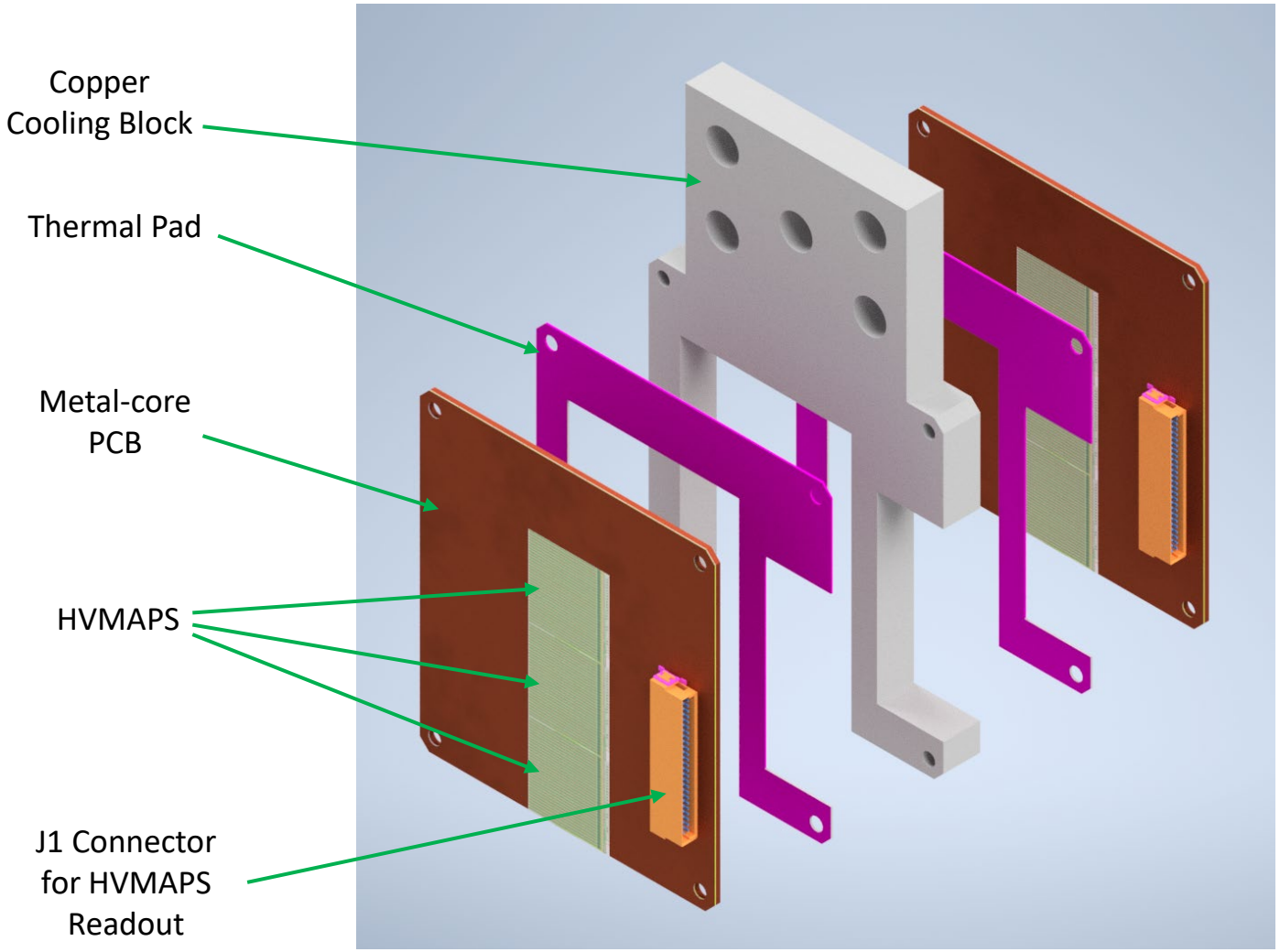
Mounting and cooling structure design:
Nafis Niloy and Kristofer Isaac



New HVMAPS detector planes

Recent work updates and status:

- Compton e-Detector design for in-vacuum operation :
  - Each detector plane consists of 3 HVMAPS wire-bonded to a metal-core PCB
  - Two planes will be attached to one cooling block, interfaced together using thermal pads
  - Cooling block will be a single piece of machined copper (different color used in figure for ease of visibility)

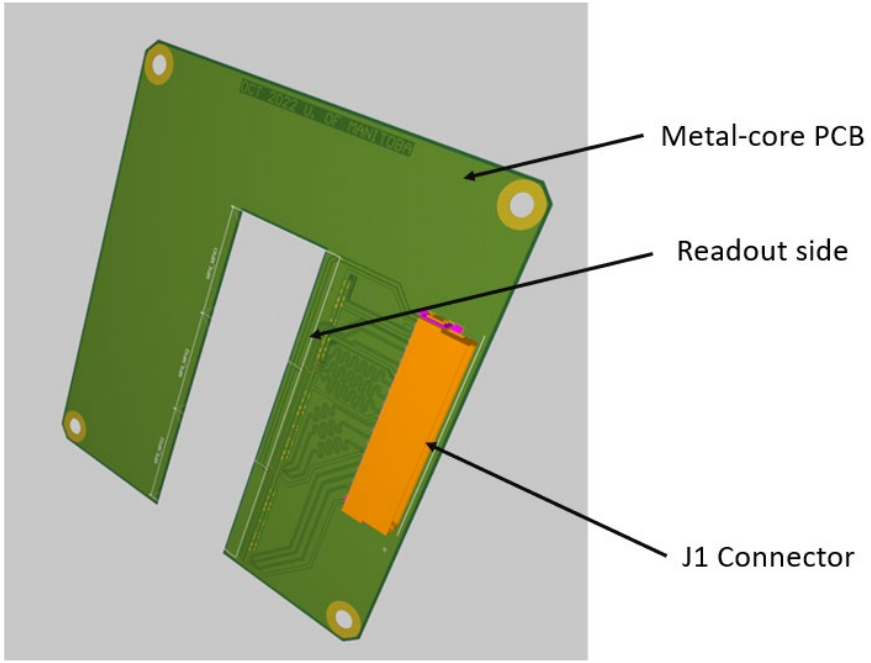


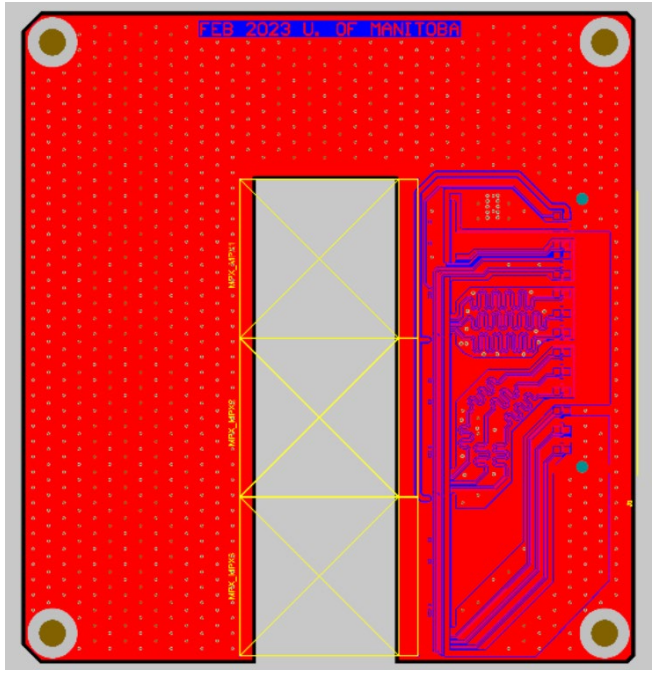
Recent work updates and status:

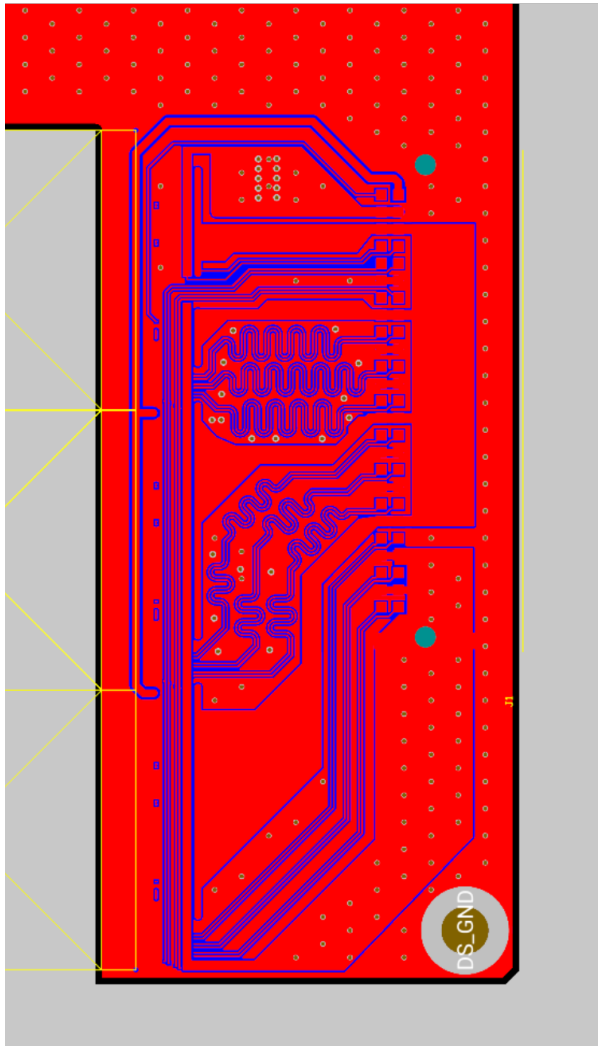
- Compton e-Detector design for in-vacuum operation :

PCB and readout design: Jie Pan

- HVMAPS will be glued and wire-bonded to a PCB
- Metal-core PCB will help conduct heat produced by the HVMAPS away for dissipation
- Using thermal pads to improve thermal conduction between metal-core PCB and HVMAPS







Recent work updates and status:

- Compton e-Detector design for in-vacuum operation :

- A prototype of the Compton heat exchanger was designed and machined out of copper
- Rather than manufacturing the custom copper feedthrough cylinder planned for the final design, the prototype model utilizes separate chilled water lines fitted to the heat exchanger with compression fittings to reduce prototype costs and leverage existing vacuum infrastructure
- Next steps for prototype:
  - Pre-test seal of prototype heat exchanger using pneumatic pressure-differential test
  - Fully assemble Compton prototype heat exchanger, including chilled water lines
  - Assemble Compton test planes onto heat blocks

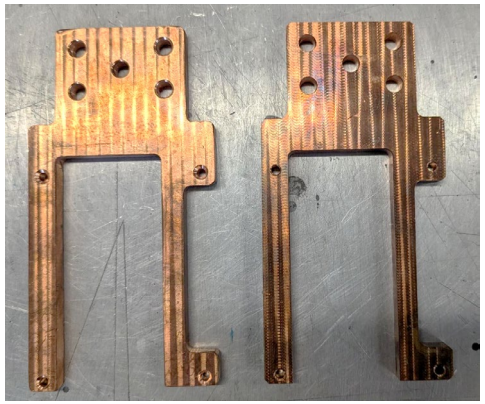


Fig. Prototype heat blocks

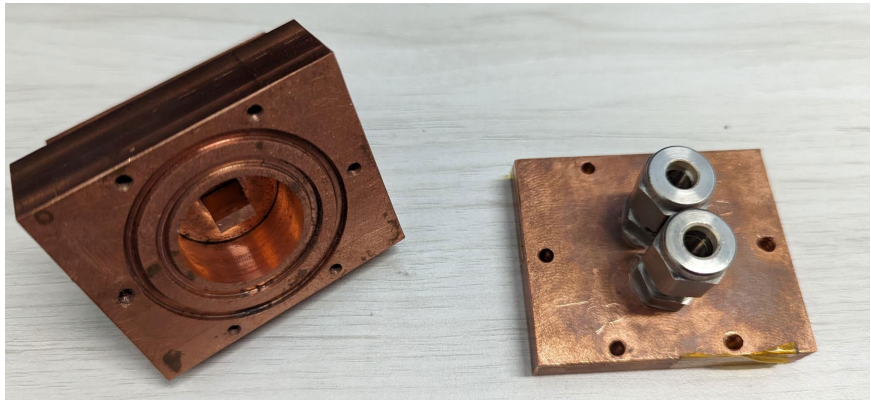


Fig. Prototype heat exchanger, featuring double o-ring grooves and turbulence-generator tab

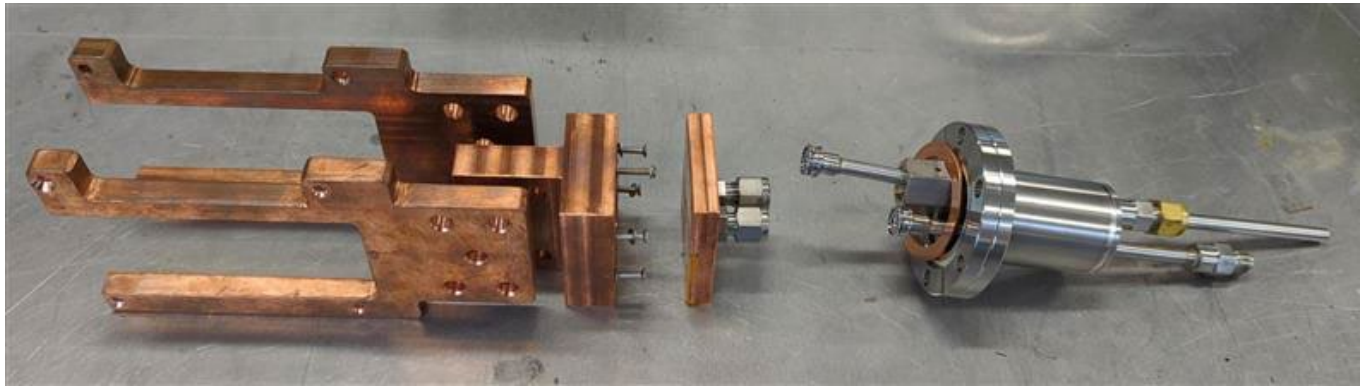
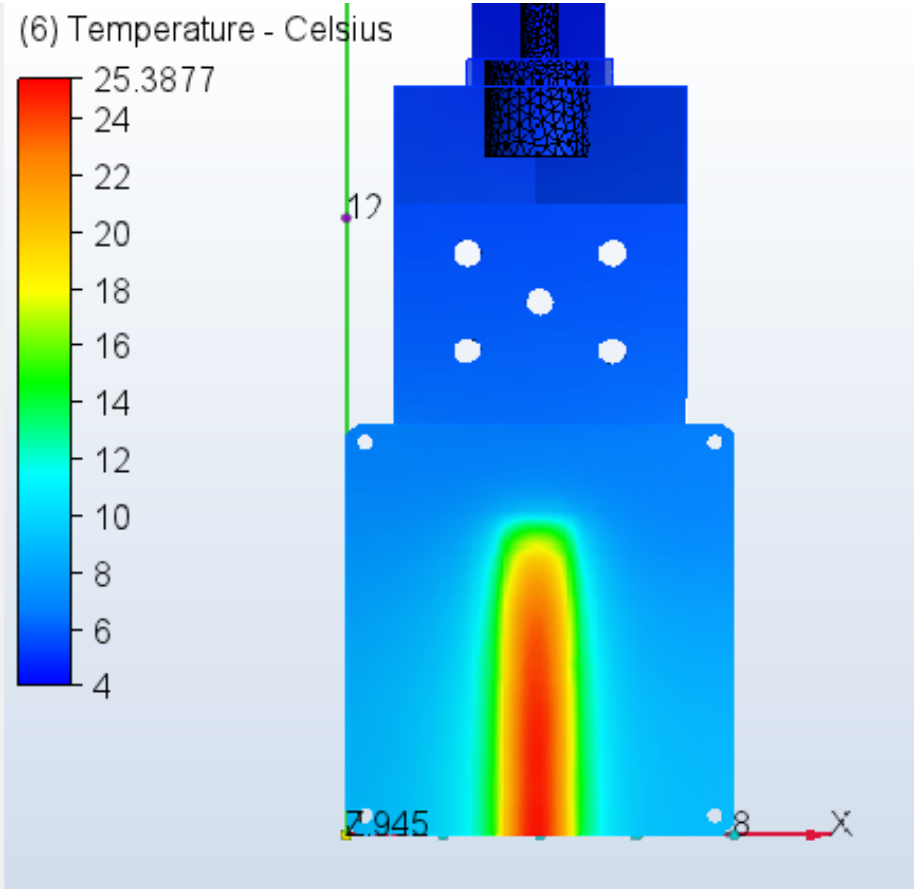


Fig. Rough layout of heat exchanger prototype, including chilled water feed-through flange

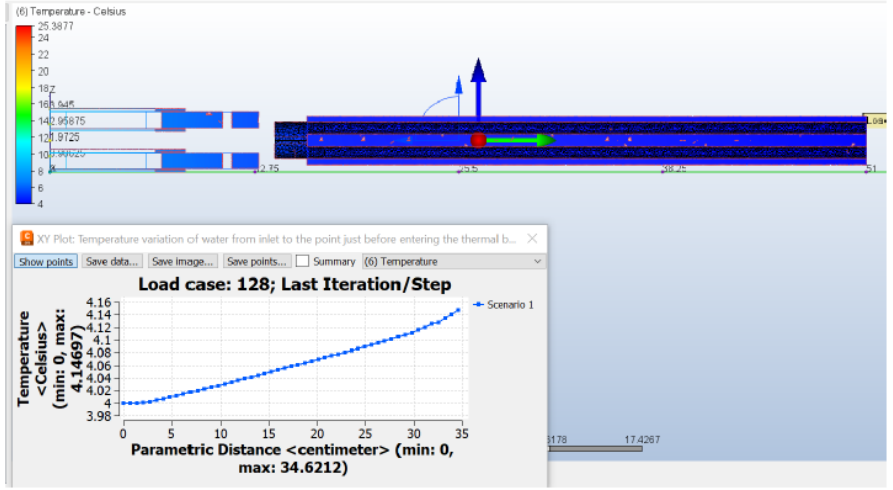
Recent work updates and status:

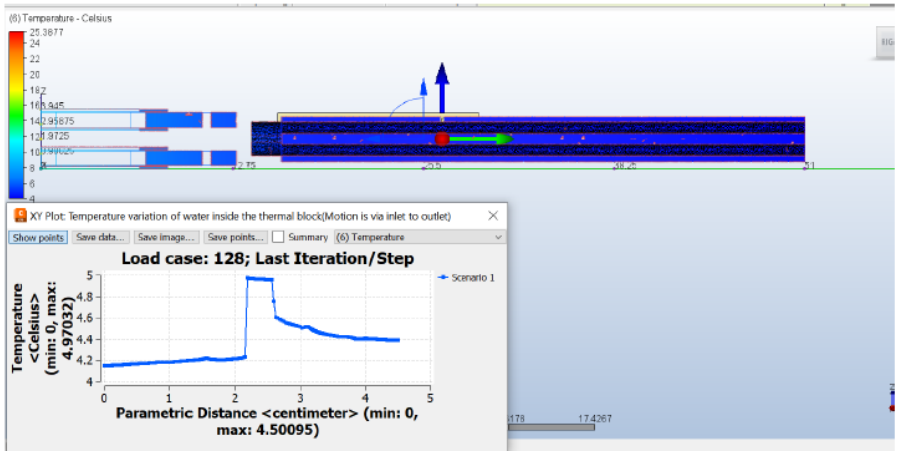
Thermal simulations and measurement setup: Shefali Prabhakar

- Cooling studies:



Temperature distribution of overall assembly





Temperature variation of coolant inside the heat exchanger

Recent work updates and status:

Thermal simulations and measurement setup: Shefali Prabhakar

- Cooling studies:

  - The aim of this setup is to test cooling capabilities in vacuum
  - Currently using dummy (heater) chips
  - Goal is to verify modeled cooling performance with measured temperature gradients at various positions
  - Thermal simulations of the same model as shown below.

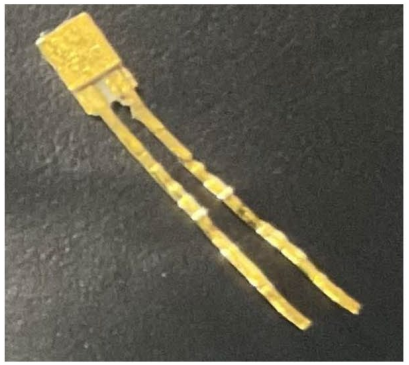


Fig.b

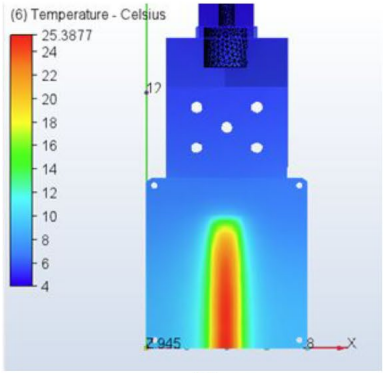
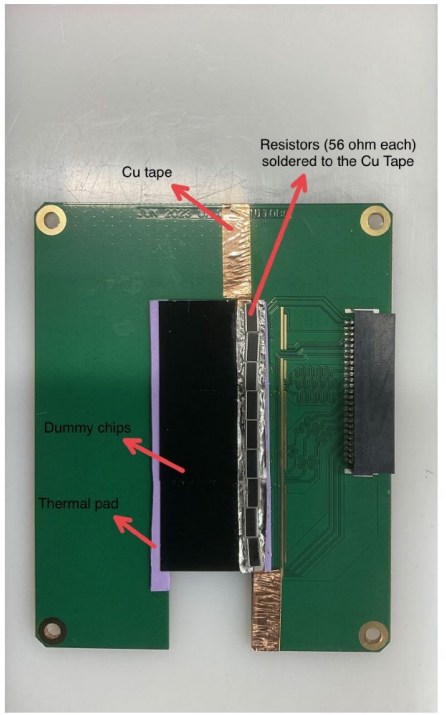
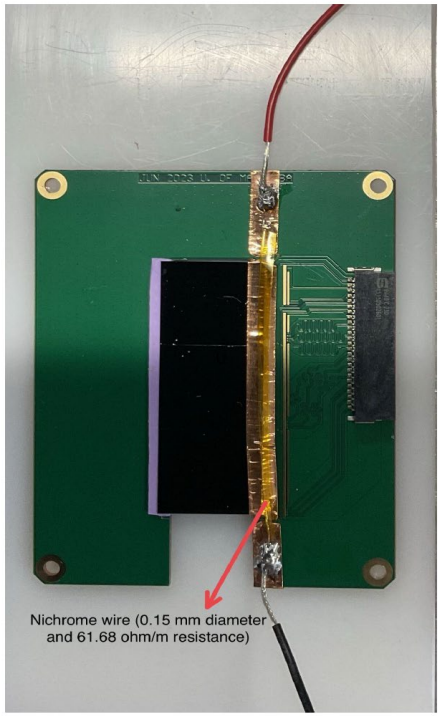


Fig.c



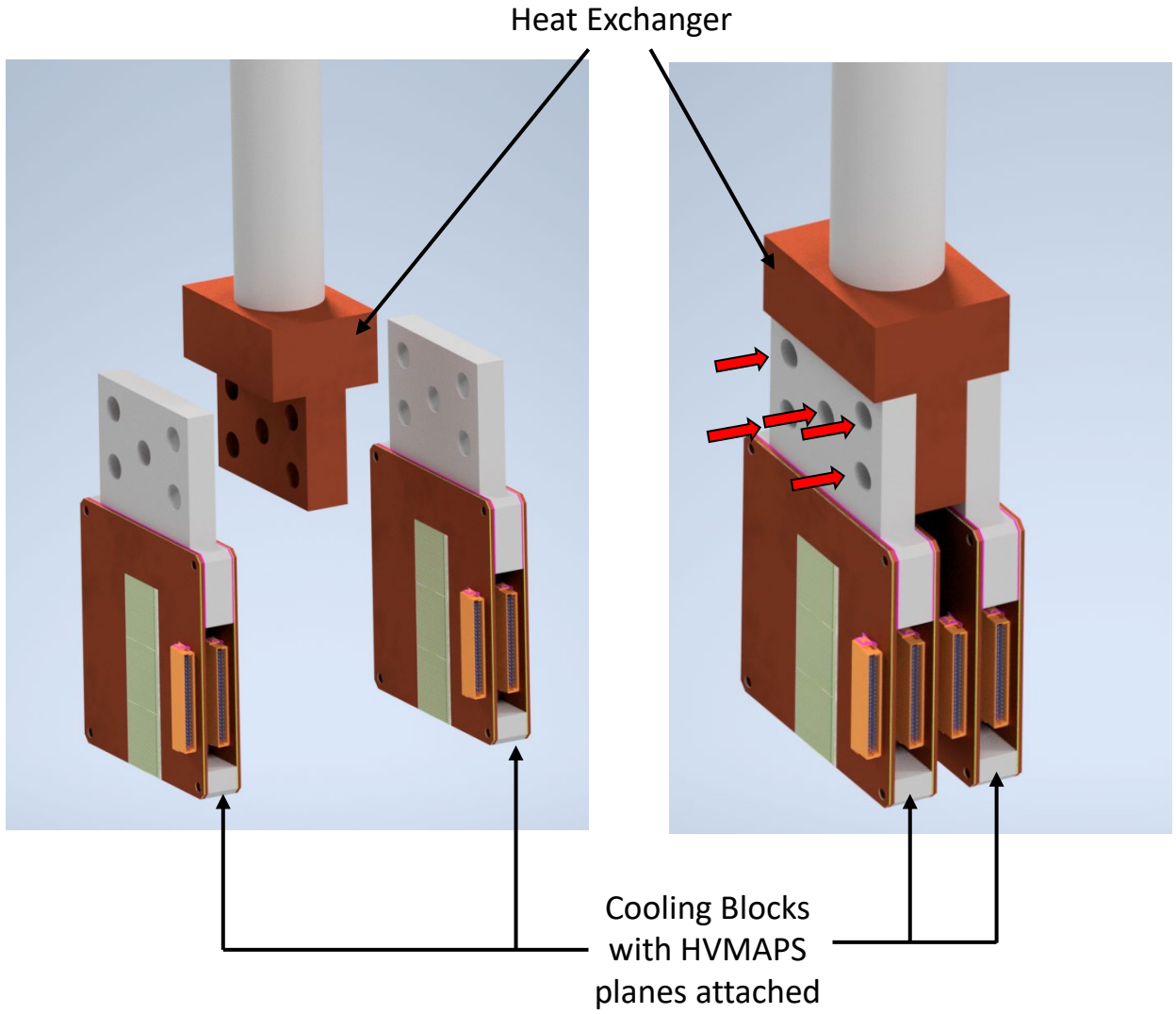
A.) Combination of resistors as a heating element.

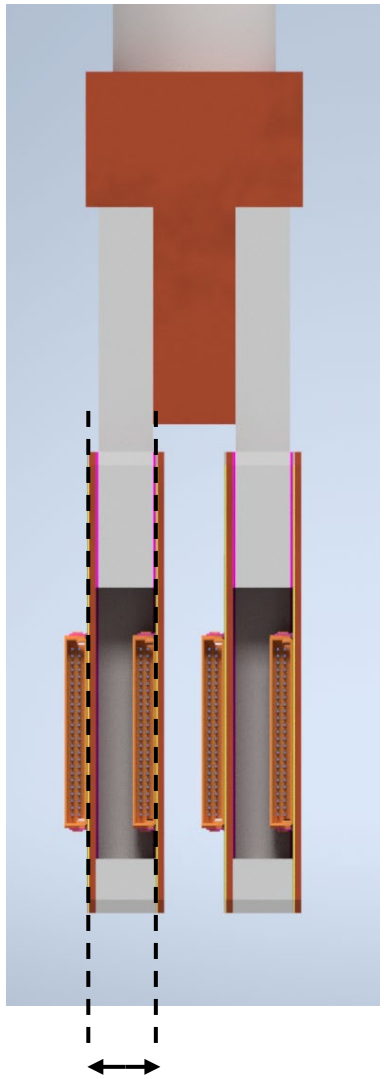


B.) Nichrome wire as a heating element

Recent work updates and status:

- Cooling studies:

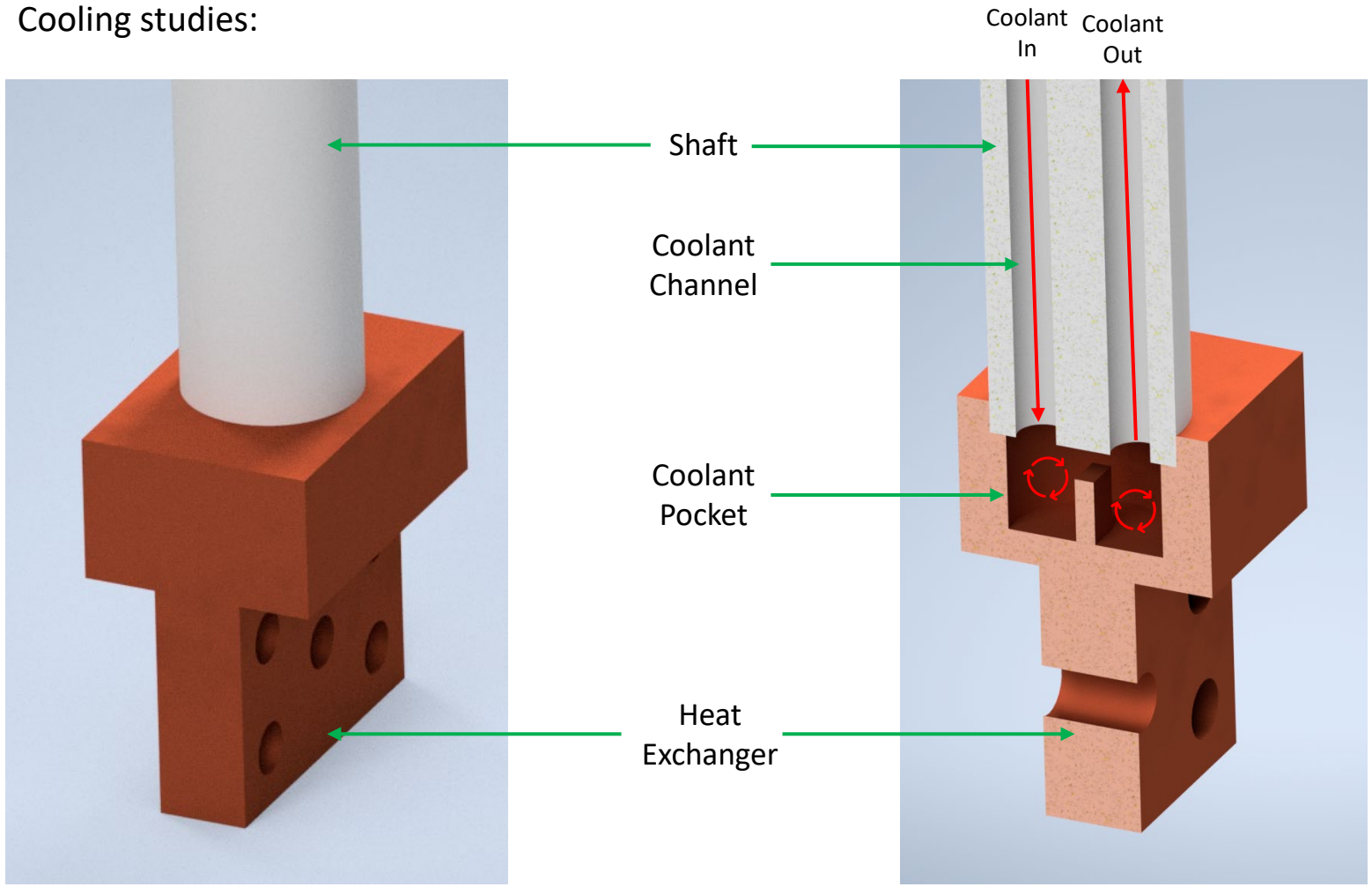




- Both cooling blocks will be attached to either side of the copper heat exchanger using 5 fasteners (red arrows)
- Applies a clamping pressure of 4000 psi between mating heat-exchanger components
- Maximizes conduction between components
- Heat exchanger will be machined out of a single block of copper
- Distance between two adjacent HVMAPS planes is 12.6 mm

Recent work updates and status:

- Cooling studies:



- Shaft holding the assembly in beam line will be attached to a linear translation stage to move detector planes up and down
- Translation stage attached via a feed-through
- Shaft will be a copper rod with coolant channels bored along its length
- Will be using LCW (Low Conductive Water) as coolant
- Pocket is designed to make the flow of coolant turbulent, thereby increasing heat transfer to coolant
- Shaft and heat exchanger will be brazed to prevent possible leaks

Chip Development Status:

- The most recent version of the chip as described in this document was produced by TSI
- TSI was taken over by Bosch in September and the foundry will be shut down at the end of 2023 – no further production of these types of chips will take place through TSI/Bosch after that – we have enough to build the Hall A Compton detectors but not for any future development
- There is presently a community wide search for alternatives
- We have identified AMS as a suitable alternative – with some design changes
    - Intermediate design changes in the short run to be submitted for an engineering run in April, with evaluation in the Summer months
    - Possible production run in the Fall
    - Additional design changes and engineering runs possible in 2025 - …
        - For Chiral Belle: Making the chip faster (?)
        - Higher resolution (?)
        - …

Questions / unresolved issues:

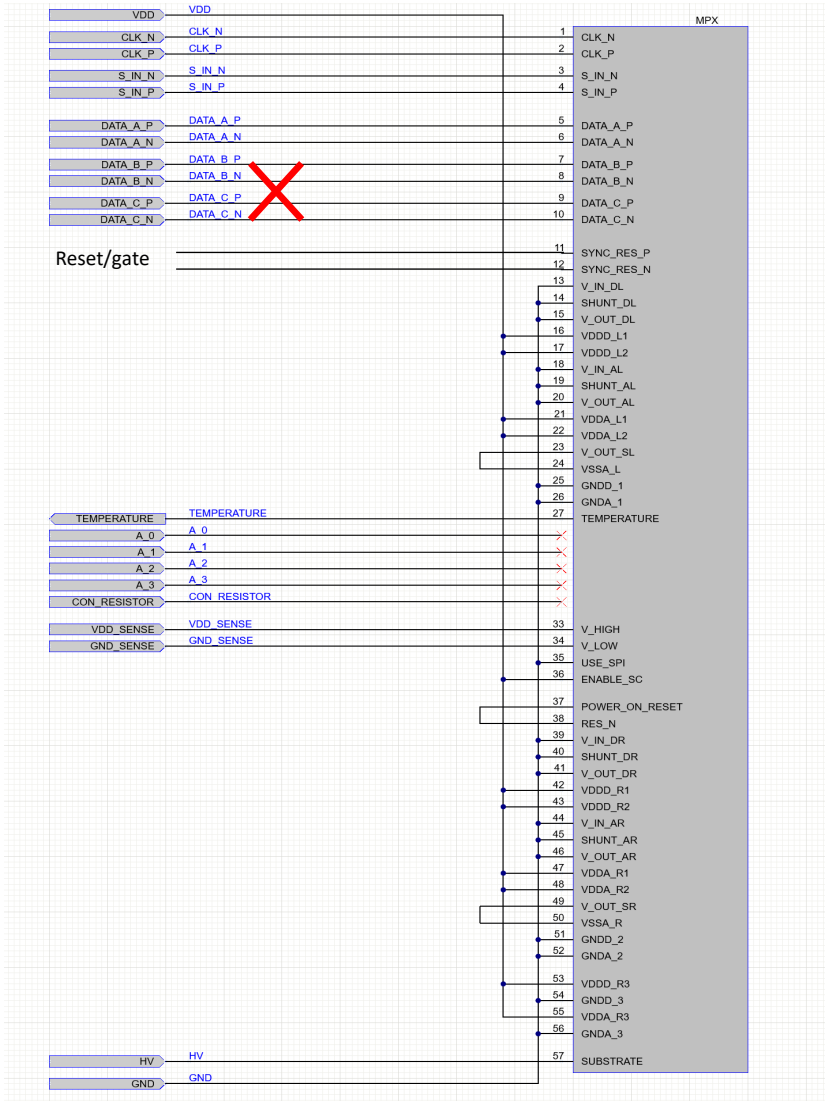
- Are these detectors suitable ?
  - Too slow, resolution too low, …
- Establish detector position
- How many positions/detectors
- Continue simulations (money available through the NSERC operating grant – Wouter will look for student for next year)
- DAQ and system interface and requirements
- Floor plans / where can we put how much stuff

Backups

Readout Setup:

Chip-to-flexprint connections:

- Single LVDS pair readout per chip at ~180 Mbps
- 7 chips ~ 1.28 Gbps
- 14 lines per chip through flexprint and ribbon
- Clk_P/N from lpGBT
- S_In_P/N chip addressing through lpGBT slow control
- SYNC_RES_P/N chip gating (or similar) also through lpGBT
- Rest of the lines are voltage distribution



Summary of HV-MAPS operation

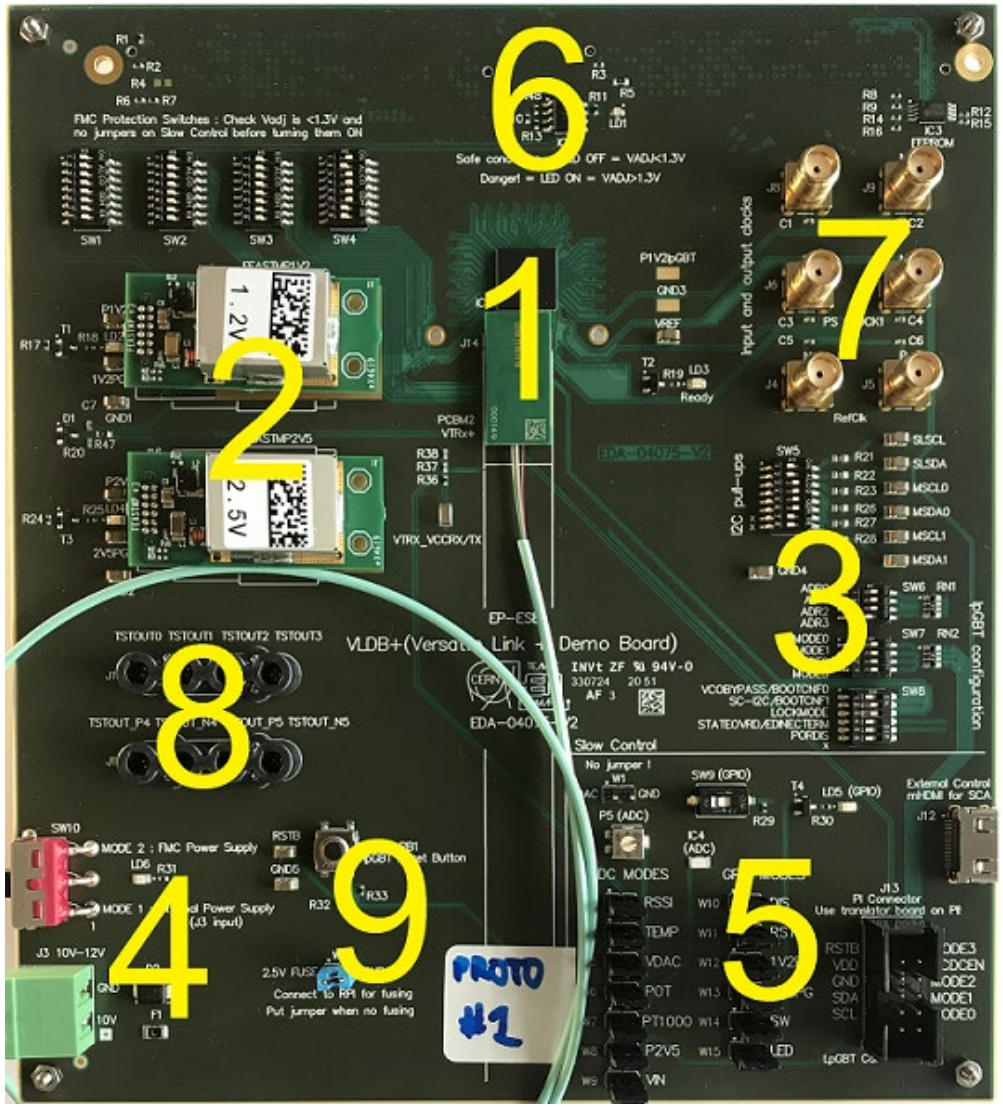
- Chip connections:

1. There will be 4 differential outputs (8 lines) per chip that are connected to the lpGBT:
    1. Clock (Clk_n/p)
    2. Data-out (DOut_n/p)
    3. Gate_n/p
    4. Addressing (Sin_n/p)

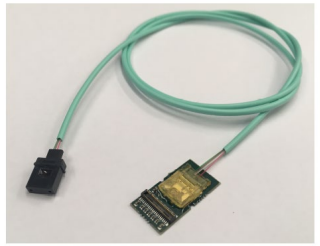
2. There could be one more digital temperature signal from each chip to the lpGBT input (TBD)
3. All signals except the temperature diode are LVDS
4. Target TX speed is 1.28 Gbps (~180 Mbps per chip to lpGBT)
5. Target RX speed is 80 Mbps (from lpGBT to chip)

VLDB:

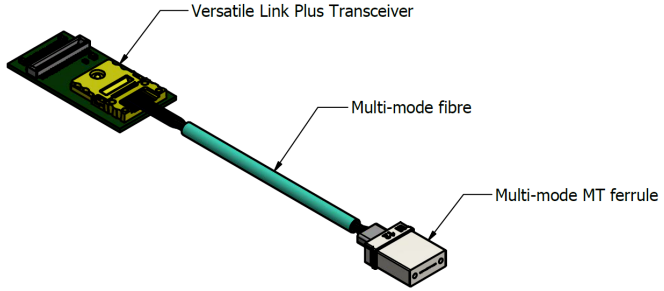
- Item 1: Core parts needed – 4 lpGBT, 1 VTRX+
- Item 2: FEASTMP may not be needed. Use remote power from PS unit (see slide 6) – need to implement a sense wire – maybe can use them though
- Item 3: Not needed - mode selection should take place via the downlink interface
- Item 4: Needs to be re-designed to supply power to the lpGBTs , the VTRX+, and to the HCMAPS chips
- Item 5: Not needed – startup configuration and operation mode need to be “hard wired” by pulling control pins high/low with resistors
- Item 6: Not needed
- Item 7: Not needed – reference clock should come through downlink, but the lower two connectors could be kept for benchtop testing/prototyping
- Item 8: Could be kept for prototype testing
- Item 9: Not needed but might be useful for testing



VTRX+ Info:



- Fiber optic transceiver
- 4 upstream channels (sum = 10.24 Gb/s)
- 1 downstream channel (2.56 Gb/s)
- 20 cm pigtail with female MT terminator
- Needs to have MT-MPO (male) adapter or other to connect to standard fiber



From VTRX+ CERN Manual