Introduction to the level1 trigger

2024/10/8

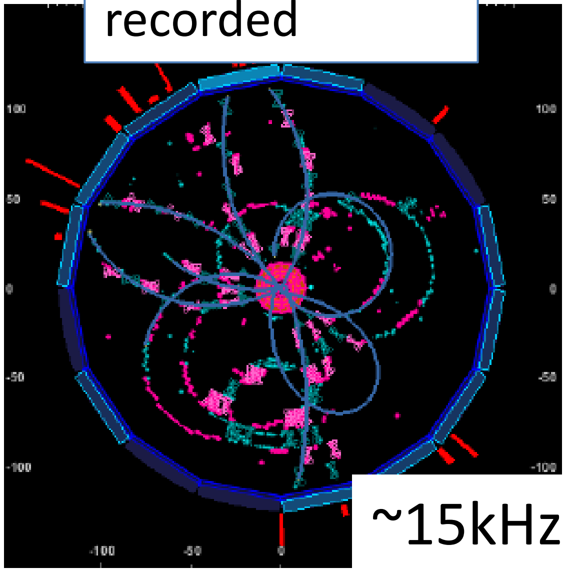
KEK Taichiro Koga

Trigger?

-"Trigger" in particle physics (wikipedia)

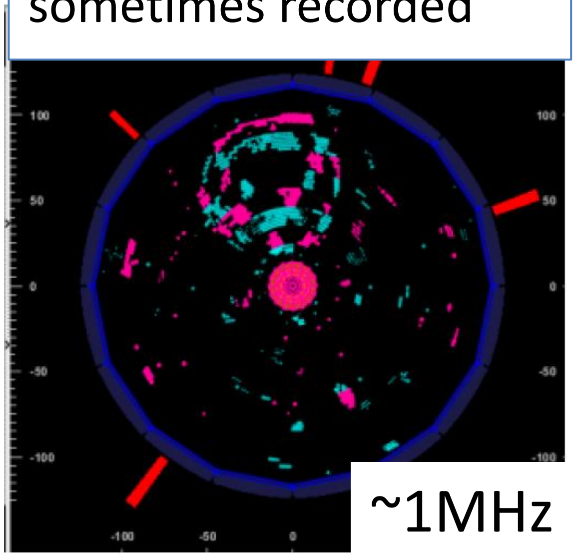
-a **trigger** is a system that uses criteria to rapidly decide which events in a particle detector to keep when only a small fraction of the total can be recorded.

physics signal recorded



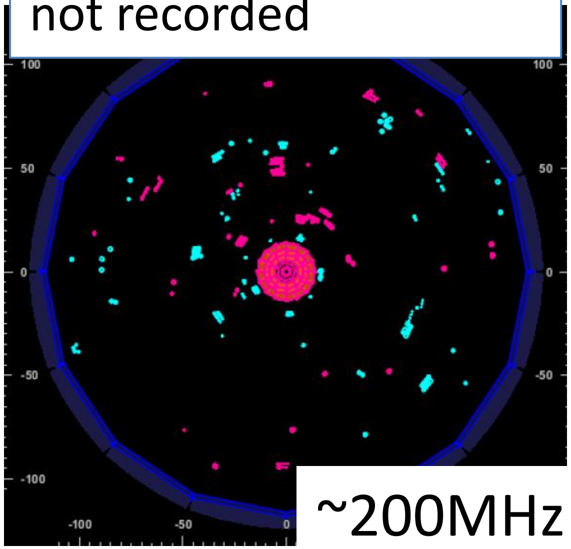
~15kHz

beam background sometimes recorded



~1MHz

collision w/o interaction not recorded



~200MHz

Example of cosmic trigger with scintillator

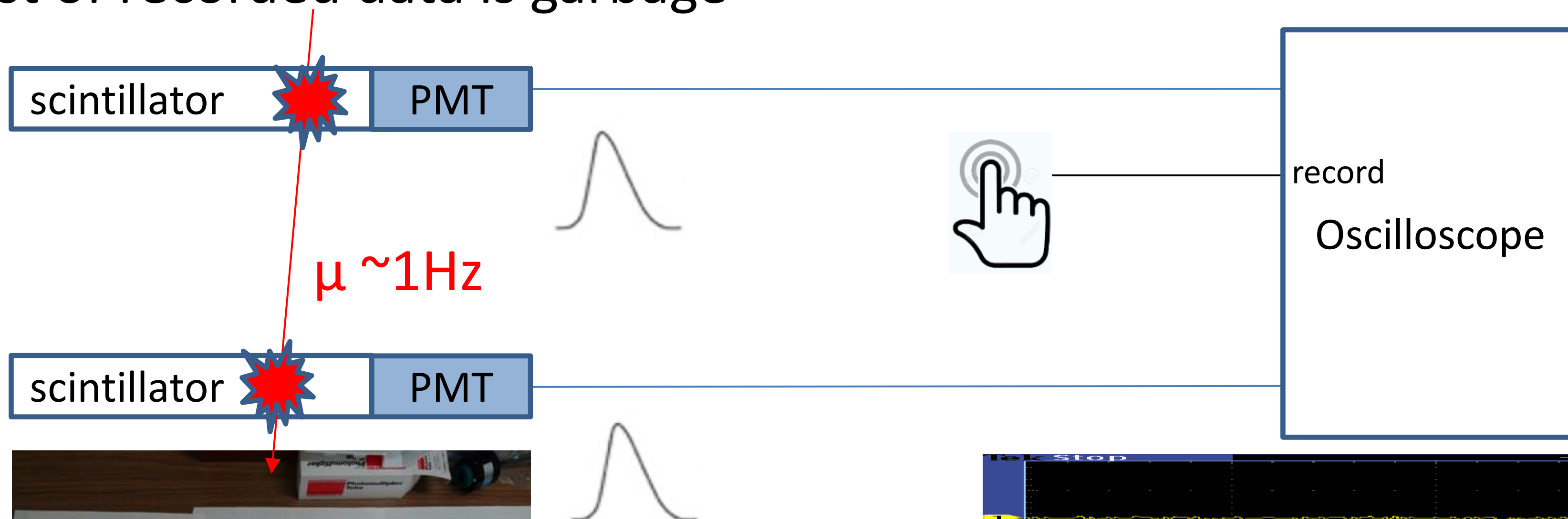
-Let's detect cosmic muon with two scintillators and an oscilloscope

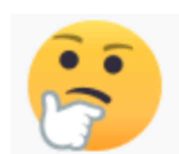
-If we record waveform by hand, we can not see cosmic due to low rate

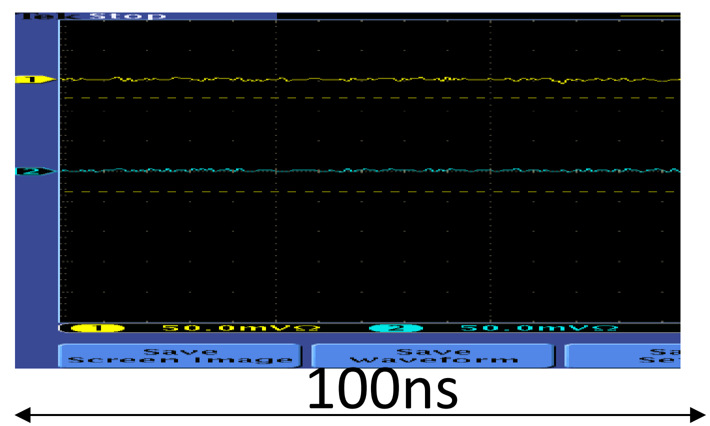
-Expected #cosmic signal per a record

= (oscilloscope timing window) × (cosmic rate) = ~100ns × ~1Hz= 10^{-7}

-Most of recorded data is garbage





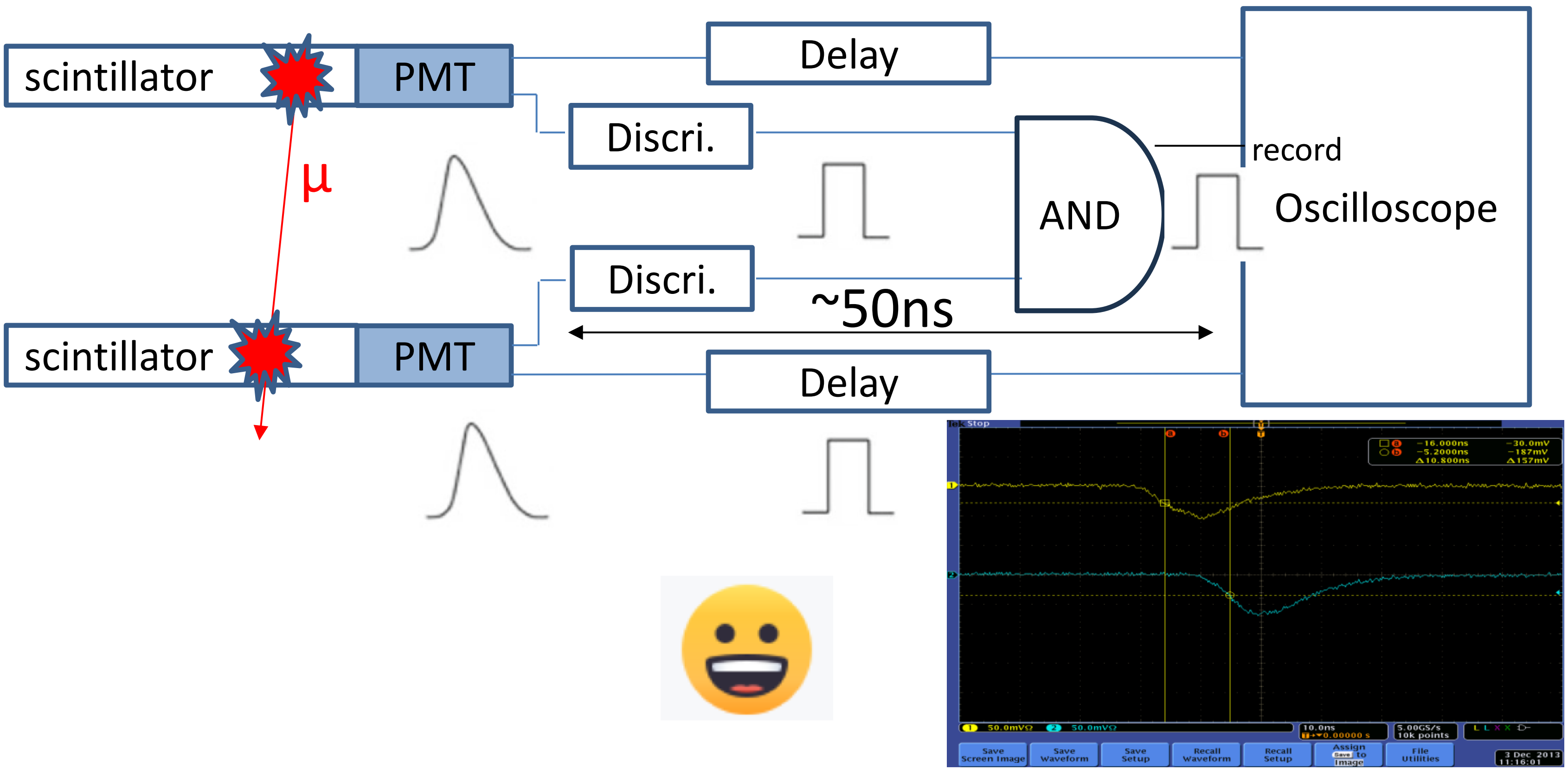


Example of cosmic trigger with scintillator

-Add cosmic trigger to take coincidence of two scintillator signals

- -Discriminator: convert analogue to digital
- -Coincidence: take AND of digital signals
- -Delay: delay analog signal for waiting coincidence

-Most of recorded data is cosmic

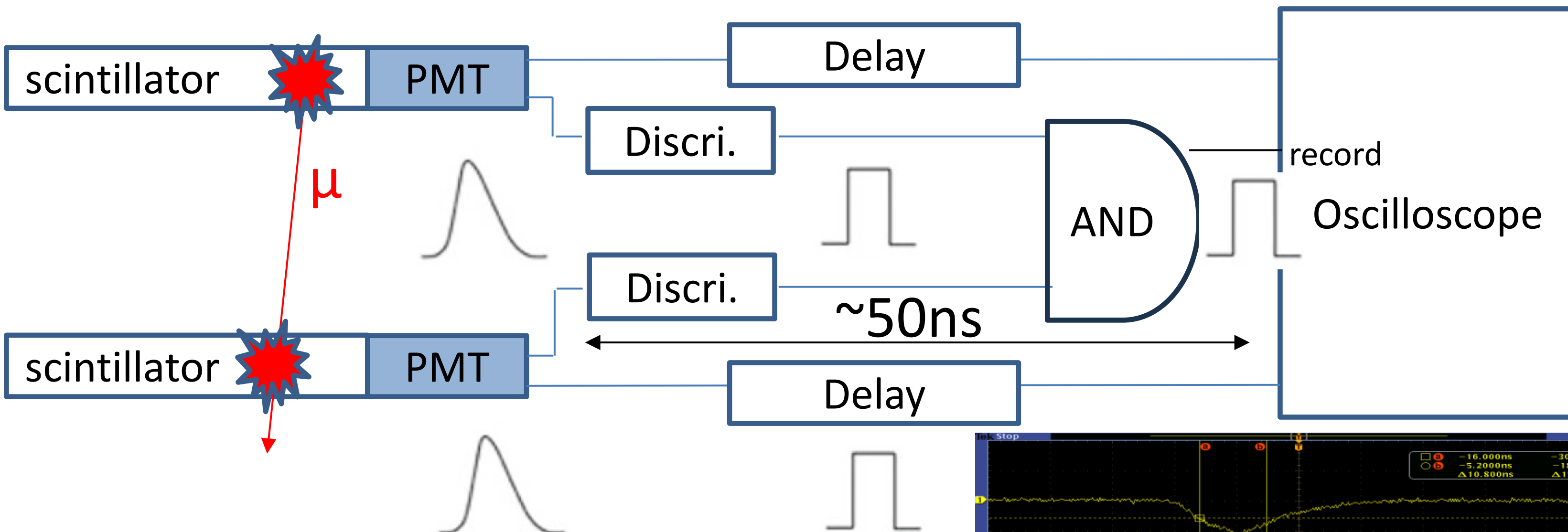


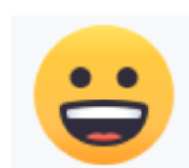
Example of cosmic trigger with scintillator

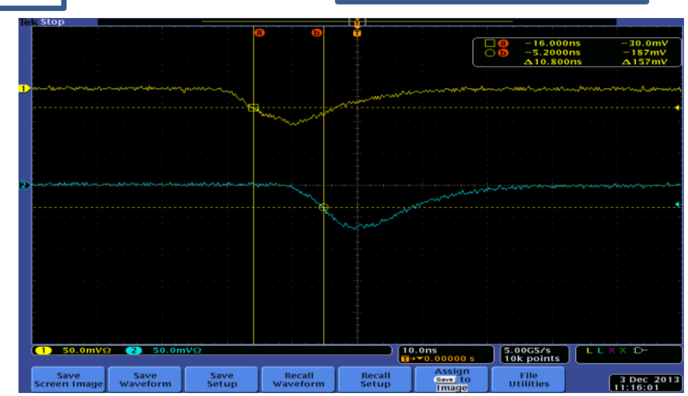
-Add cosmic trigger to take coincidence of two scintillator signals

- -Discriminator: convert analogue to digital ← ①Digital conversion
- -Coincidence: take AND of digital signals ← ②Digital calculation
- -Delay: delay analog signal for waiting coincidence ← ③Buffer

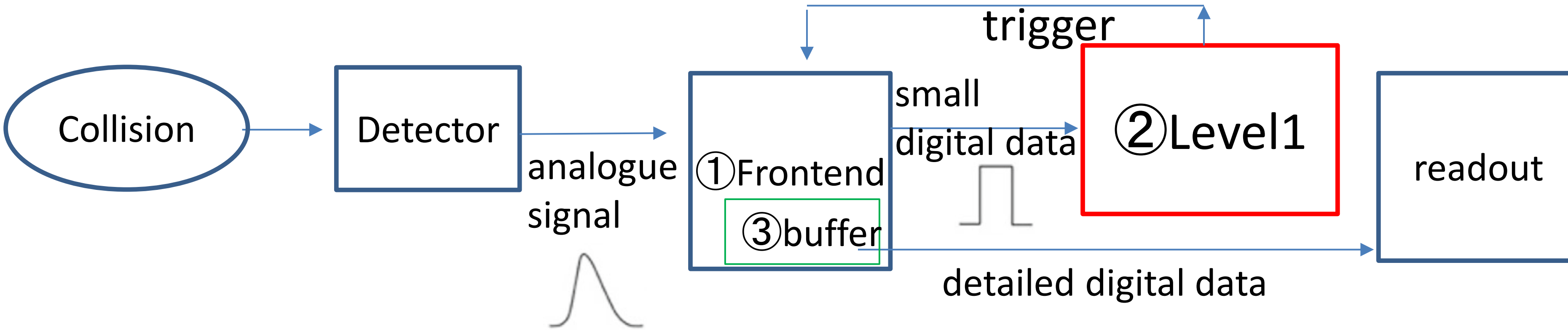
-Most of recorded data is cosmic ← event rate, data size reduction







Recent level1 trigger system



-Basic concept is the same as cosmic example:

-①Digital conversion on detector front end boards

-②Digital calculation on Trigger boards

-③Buffer on detector front end board to wait a few μs until trigger comes

limited by buffer size

-To provide trigger within a few μs latency, FPGA is used for ②

FPGA

-"Field Programmable Gate Arrays"(FPGA): programmable integrated circuits

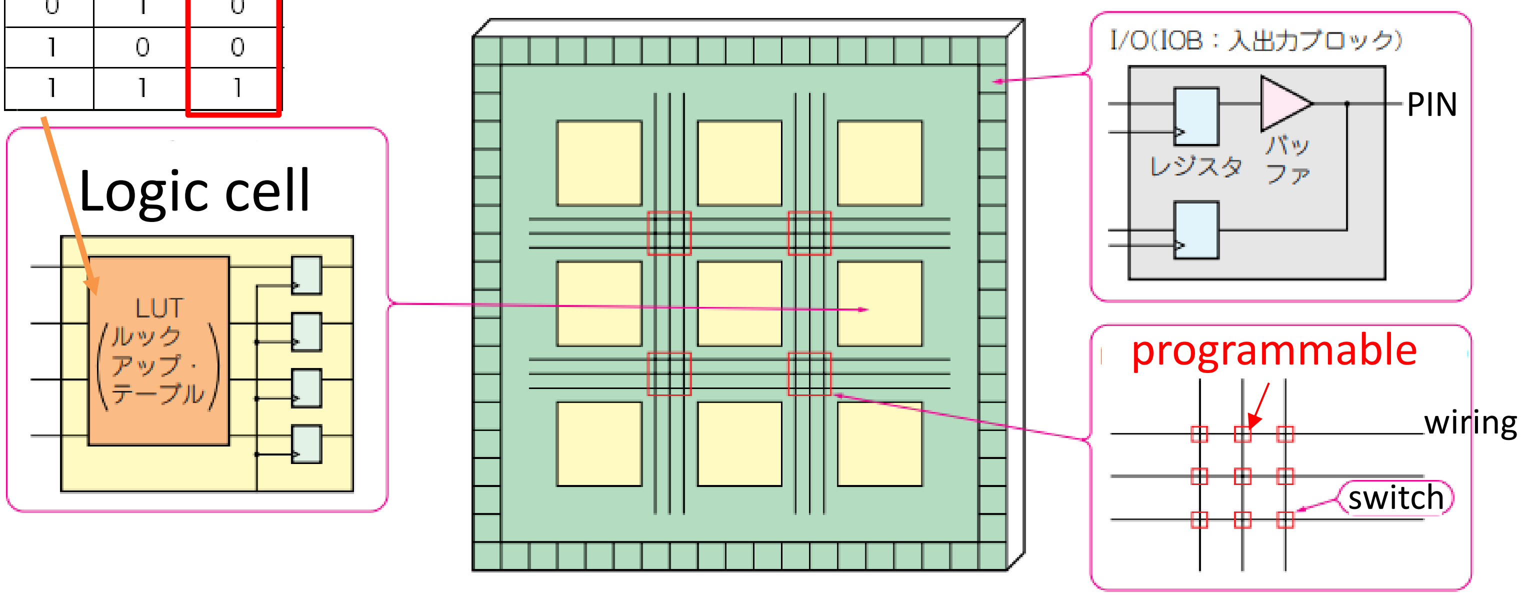
-I/O: PIN for input and output

-Logic cell: combination of LUT(combination circuit) and Flip flop(synchronous circuit)

-Internal writing: connect Logic cell, IO

IN A	IN B	OUT
0	0	0
0	1	0
1	0	0
1	1	1

programmable

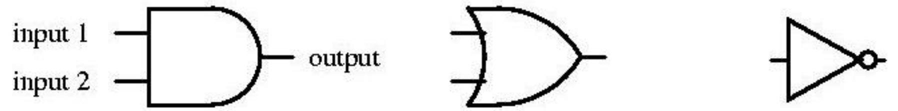


トラ技

Digital calculation on FPGA

-"Field Programmable Gate Arrays"(FPGA): programmable integrated circuits

-combinational circuit:
take AND, OR, NOT etc.



AND

IN1	IN2	OUT
0	0	0
0	1	0
1	0	0
1	1	1

OR

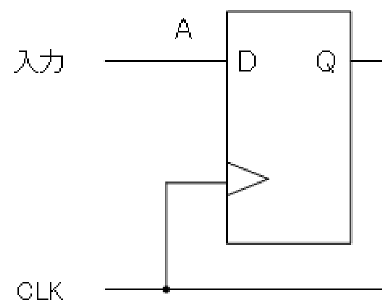
IN1	IN2	OUT
0	0	0
0	1	1
1	0	0
1	1	1

NOT

IN1	OUT
0	1
1	0

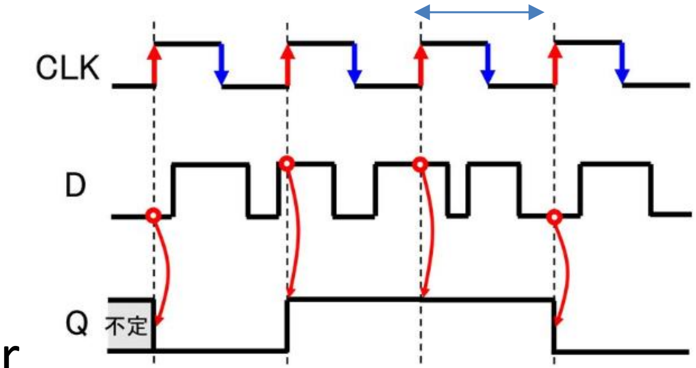
Look up table (LUT)

-synchronous circuit:
store output of
combinational circuit etc.



D-Flip flop register

127MHz etc.



-Any combinations of above circuits can be implemented on FPGA.

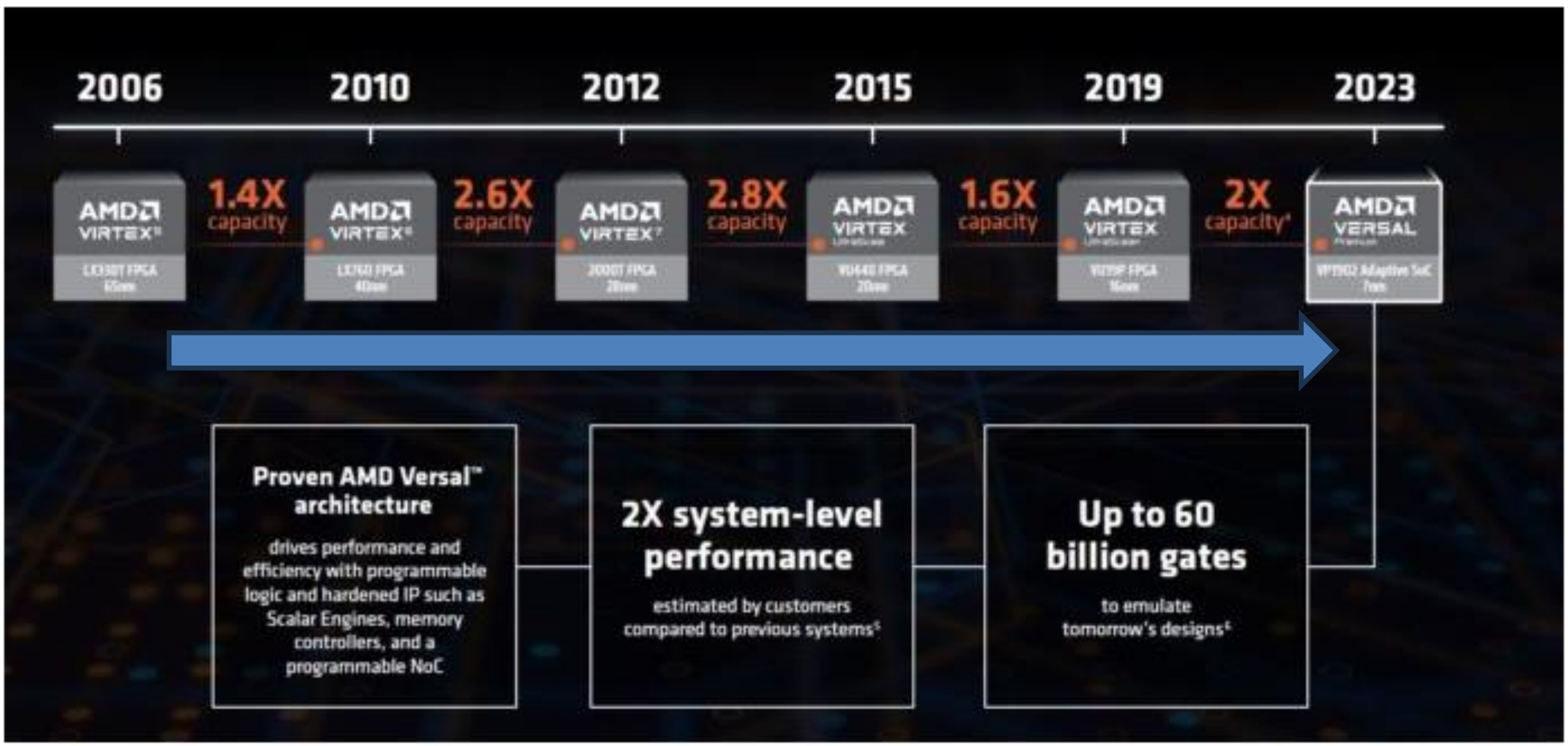
-The number of available circuit is limited by size of FPGA and latency

worse accuracy than software in general. major challenge.

FPGA technology

-FPGA performance has been improved in recent ~20years commercially
 -~2times circuit size (logic cell) in each 3~4 years !!

-Trigger performance has been improved and accordingly
 -advanced, complex algorithm with large resource



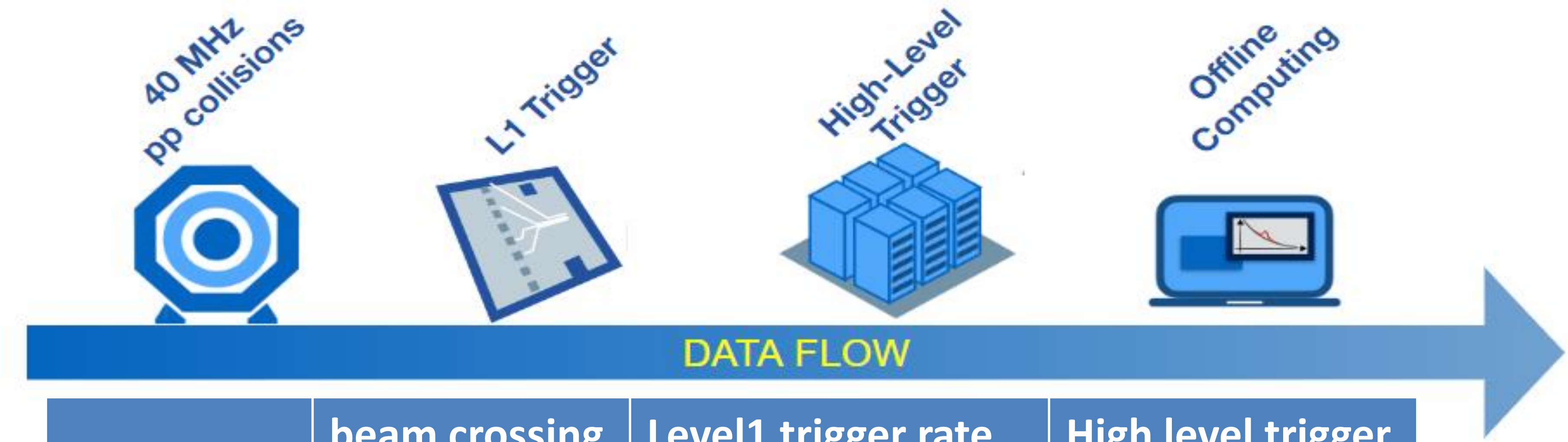
AMD Xilinx Emulation Virtex And Versal Lines For 17 Years

Trigger in various experiments: collider

-Level1(0) Trigger: Hardware (electric circuit)

-High-level Trigger: Software (computer) ATLAS workshop

-No level1 (Streaming DAQ) is modern movement, but not covered in this talk



	beam crossing rate	Level1 trigger rate (FPGA)	High level trigger rate (CPU/GPU)
ATLAS	40MHz	100kHz	1kHz
LHCb	40MHz	1MHz	12.5kHz, 0.6GB/s
LHCb upgrade	30MHz	no Level1 !	2-5 GB/s
Belle II	250MHz	30kHz	5~10kHz, 1.8GB/s

Belle II level1 trigger

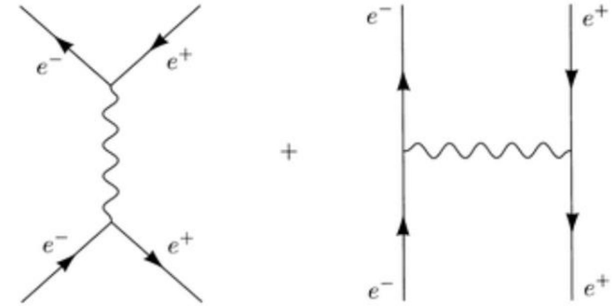
Event rate at Belle II

-Expected event rate at target luminosity

Process	Event rate
e^+e^- bunch collision	~200MHz
Beam background	>~300kHz (2022)
Bhabha scattering ($e^+e^- \rightarrow e^+e^-$)	>~50kHz
Two photon ($e^+e^- \rightarrow e^+e^-e^+e^-$ etc.)	~10kHz
$e^+e^- \rightarrow \gamma\gamma$	~2kHz
Continuum ($e^+e^- \rightarrow$ uubar,...)	~2kHz
$e^+e^- \rightarrow \Upsilon(4S)$	~1kHz
$e^+e^- \rightarrow \mu^+\mu^-$	~0.6kHz
$e^+e^- \rightarrow \tau^+\tau^-$	~0.6kHz
dark matter/new particle ?	???

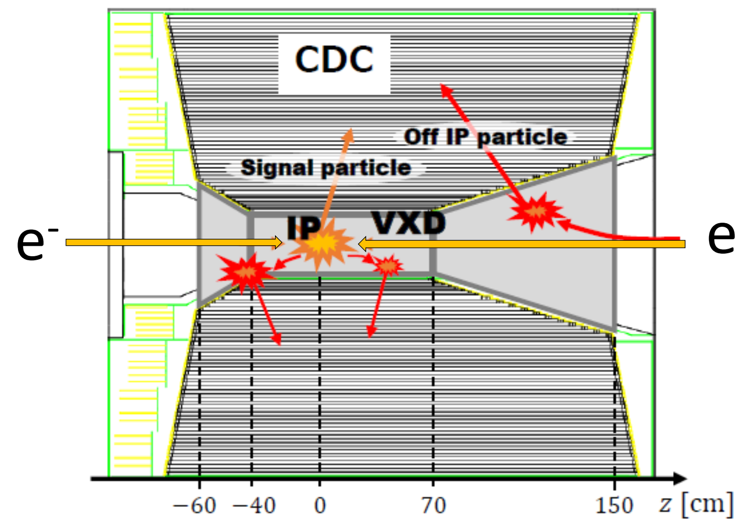
Physics target ~15kHz

Bhabha scattering



background >~300kHz

Beam background



-Maximum trigger rate at Belle II DAQ is 30kHz

→ trigger system is needed to reject background with S/N = ~1

Requirement for Belle II level1 trigger

-Belle II TDR in 2010: https://arxiv.org/abs/1011.0352

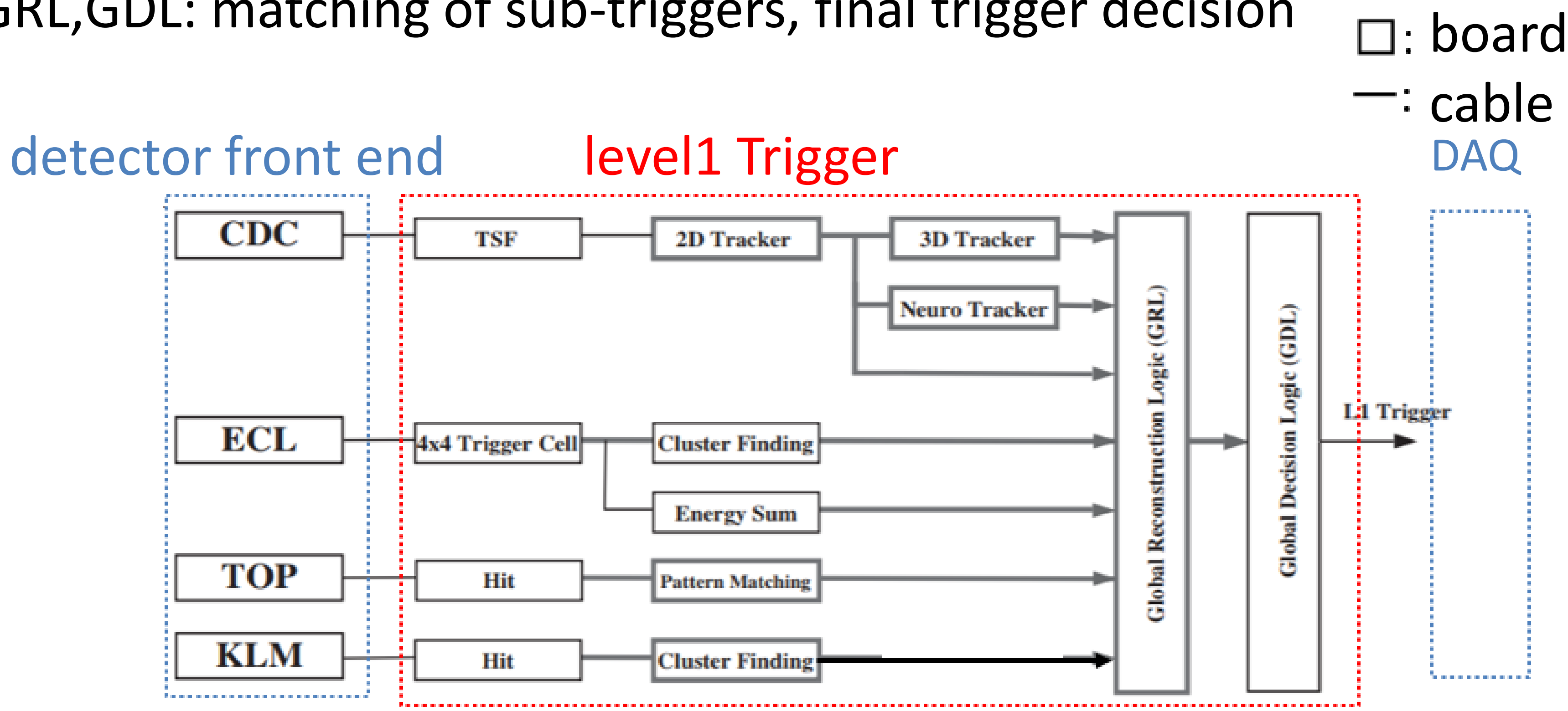
-Belle II: 40times higher luminosity than Belle

- -maximum trigger rate is increased accordingly
- -latency is increased by upgrade of detector FE with large buffer

	requirement for BelleII	**requirement for Belle**
Efficiency	~100% for BB pair	~100% for BB pair
Maximum trigger rate	~30kHz	~0.5kHz
Latency	5.0μs	2.2μs
Deadtime	no deadtime	no deadtime
Event timing resolution	10ns	~16ns

Belle II level1 trigger system

-CDC, ECL: main triggers for charged particles and gamma
-KLM: trigger muon
-TOP: measure event timing
-GRL,GDL: matching of sub-triggers, final trigger decision



Universal Trigger board (UT)

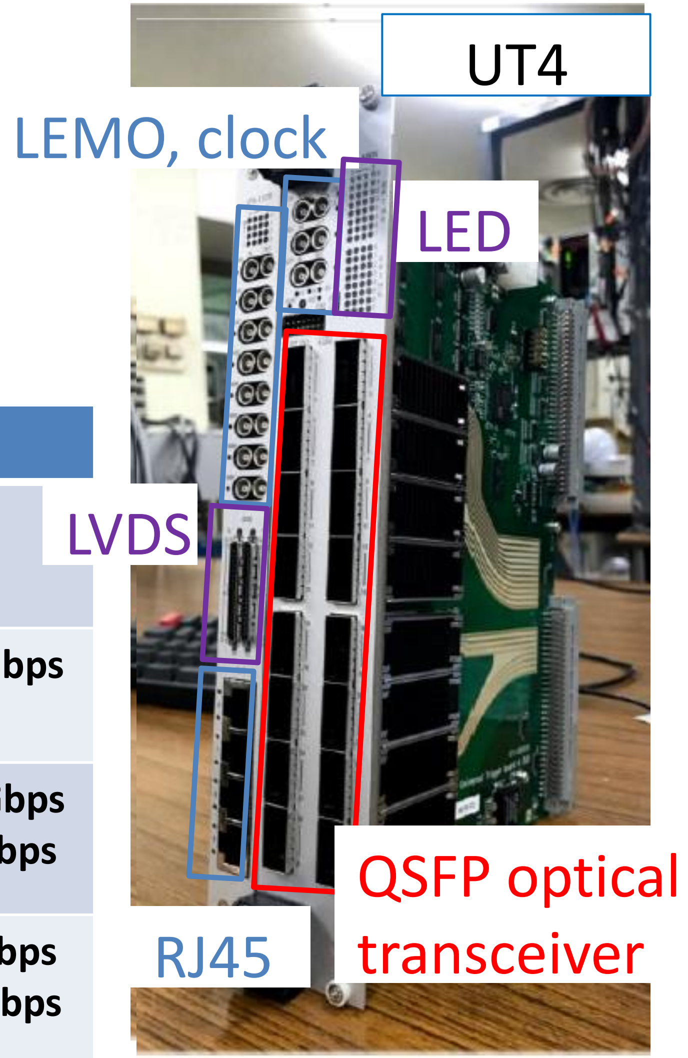
-Main board used by different sub-triggers commonly

-Large IO with optical transceiver

-Large FPGA resource

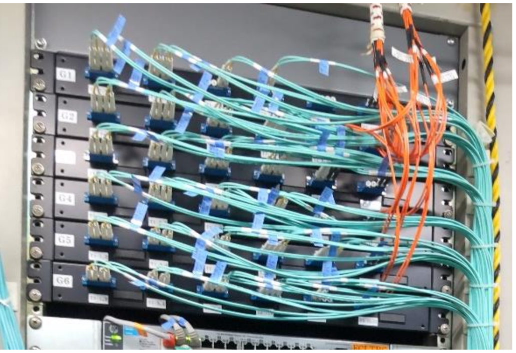
History of UT development

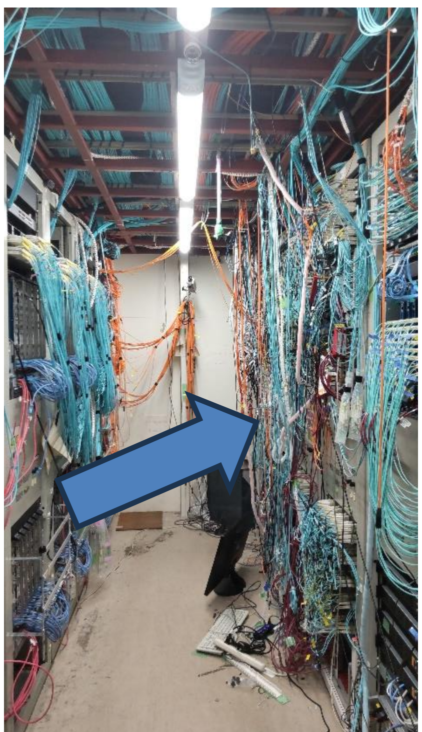
Name	Year	Main FPGA	#Logic cell	Main IO
UT (test)	2006	Spartan3	**50k(?)**	**LVDS 448ch**
UT2 (test)	2008	Virtex5 LX220T	**220k**	**GTP 3.1x32Gbps**
UT3	2011	Virtex6 HX380T,565T	**380~ 570k**	**GTX 6.2x40Gbps GTH 11x24Gbps**
UT4	2018	Virtex Ultrascale XCVU080/160	**1000~ 2000k**	**GTH 16x32Gbps GTY 25x32Gbps**



Trigger system in Ehut

patch panel (connect different type of optical fibers)





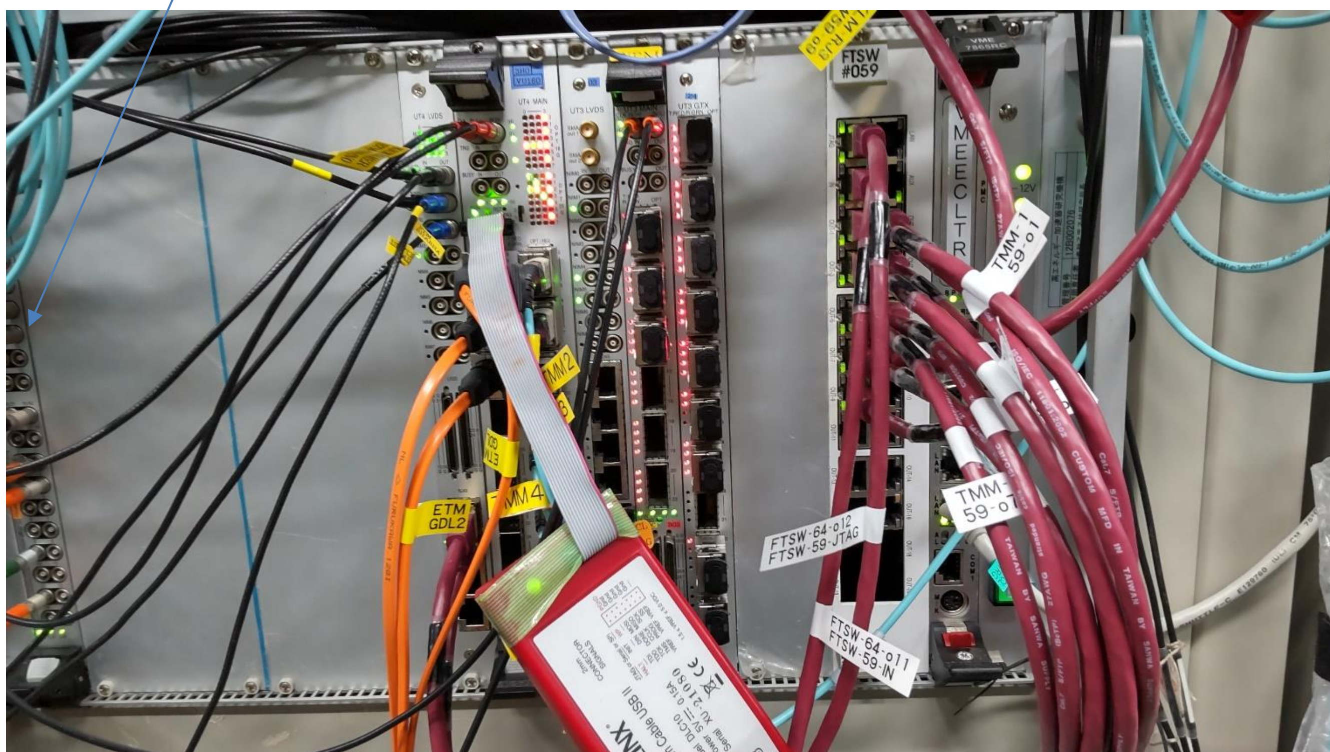
clock distributer

UT4

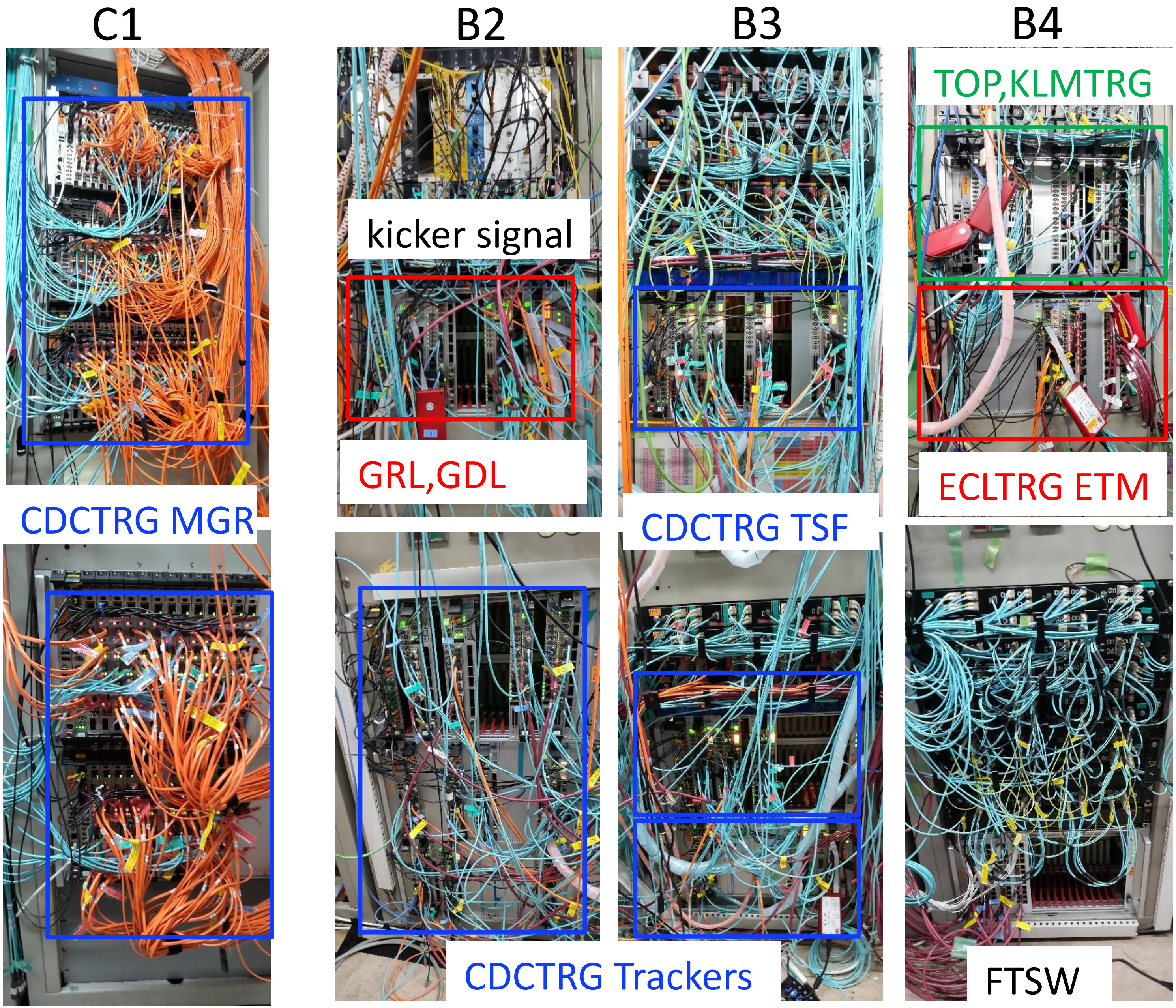
UT3

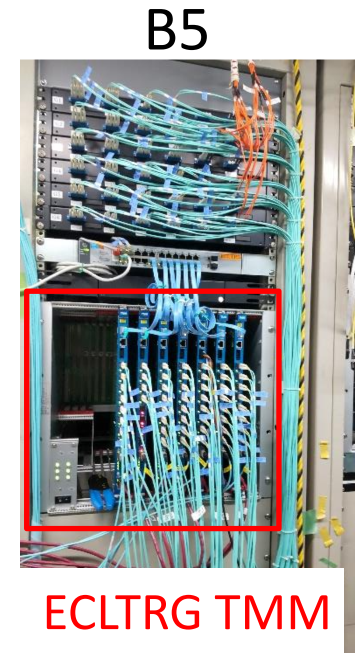
vmecpu

vmecrate



Trigger system in Ehut





don't imitate dirty cabling..

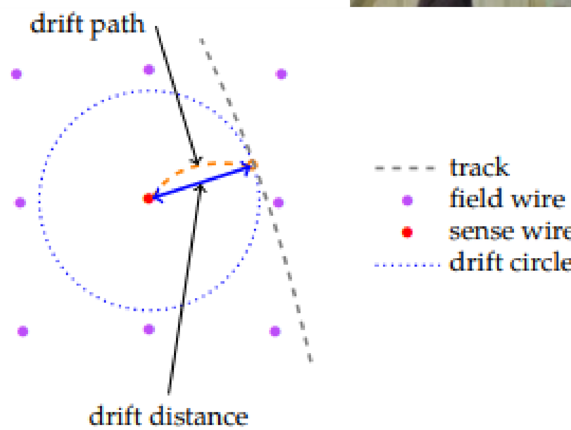
Sub trigger logic
(CDCTRG,ECLTRG)

CDC detector

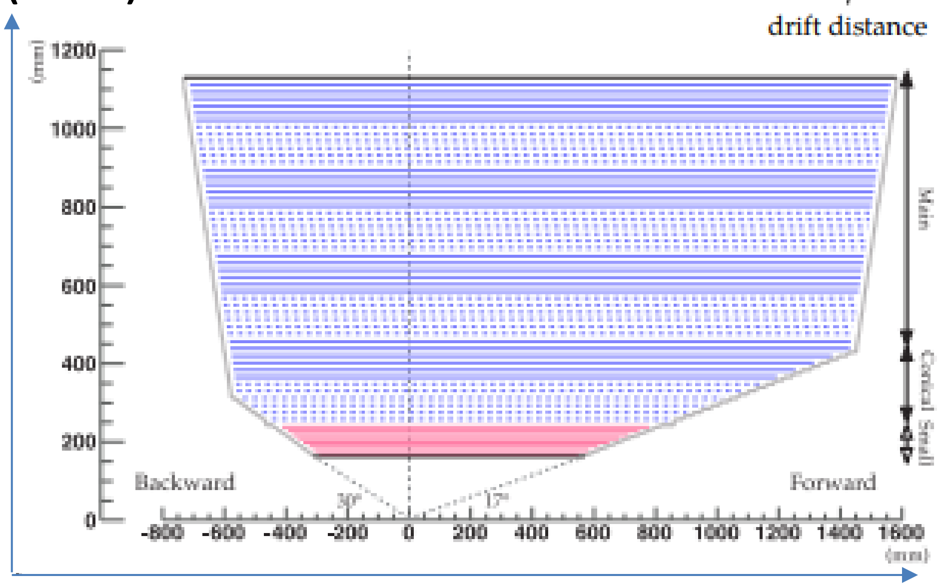
-Central drift chamber (CDC)

-Reconstruct charged particle
  -~14000 axial and stereo sense wire

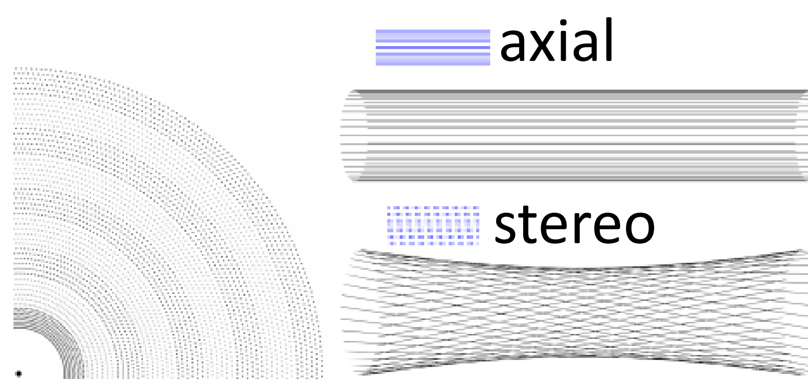
-Precise tracking
  -drift time ⇔ drift distance
  -drift time ~500ns



y(mm)



z(mm)

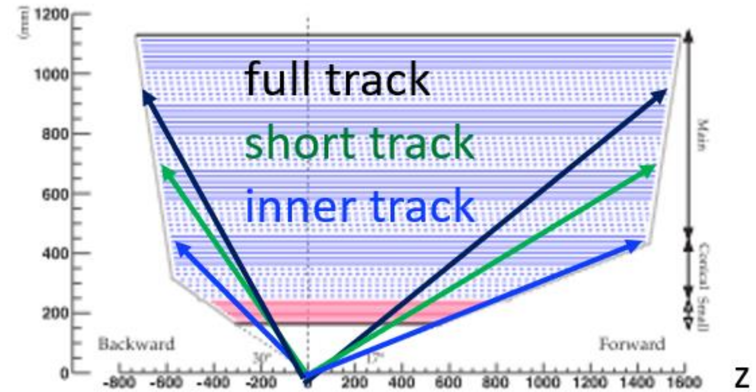


CDC Trigger

-Role: Trigger charged particles

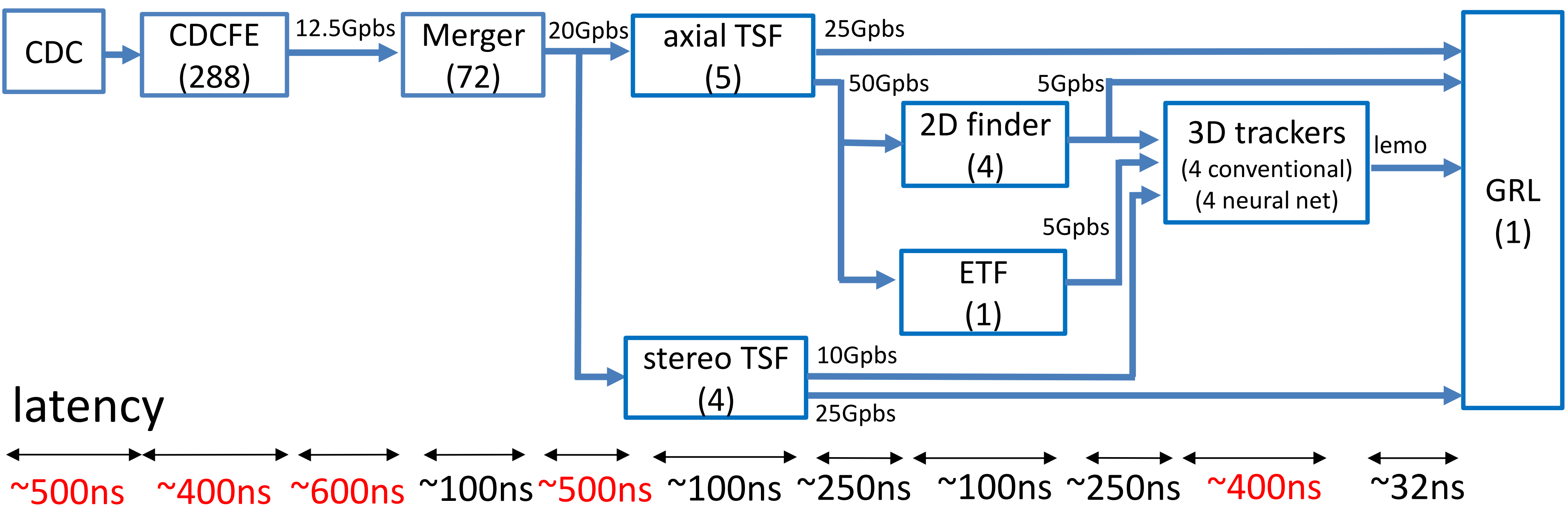
-Three kind of track with different θ region:

- -full track (f,y)
- -short track (s)
- -inner track (i)



-Consists of ~100 boards

(): number of boards

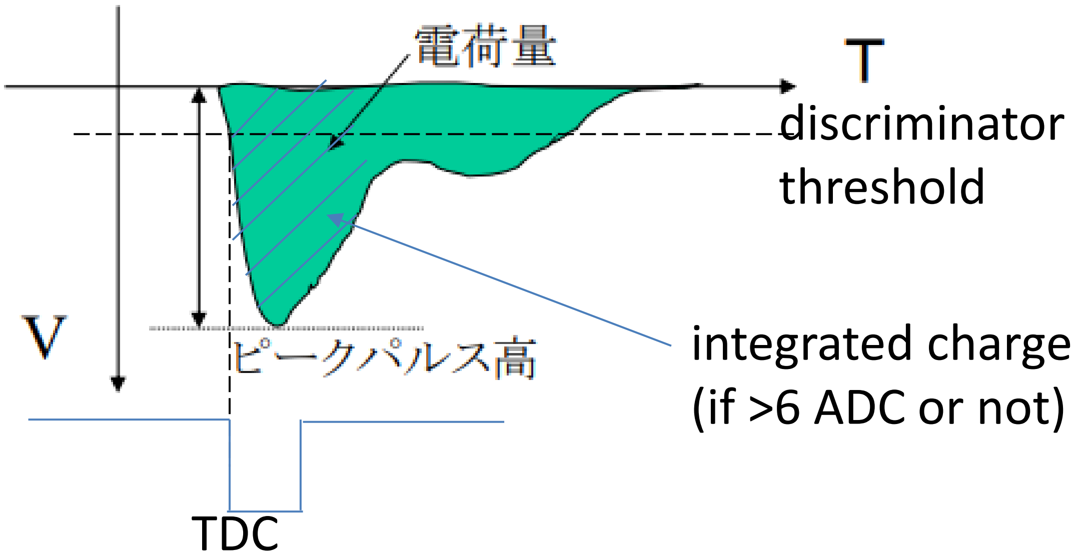


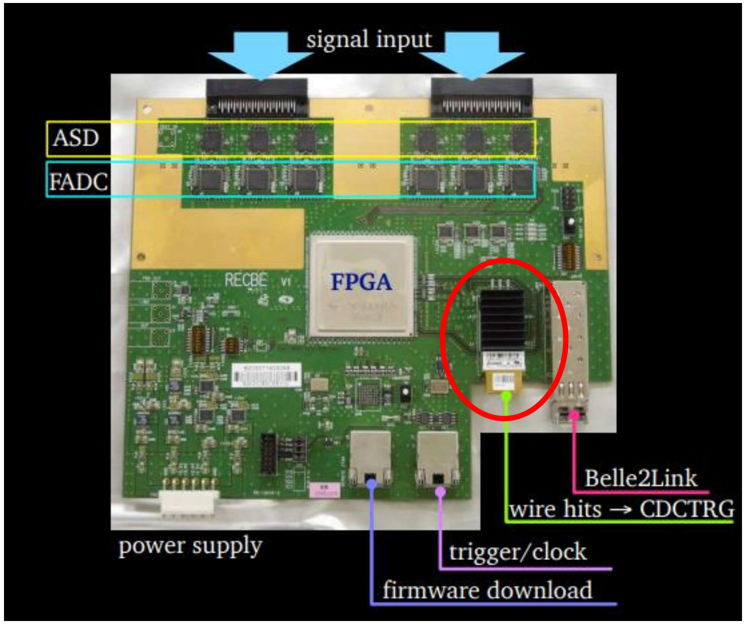
total: ~3.3μs

CDC trigger: CDC front end

https://iopscience.iop.org/article/10.1088/1748-0221/12/06/C06014

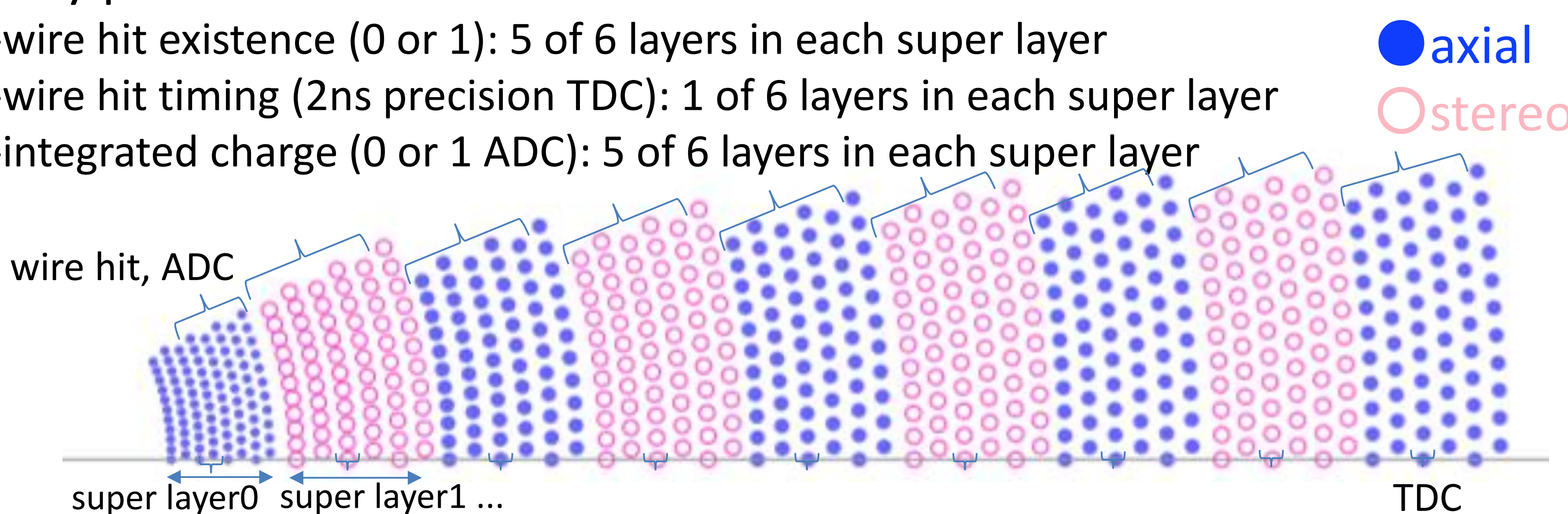
-digitize analogue signal on CDCFE





-Only part of information is sent to CDCTRG

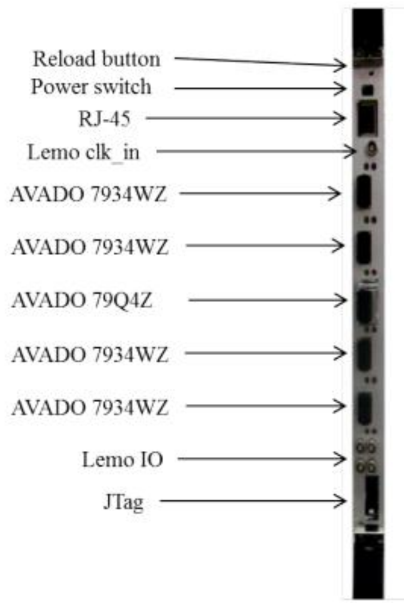
- -wire hit existence (0 or 1): 5 of 6 layers in each super layer
- -wire hit timing (2ns precision TDC): 1 of 6 layers in each super layer
- -integrated charge (0 or 1 ADC): 5 of 6 layers in each super layer

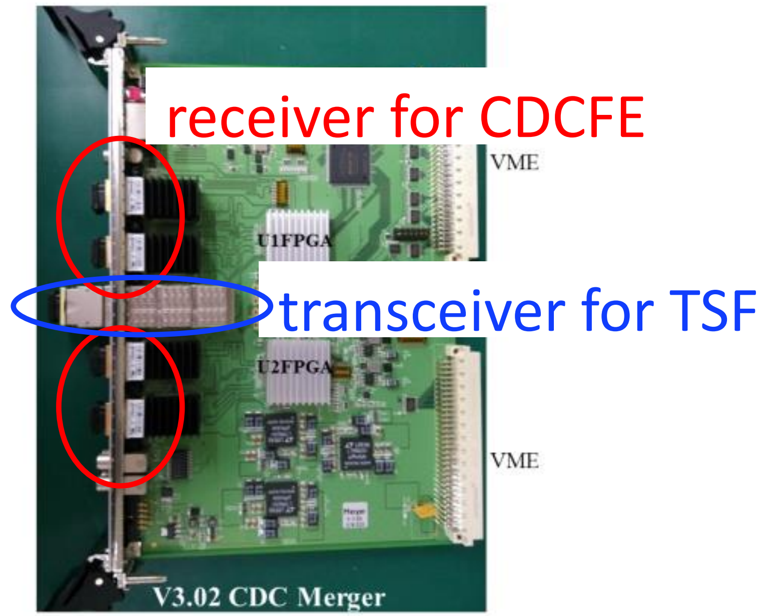


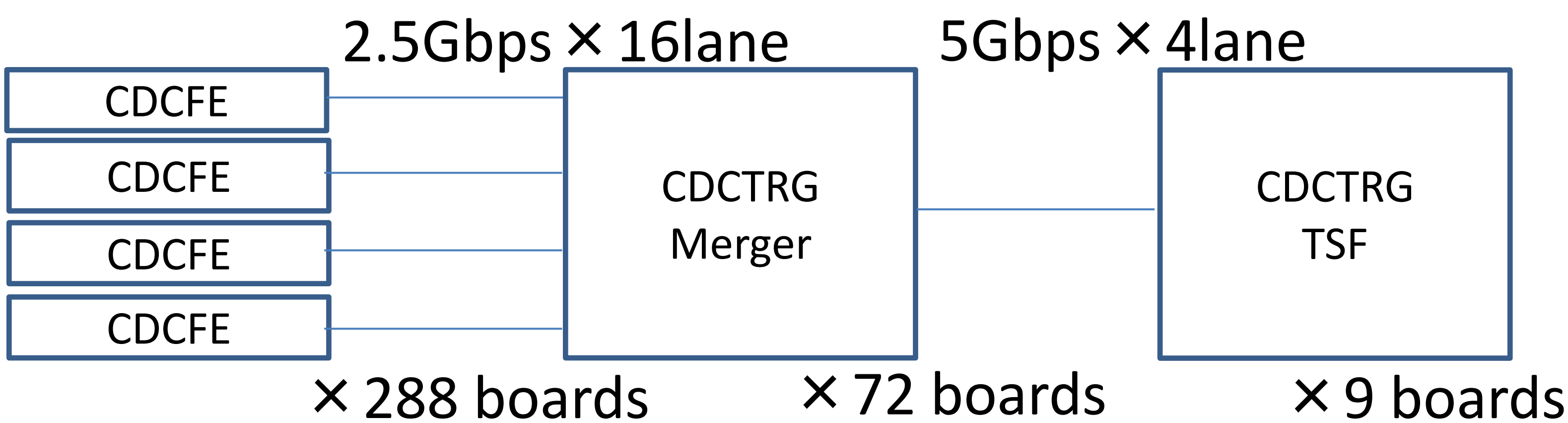
CDC trigger: MGR

-merge signal from four CDCFE
-send merged signal to TSF

https://docs.belle2.org/record/439/files/BELLE2-NOTE-TE-2016-013.pdf



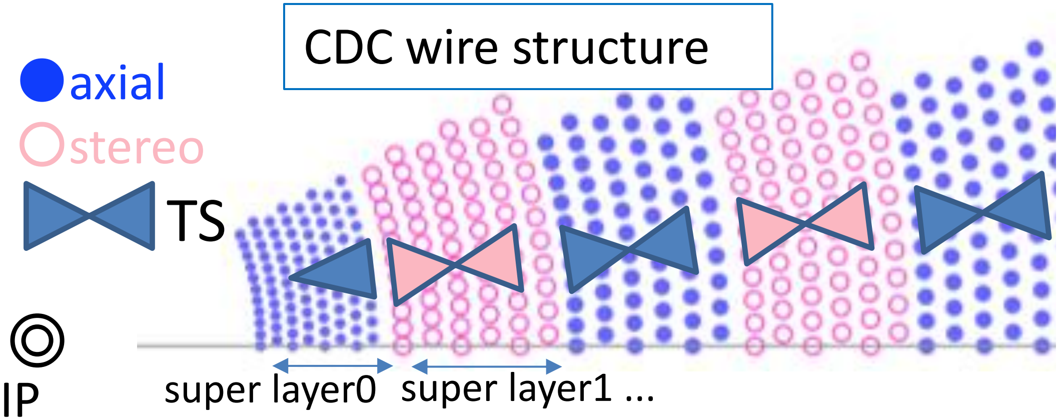


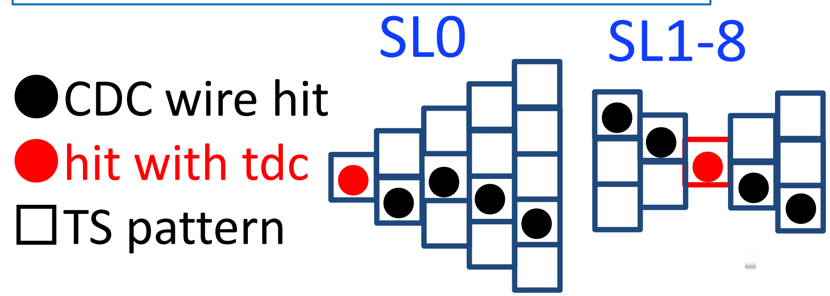


CDC trigger: Track segment finder (TSF)

-Find bunch of wire hits (Track segment, TS) to reduce noise and data size

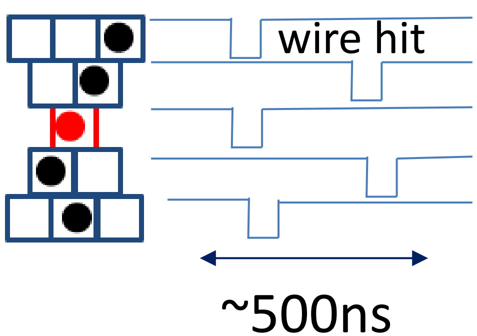
- -require 4 of 5 layer hits in each super layer
- -pt>~0.35 GeV is required: curing track is not reconstructed at this stage

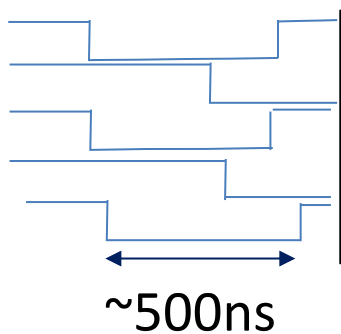




TSF algorithm

receive wire hit with ADC>6 → 500ns buffer → AND (4 of 5 layer hits) → Pack TS info





Look Up Table

-TS found or not

-Left/right flag (pre-calculated in table)

-TS position
-wire hit pattern
-TDC of central wire
-Left/right flag

CDC trigger: 2D tracking

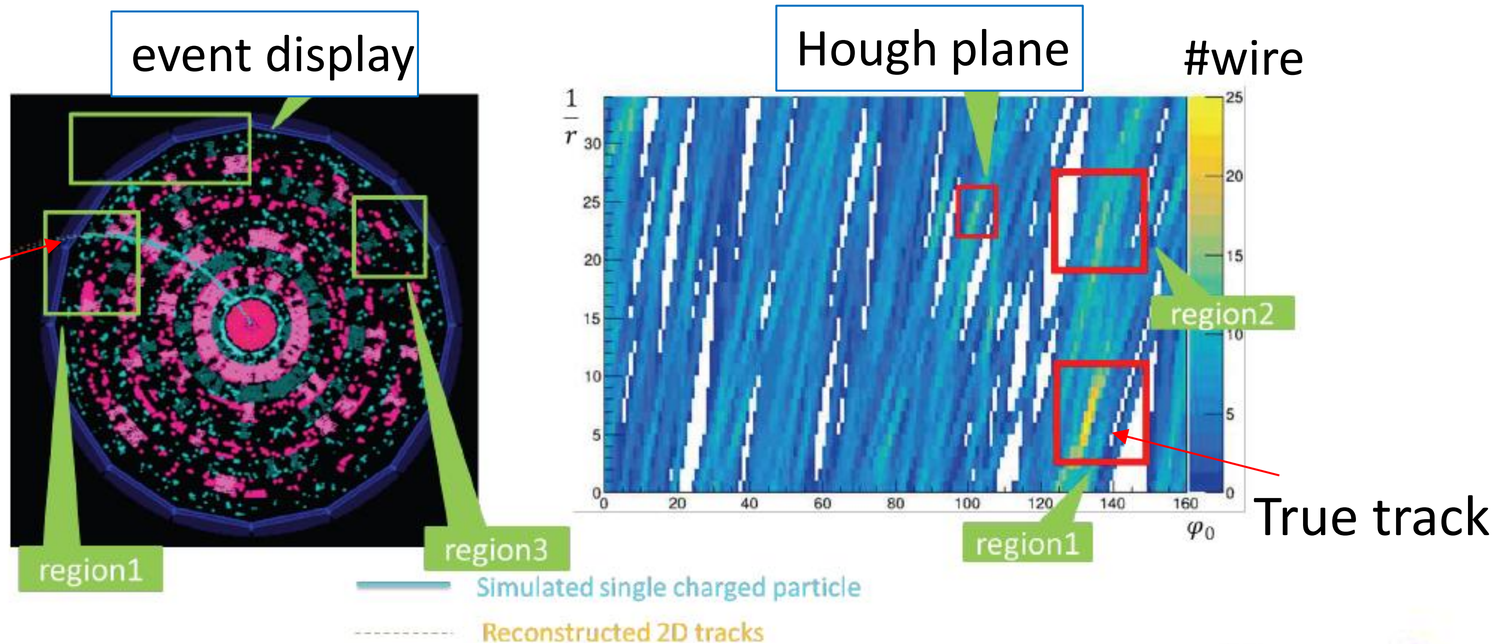
-Transform wire hit pattern inside TS to Hough plane (pt, ϕ). Only axial layer.

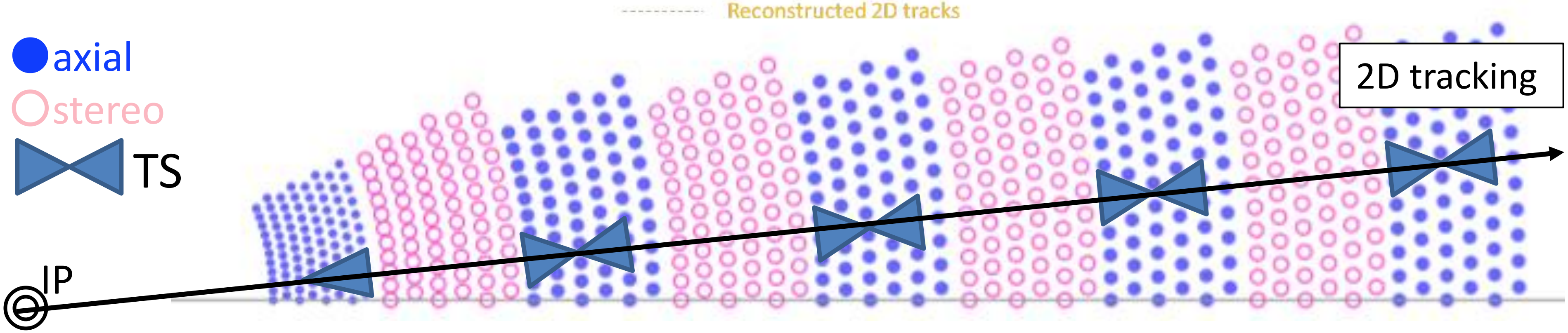
- -pt: 34bin in [0.3-10] GeV, ϕ: 160 bin in [0-360] degree
- -#wires>=20 is required (now >=16) in Hough peak
- ->98% efficiency at barrel, pt>0.4 GeV

https://docs.belle2.org/record/3592/files/BELLE2-MTHESIS-2023-012.pdf

phase3 BG MC

True track

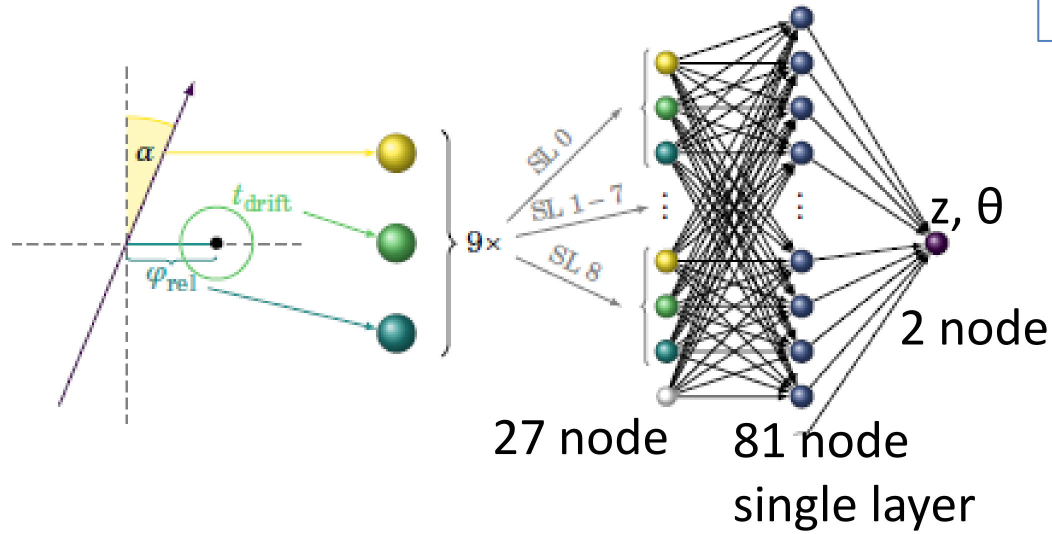




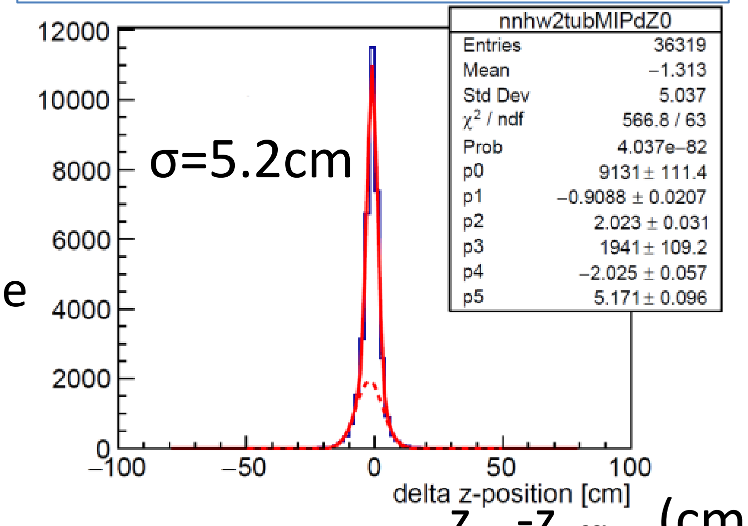
CDC trigger: 3D tracking

-3D track fitting to measure z position, by using neural network

- -input: 2D track(ϕ_{rel}, α), central wire hit timing of TSF
- -output: z,θ of 3D track
- -Training is done at offline with offline reconstructed track

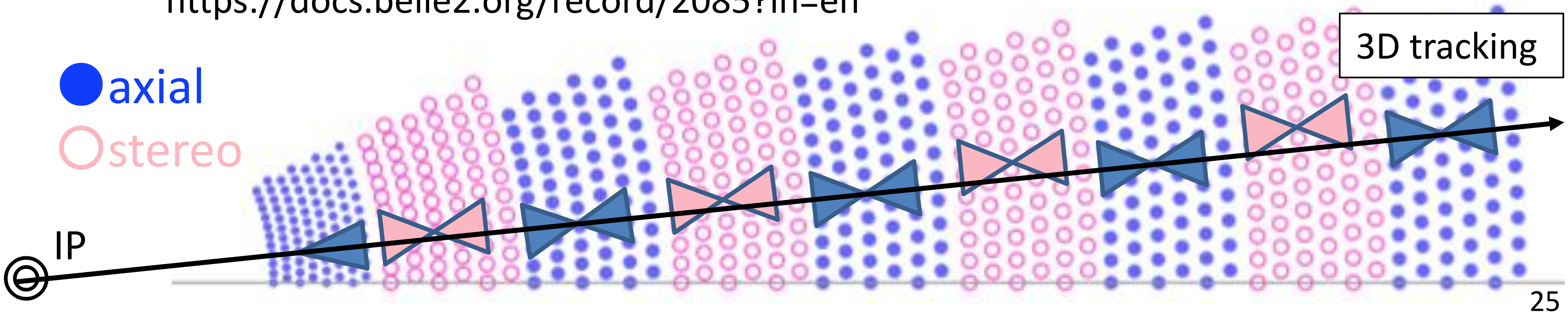


CDCTRG Z resolution at IP



z_{trg}-$z_{offline}$(cm)

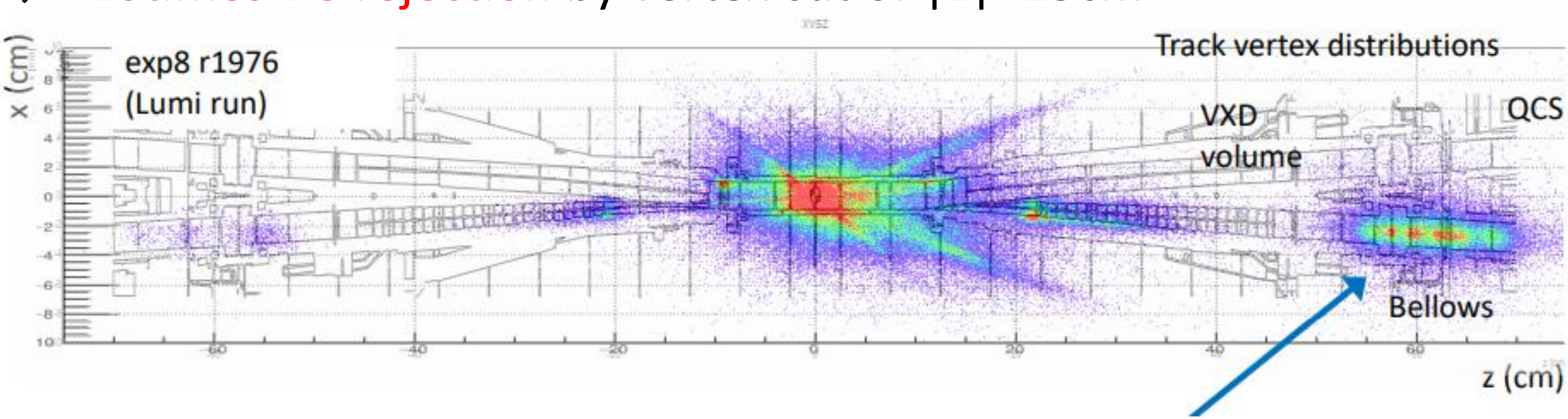
https://docs.belle2.org/record/2085?ln=en

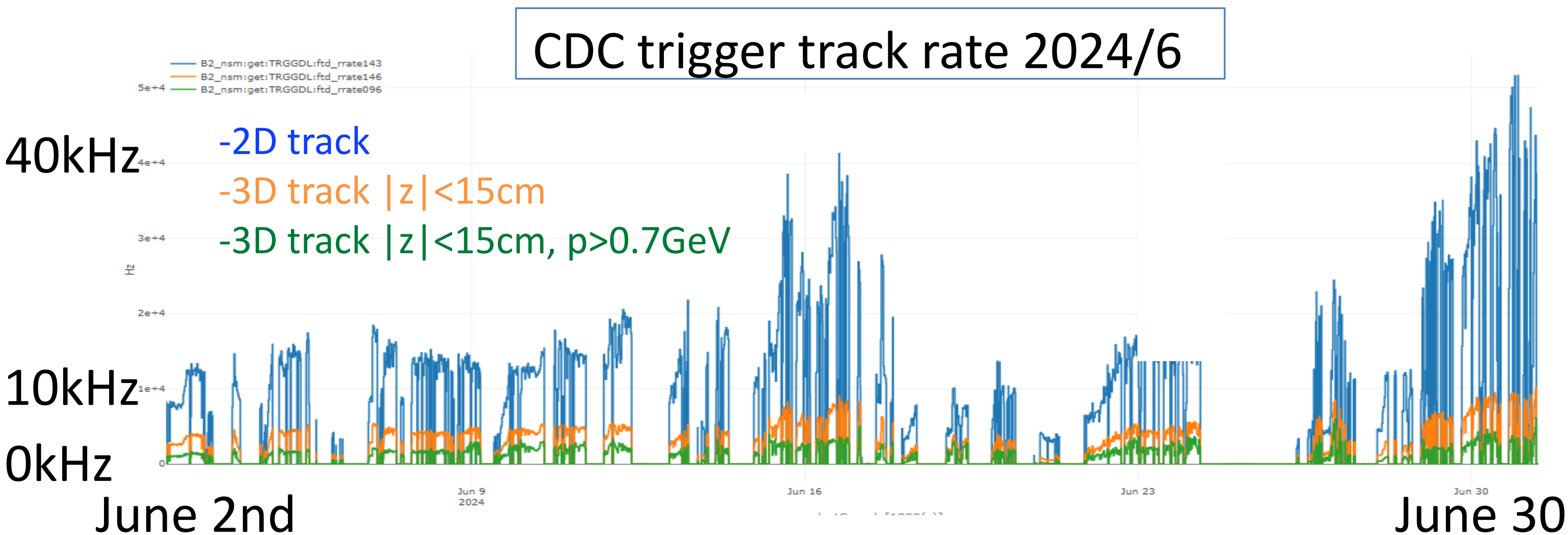


beam BG rejection

-beamBG is coming from large Z vertex with low momentum

→ ~10times BG rejection by vertex cut of |z|<15cm



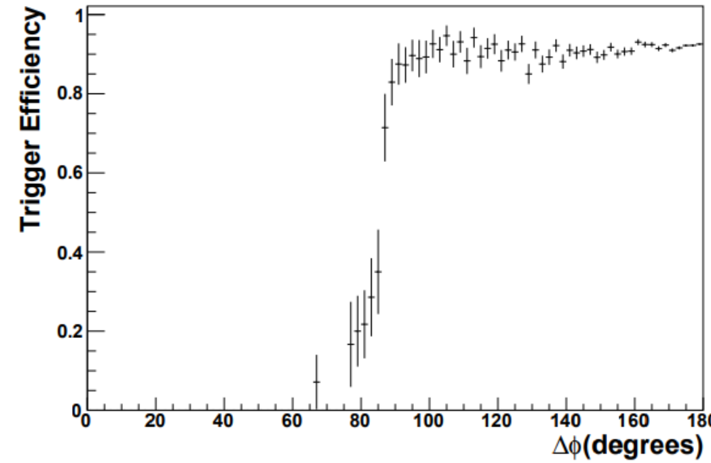


CDC trigger: performance

-Major trigger conditions:
-#track>=1, p>0.7GeV (stt)
-#track>=2, opening angle Δϕ>90deg. (fyo)
-#track>=3 (ffy)

-~95% efficiency per track is achieved

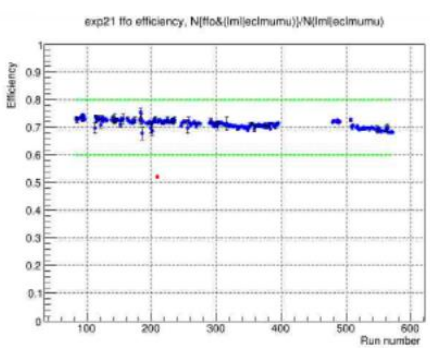
dimuon efficiency of back-to-back 2track trigger



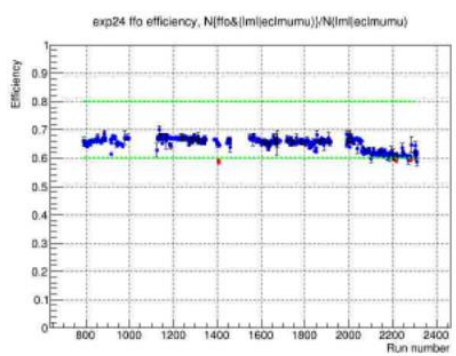
-large run dependency due to CDC gas gain, dead channel etc:
At maximum ~10% change of efficiency. (much improved in 2024)

two track efficiency with mumu

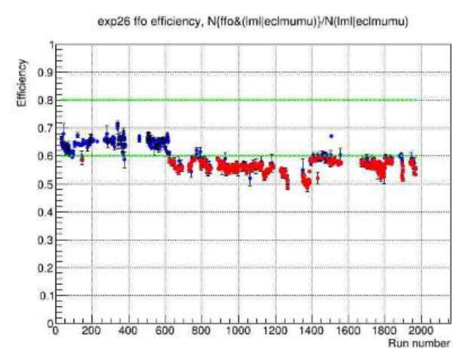
2021c



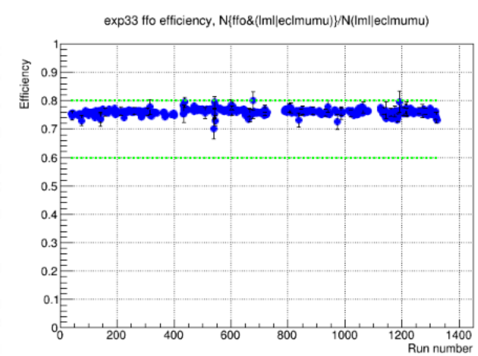
2022a



2022b

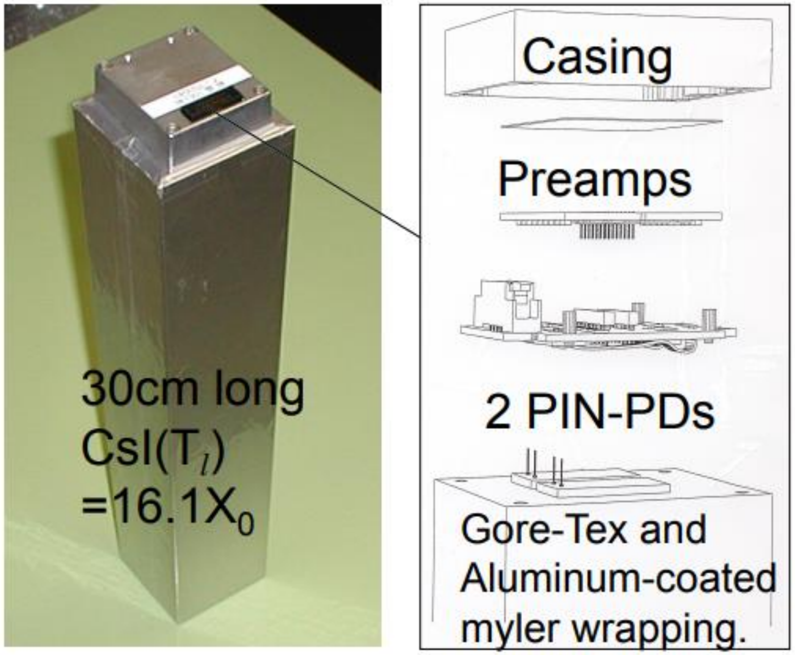


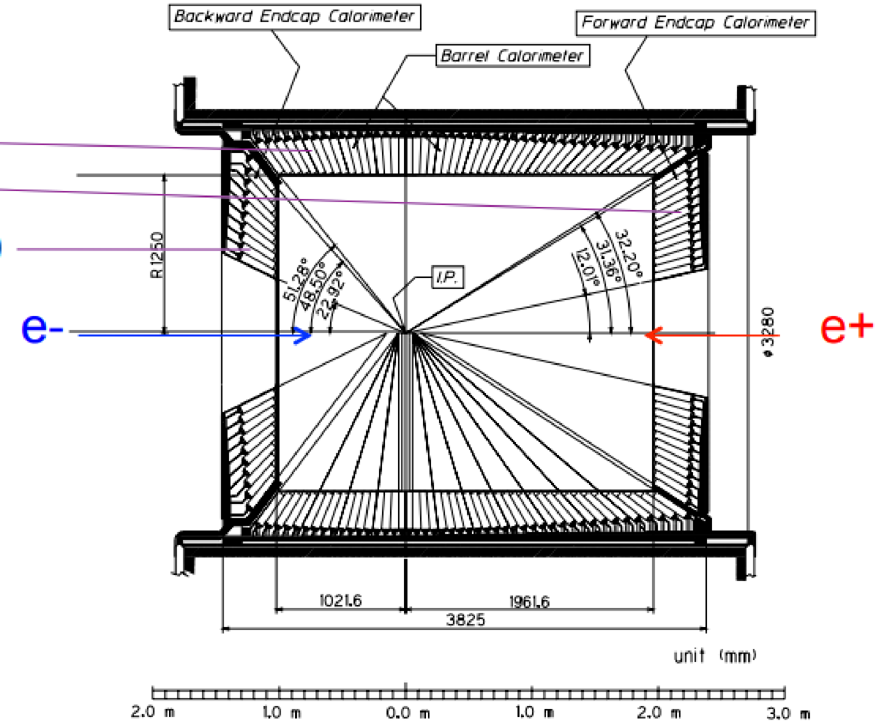
2024b



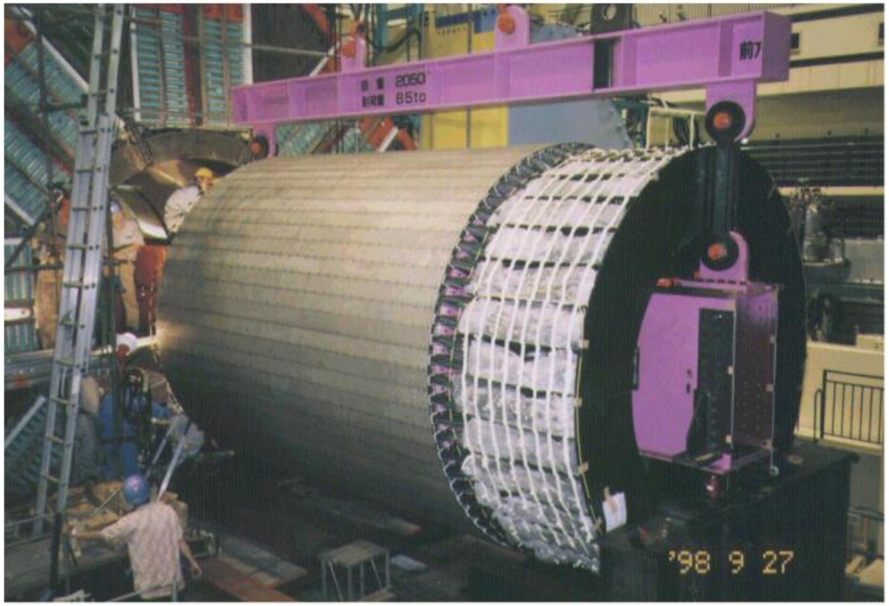
ECL detector

- -Electromagnetic calorimeter
  - -measure photon and charged particles
  - -excellent energy resolution with CsI
  - -high angular acceptance



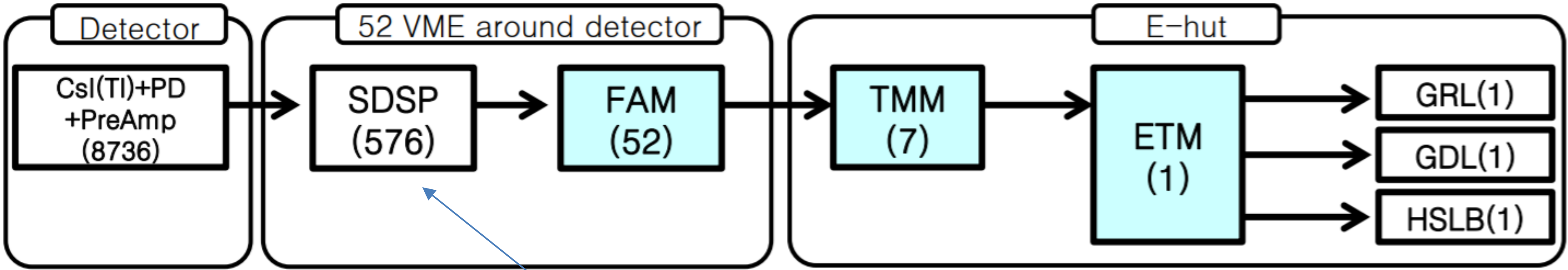


8736 Crystals



ECL trigger: Shaper DSP

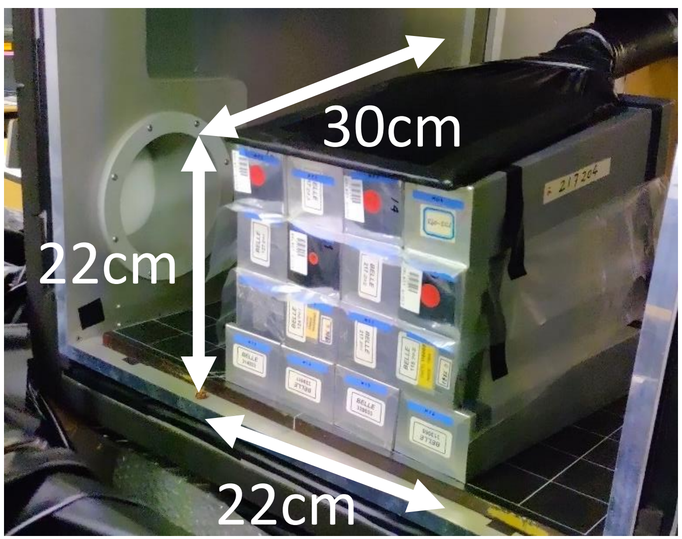
(): number of boards



-Shaper DSP:

Take analog sum of 16 crystals (Trigger cell)

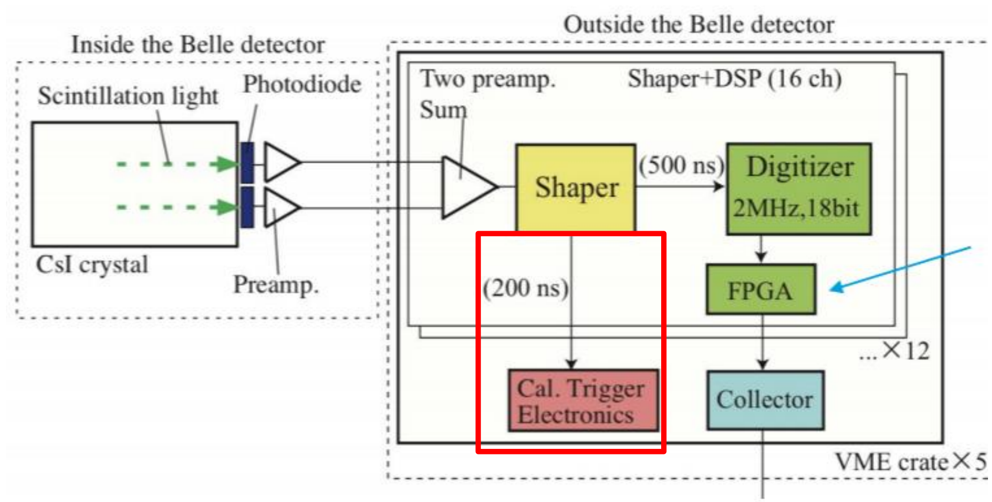
one Trigger cell (TC)



-Different shaper is used for ECL and ECLTRG

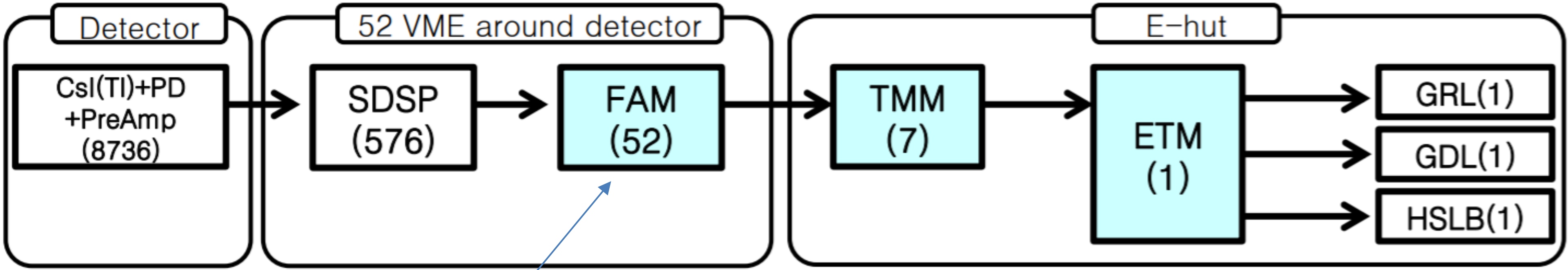
-200ns faster shaper for ECLTRG

-measured energy can be different from ECL



ECL trigger: FAM

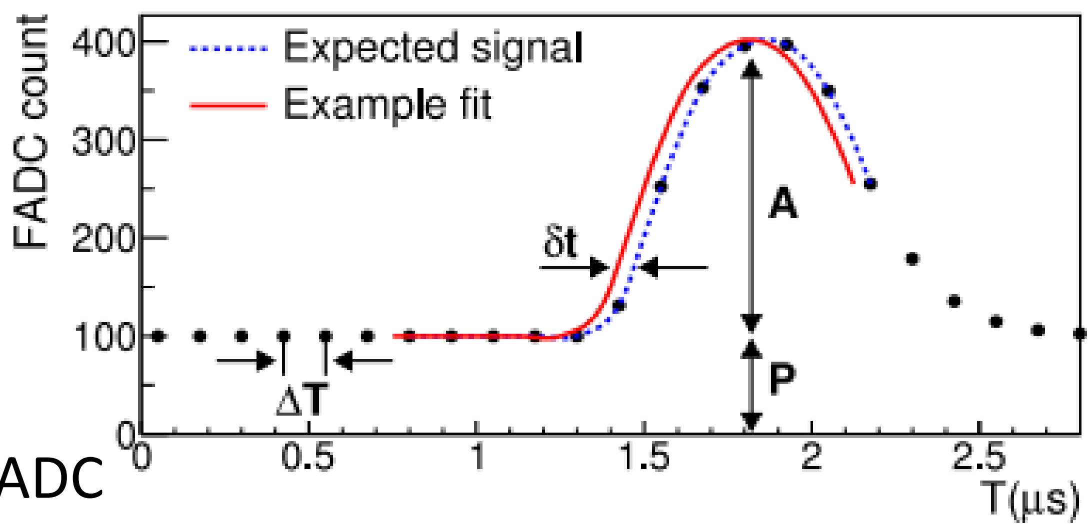
(): number of boards



Degitization, waveform fit

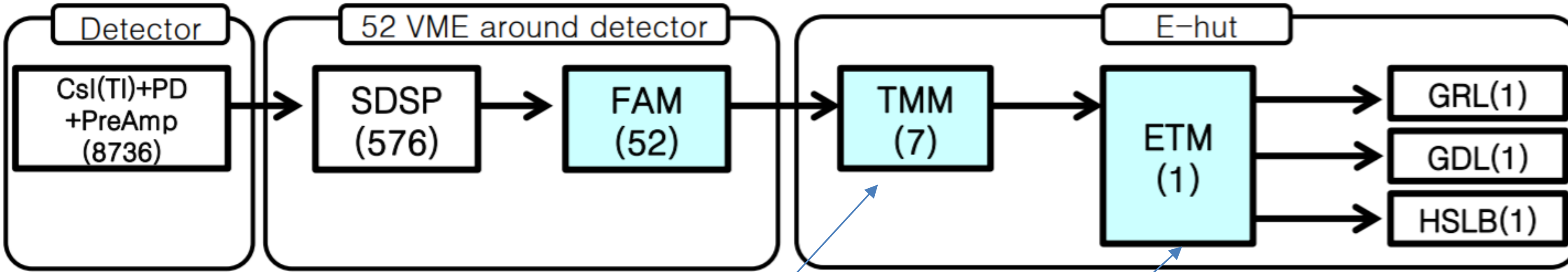
-Waveform fit (only once by using a template) to estimate energy, timing

8MHz FADC



ECL trigger: TMM, ETM

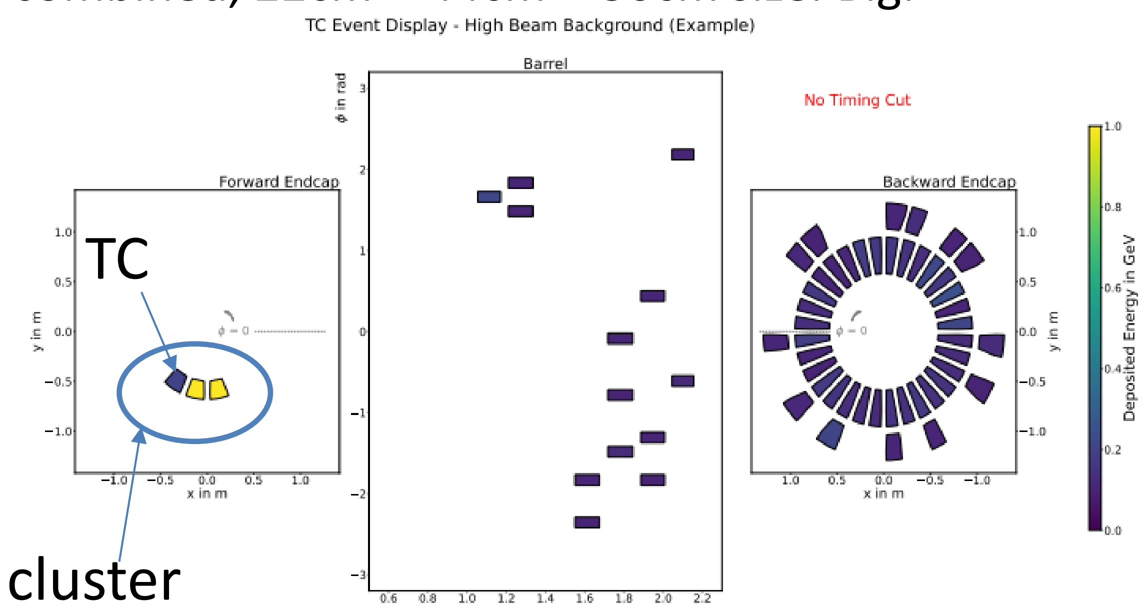
(): number of boards



-TMM: merge and send all TC energy and timing to a UT4

-ETM: Combine next TCs to reconstruct a cluster

- **>100MeV required to TCs**: main reason of energy difference btw. ECL and ECLTRG
- if two TCs are combined, 22cm × 44cm × 30cm size. Big.

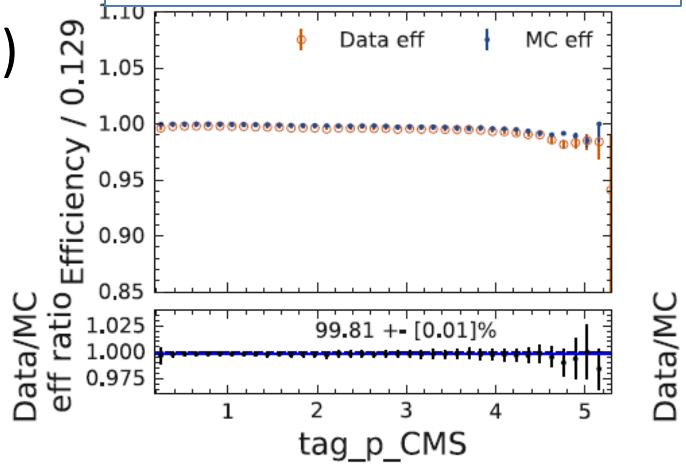


ECL trigger: performance

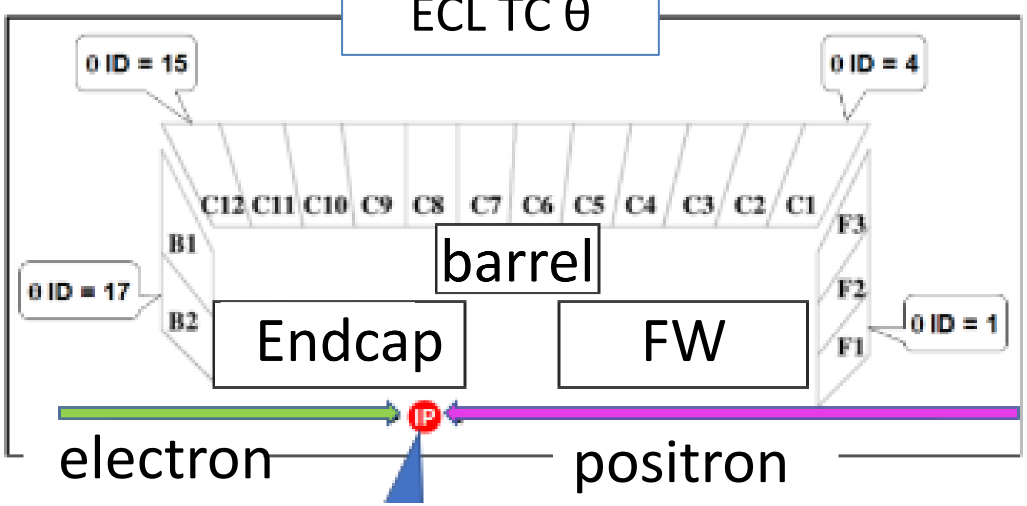
-Major trigger condition:
- -hie: energy sum>1GeV in $2<=\theta_{ID}<=15$
- -c4: #cluster>=4 in $2<=\theta_{ID}<=15$
- -several combination of cluster and energy (lmlxx)

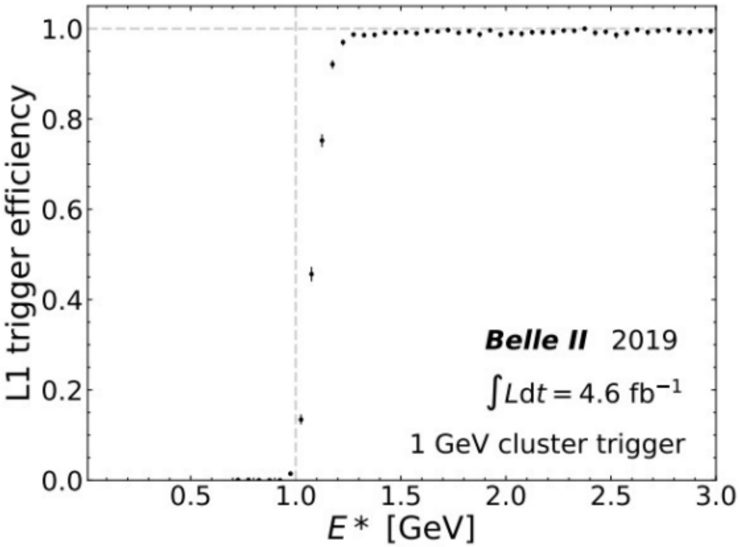
-~1% level data/MC agreement
- -most stable trigger: small run dependency

ECLTRG efficiency with e



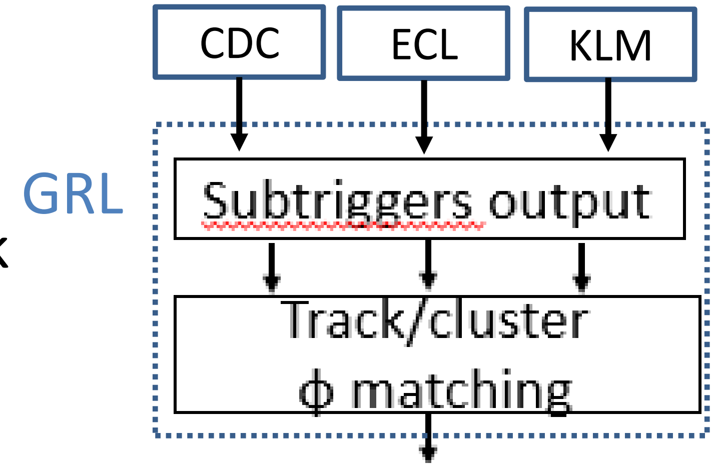
ECL TC θ

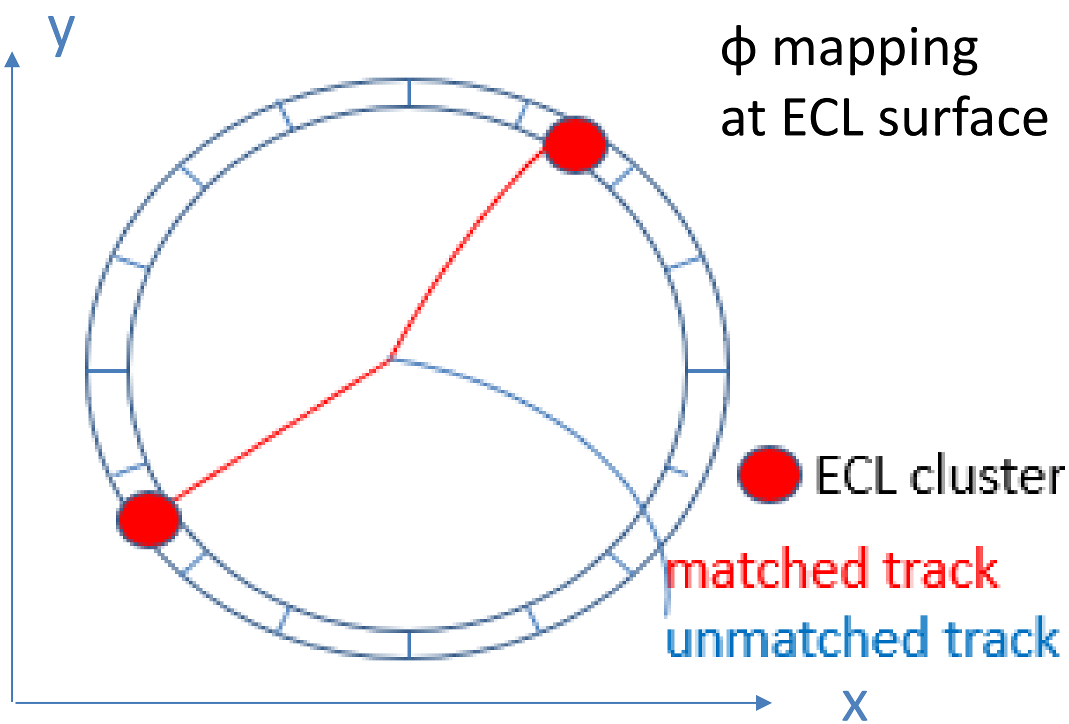




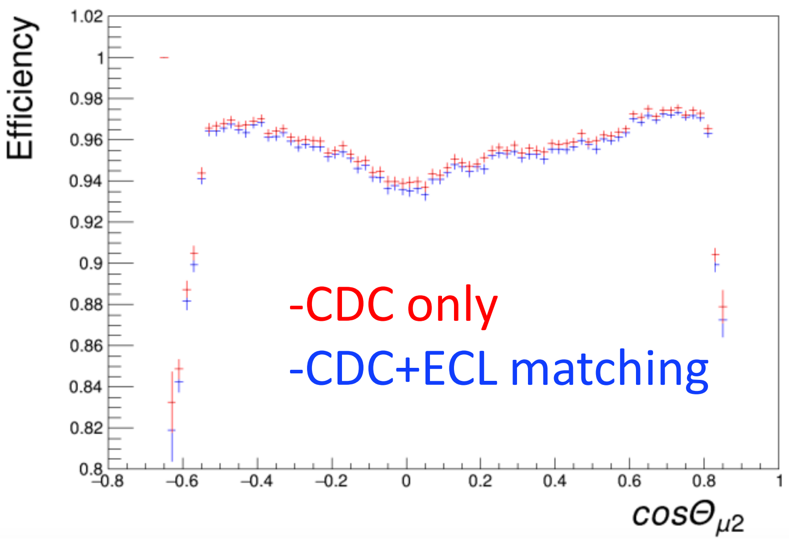
GRL

-GRL: Global reconstruction logic
- -take ϕ matching of CDC/ECL/KLM/TOP
- -event classification by using neural network





Efficiency with μμγ



99.5% matching efficiency

GDL

-GDL: Global decision logic

-ITD: adjust delay and persistence of input

-FTDL: calculate if trigger condition is 1 or 0

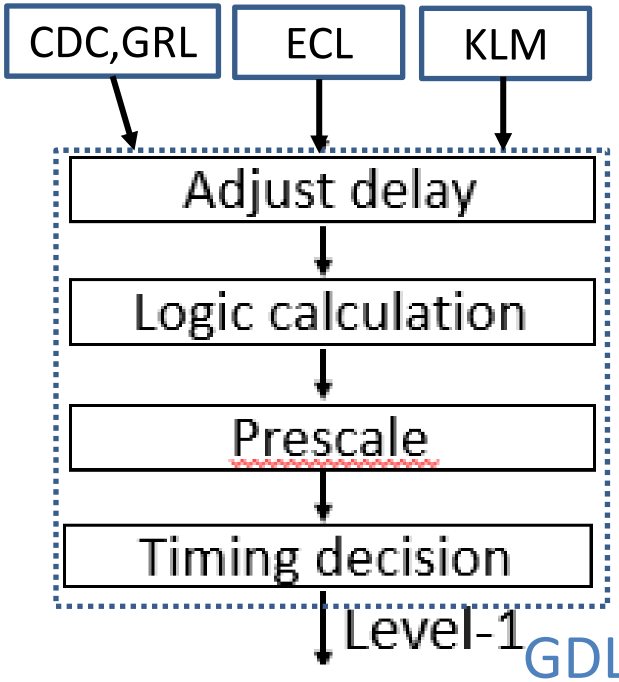
-trigger condition = AND, OR of input bit (output bit)

-in total, ~200 trigger conditions

-PSNM: apply prescale in each trigger condition

-prescale=10: fire a trigger if the trigger condition is satisfied 10 times

-TMDL: combine trigger condition and event timing



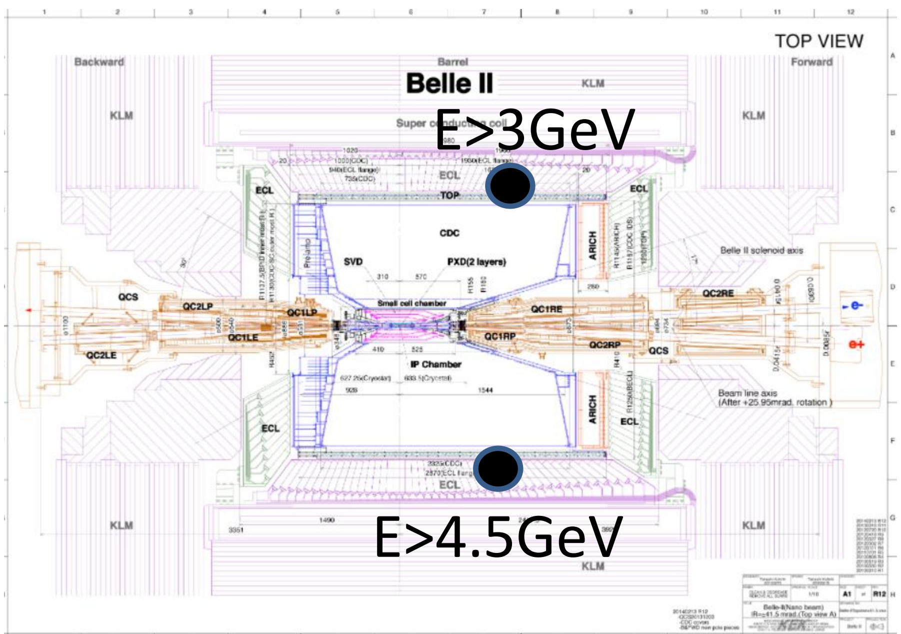
Veto

Bhabha veto with ECL trigger

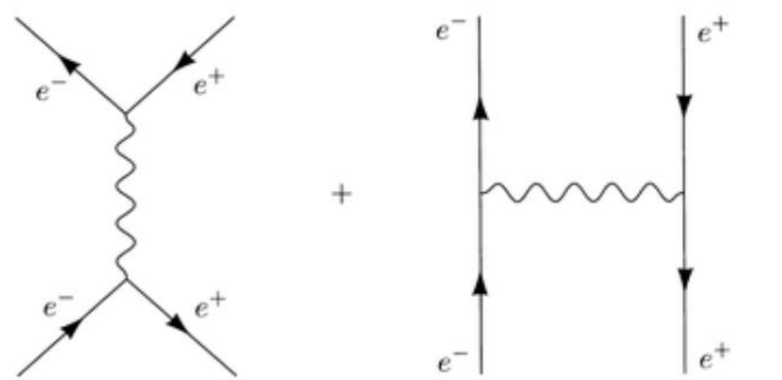
-Two back-to-back high energy electrons are produced by Bhabha.
Large cross-section: ~50kHz.

-If following condition satisfied at ECLTRG, “Bhabha veto” is fired:
[E1>4.5GeV, E2>3.0GeV, $160<\Delta\phi_{CM}<200$deg, $165<\Sigma\theta_{CM}<190$deg]
->~80% Bhabha rejection

-This veto is applied to most of trigger bits



Bhabha

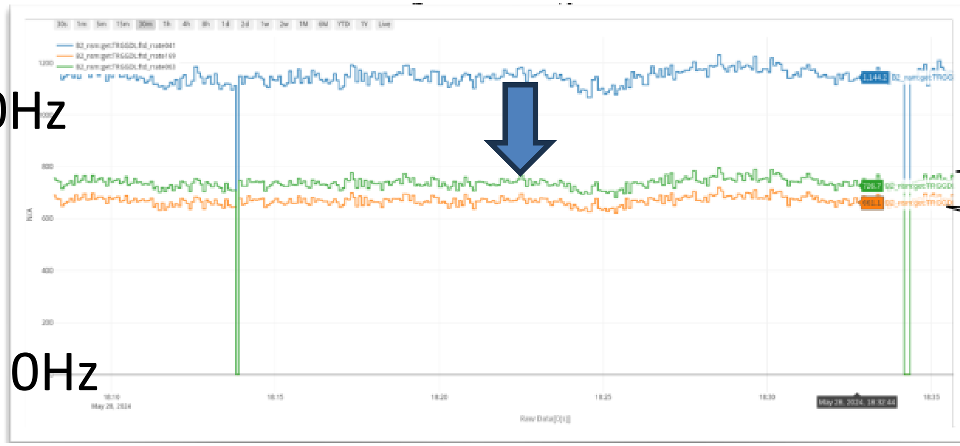


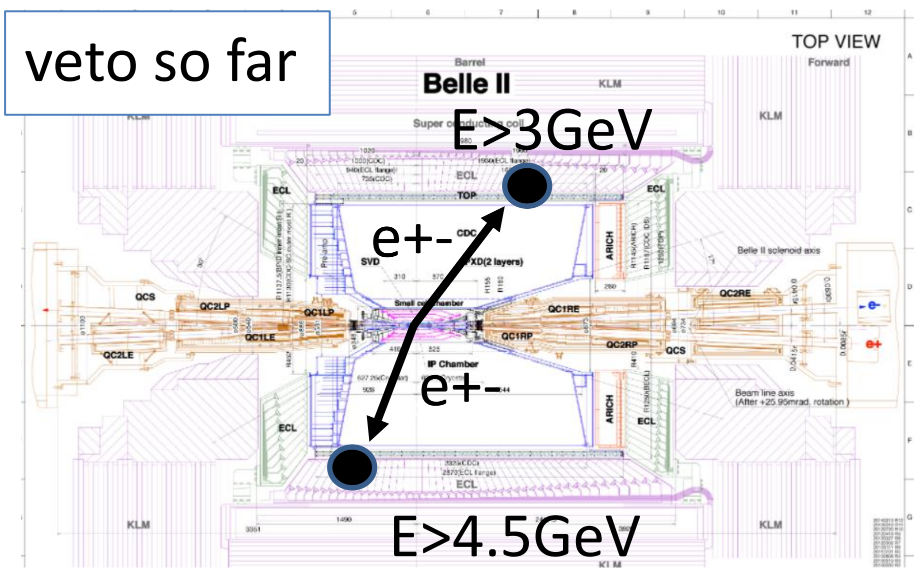
New Bhabha veto with ECL trigger

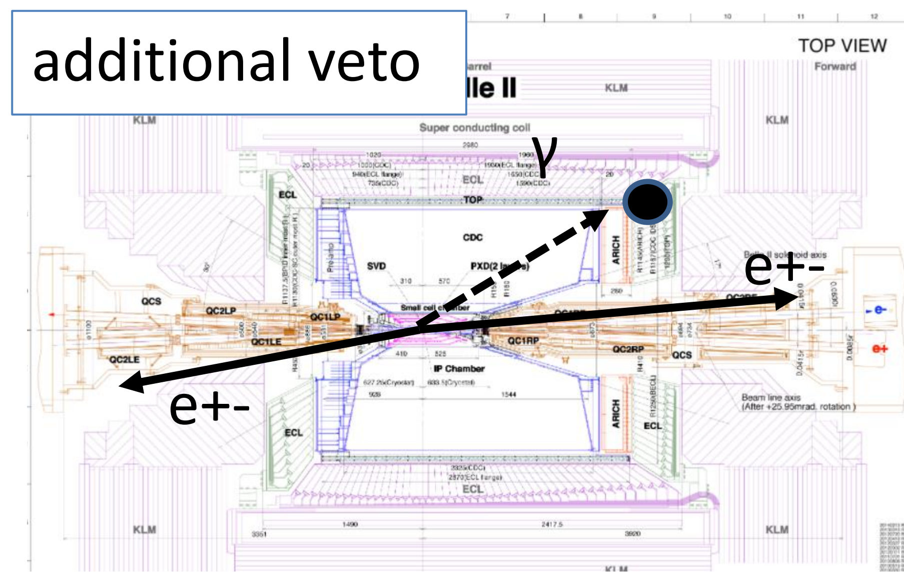
-new Bhabha veto for energy sum 1GeV trigger: ~90% Bhabha rejection

-additional veto: (#cluster==1 at endcap) OR (#cluster==2, lower energy at endcap)

->Will be activated if trigger rate reaches DAQ limit





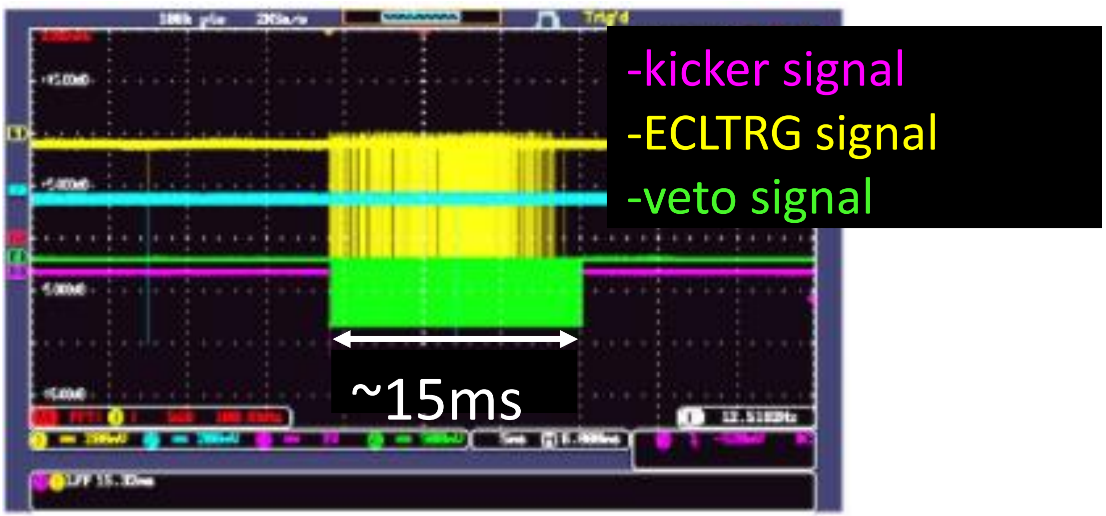


Injection veto

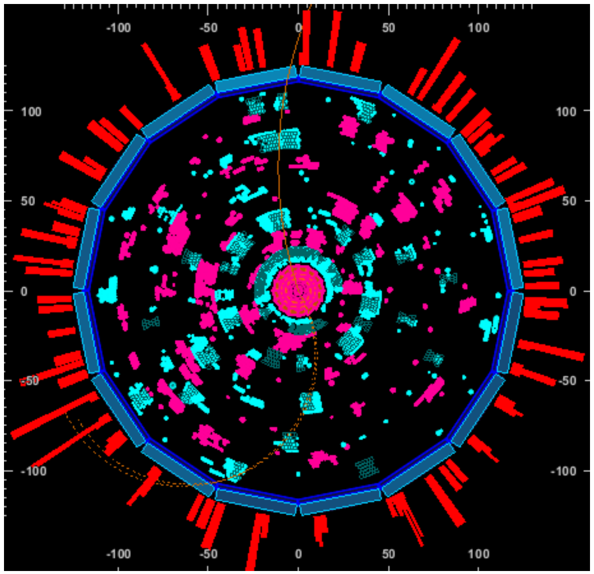
-Huge background appear just after beam injection

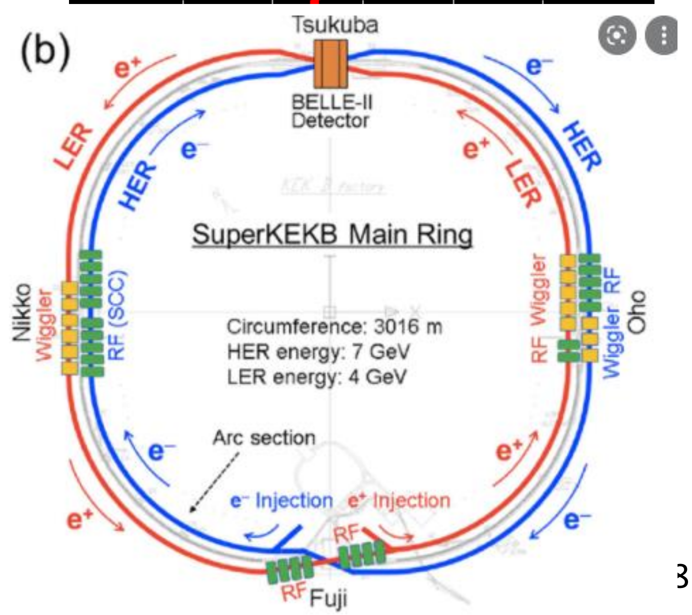
-Belle II BG level is high every turn(10μs), when the injected beam pass through Belle II

-trigger is vetoed for a while after beam is injected to main ring ->~99% BG rejected



Injection BG





-Veto causes large DAQ deadtime of 5~15%

-several efforts were done since 2019

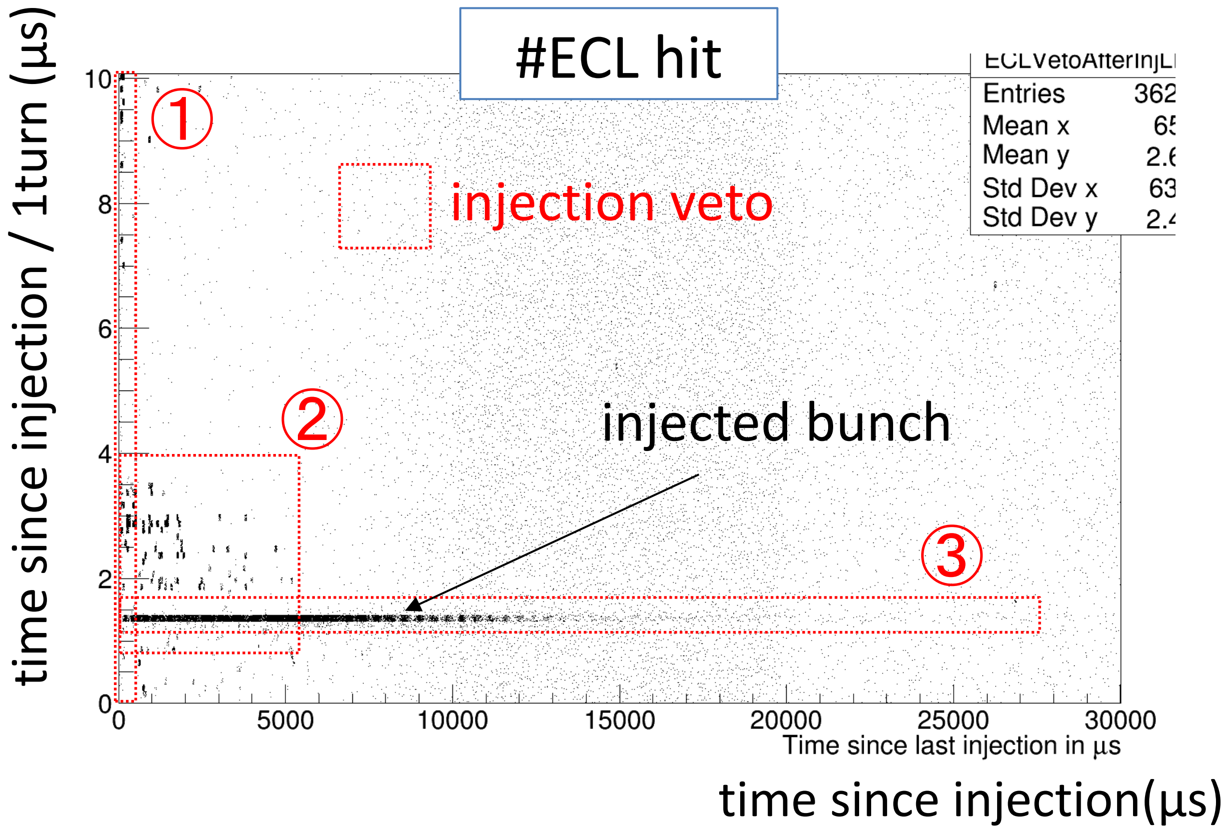
Belle II Injection veto

-Injection veto structure

-①~0.5ms after injection: veto trigger entirely (since Belle)

-②0.5~10ms after injection: veto trigger 3~4μs around injected bunch (2019)

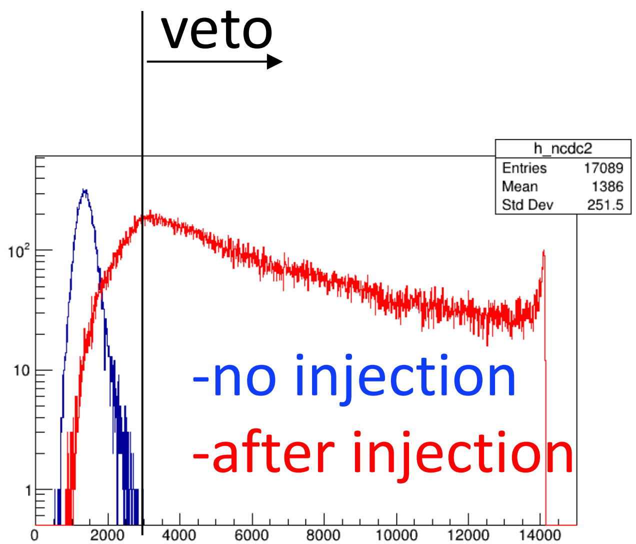
-③10~30ms after injection: veto trigger 1~2μs around injected bunch (2020)



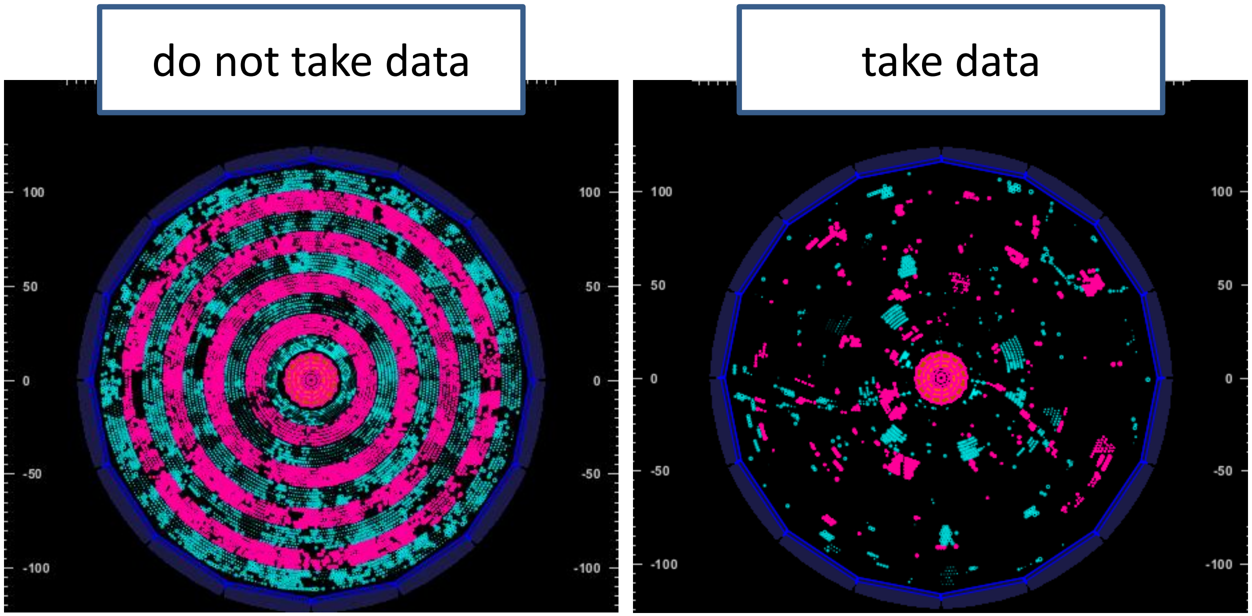
Belle II Injection veto

-Active injection veto (2024)
  -check occupancy of ECLTRG(#TC hit) and CDCTRG(#wire hit)
  -if occupancy is lower than threshold, take data even after beam injection

-~5% dead time reduction, 10~20% trigger rate increase.
 Data quality may be affected → please analyze the 2024 data carefully !



#CDCTRG wire hits



Trigger rate and condition

present TRG status

-Status @ 2024/6/10

-**We almost achieved initial requirements !**
 -thanks to many efforts in LS1

new feature turned on:
 tighter prescale,
CDCTRG ADC, new 3D,
stt disabled

item	requirement	present status
Trigger rate	<30kHz @ L=6.0 × $10^{35}cm^{-2}s^{-1}$	~5.5kHz (~2.5kHz w/ new feature) @ L=3.8 × $10^{34}cm^{-2}s^{-1}$
Latency	4.4μs	4.4μs
Event timing resolution	10ns	~8ns
Efficiency	>99% for BB pair	>99% for BB pair **>95% for ττ pair** **dark search trigger**

Level1 trigger rate fraction @ 2024

-exp33run250, Total L1 rate=~7kHz, Luminosity=~3.5 × 10^{34}

-injection BG ~1kHz, storageBG,luminosity~6kHz

event triggered by upper bits are excluded in lower bits in table

Category	bit	Raw rate (kHz)	Exclusive rate (kHz)
CDC standard bits	ffy: #full track>=3, |z|<20cm fyo: #full track>=2, Δϕ>90deg, |z|<20cm	0.60 0.89	0.60 0.48
ECL standard bits	c4: #cluster>=4 hie: Energy sum>1GeV	0.40 1.36	0.21 1.03
KLM τ/dark	klmb2b, eklmb2b, beklm: Back to back sector hits cdcklm, seklm, ecleklm: #CDC-KLM, ECL-KLM matching>=1	0.46 0.45	0.40 0.22
CDC τ/dark	stt: #full track>=1, |z|<15cm, p>0.7GeV syo: #full track>=1, #short track>=1, Δϕ>90deg, |z|<20cm fy30: #full track>=2, Δϕ>30deg, |z|<20cm	1.91 1.21 1.16	0.93 0.43 0.07
ECL τ/dark	lml: several combination of #cluster and energy eclmumu: back to back low energy hit	2.92 0.63	1.65 0.01
Calibration	PID other (Bhabha, γγ, random, trg)	0.24 1.87	0.09 0.92
Total L1	OR of all bits	7.0	7.0

List of output bits: B physics

-Traditional condition same as Belle

2021c

Physics target	bit name	condition	Raw rate (kHz)	Exclusive rate (kHz)
BB pair	ffy fyo c4 hie	CDC #2track>=3, NNtrack>=1 with |z|<20cm >=1 CDC #2track>=2, NNtrack>=1 with |z|<20cm >=1, Δϕ>90deg ECL #cluster>=4, 2<=θid<=15 ECL Energy sum>1GeV, 2<=θid<=15	1.40 1.03 0.13 0.69	1.40 0.47 0.08 0.56

Expected efficiency of generic BB (MC)

BitName	eff(%)
fff	94.11
ffs	46.41
fss	15.18
sss	3.98
ffo	95.03
fso	1.34
sso	14,04
fzo	95.03
fyo	0

BitName	eff(%)
hie	95.11
lowe	99.79
lume	38.24
hade	38.24
c2	100
c3	100
c4	99.99
c5	99.98
ecloflo	98.34
eclbst	0
g_high	95.11

BitName	eff(%)
lml0	81.02
lml1	0.94
lml2	0.03
lml3	0
lml4	0.01
lml5	0
lml6	1.82
lml7	0.02
lml8	12.12
lml9	27.82
lml10	30.16
lml12	0
lml13	0

Trigger menu for dark/low-multi

-TRG-DAQ workshop 2022, physics-TRG session
-In backup, definition of conditions are shown.

Triggers

Analyses	triggers
Z' invisibile, dark Higgs	fy30, cdcklm, stt
Z'→$\tau\tau$, $\mu\mu$	fff/ffy, cdcklm,stt (fy30, fyo)
A' invisible (single γ)	hie, lml6, lml16 (lml1, prescaled)
A' visible without γ	stt, fyo, hie
X17/ A' visible + γ	dpee (lml,,hie, c2hie)
ALP→ $\gamma\gamma$ (3γ final state)	hie (high mass) , ggsel (low mass)
ALP→ $\gamma\gamma$ fusion (ee → $\gamma\gamma$ e)	lml2, hie (stt, lml1 barrel)
Single π^0/η/η' (ee → $\gamma\gamma$ e)	hie (stt)
$\mu\mu(\gamma)$ control sample (for invisible A' + …)	stt, beklm, cdcklm (fyo, syo)
IDM + Dark Higgs	hie (lml12, stt [stt4/5])
$\pi\pi\gamma$ for HVP	hie, (ff, stt)
$\pi\pi\pi^0\gamma$ for HVP	hie, bha3d (lml1)
Dark showers	stt, stt-ecl, hie for electrons (displaced VTX)

CDC
ECL
KLM

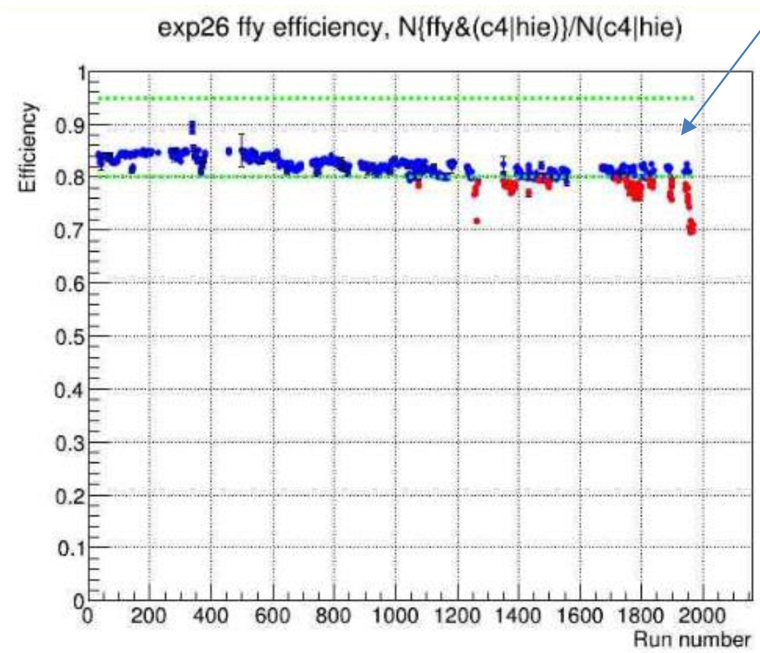
Triggers used now or in already planned extensions of analyses to the full dataset (and beyond)

Physics analysis

When you start physics analysis

-If your physics mode has high multiplicity, high efficiency is expected
  -we expect no need to take care trigger so much for your analysis

-Nevertheless, it is recommended to check trigger efficiency of data
  -In 2022, degradation of CDCTRG was seen by CDC gain drop, dead ch etc.
  -In 2024, active injection veto has been turned on.
  There might be impact on physics performance.



When you start physics analysis

-If your physics mode has low multiplicity, you should care trigger.

-0. contact trg-performance group to consult with it. Read Sphinx.

-1. choose high efficient trigger bit for your physics mode

-2. estimate trigger efficiency of your signal by using MC:

$$\epsilon = \frac{N_{\mathrm{ffy}}}{N_{\mathrm{all}}}$$

where N_{all} is the number of all generated events, and N_{ffy} is the number of `ffy` satisfied events

-3. check data/MC agreement with reference bit, independent from signal bit:

-because N_{all} can not be estimated by data

$$\epsilon_{\mathrm{exp}} = \frac{N_{\mathrm{fff}} \text{ and } (N_{\mathrm{hie}} \text{ or } N_{\mathrm{c4}})}{N_{\mathrm{hie}} \text{ or } N_{\mathrm{c4}}}$$

signal bit

reference bit

-4. apply correction and/or estimate systematics

When you start physics analysis

-Past documents to estimate trigger efficiency:

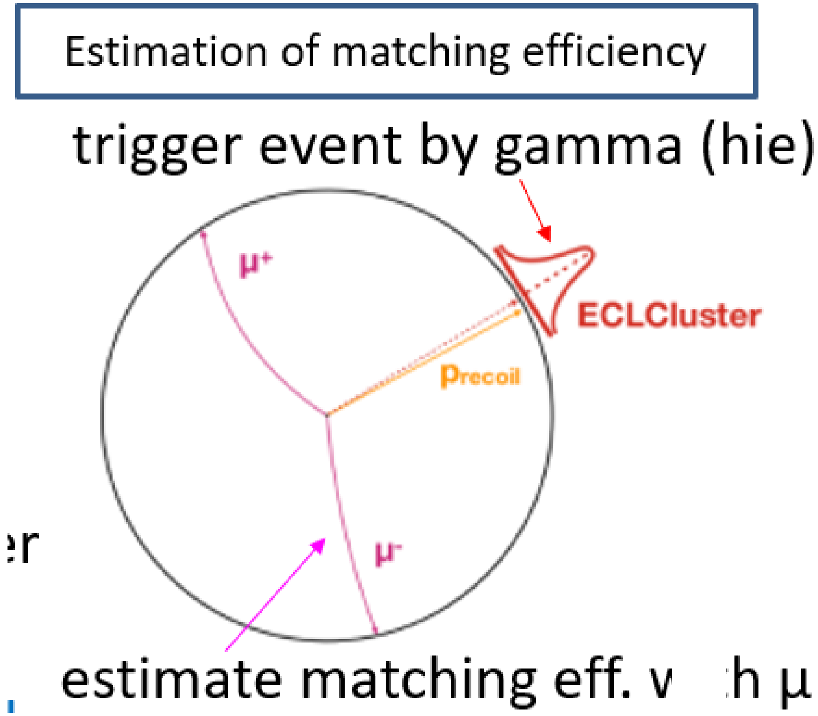
-mumu efficiency study: https://docs.belle2.org/record/4023/

-tau efficiency study: https://docs.belle2.org/record/1944?ln=en

-single photon efficiency study: https://docs.belle2.org/record/1972?ln=en

-Especially, μμγ is a good control sample to estimate trigger efficiency

-γ is triggered by ECL, μ can be used for study CDC,KLM (vice versa)



Trigger informatin on basf2

-On mdst, trigger information is stored on TRGSummary class.
Event variables are available for user. (Sphinx)

-$basf2 variables.py will show list of the available variables
  -ex. if L1PSNM(hie)==1, event is triggered by hie. if ==0, not triggered.

```
                              L1 Trigger
L1FTDL(name)            [Eventbased] Returns the FTDL (Final Trigger Decision
                        Logic, before prescale) status of the trigger bit with
                        the given name.
L1Input(name)           [Eventbased] Returns the input bit status of the trigger
                        bit with the given name.
L1PSNM(name)            [Eventbased] Returns the PSNM (Prescale And Mask, after
                        prescale) status of the trigger bit with the given name.
L1Prescale(name)        [Eventbased] Returns the PSNM (prescale and mask)
                        prescale of the trigger bit with the given name.
```

-Example of implementation on your steering file

```
tools =  ['L1FTDL(hie)']
tools+=  ['L1FTDLBit(c4)']
tools+=  ['L1FTDLBit(ffy)']
tools+=  ['L1FTDLBit(fyo)']
output = register_module('VariablesToNtuple')
output.param('variables', tools)
output.param('treeName', 'tree')
main.add_module(output)
```

-※With run-independent MC, prescale configuration and trigger menu can be different from data. Please be careful.

Summary

-Introduce trigger

- -various importance with various experiments
- -hardware(FPGA) and/only software(computer) trigger for collider

-Belle II trigger

- -CDC, ECL, KLM, TOP with ϕ matching
- -Unique logics on FPGA
- -Many trigger conditions with B, τ and low multi physics

backup

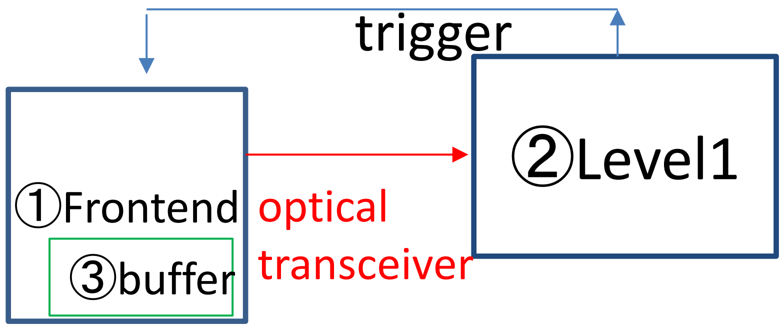
Optical transceiver technology

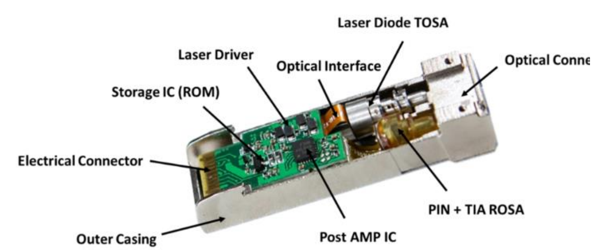
-Optical transceiver performance has been in improved recent ~20years

-~2times bandwidth in each 3~4 years !!

-Trigger performance has been improved accordingly

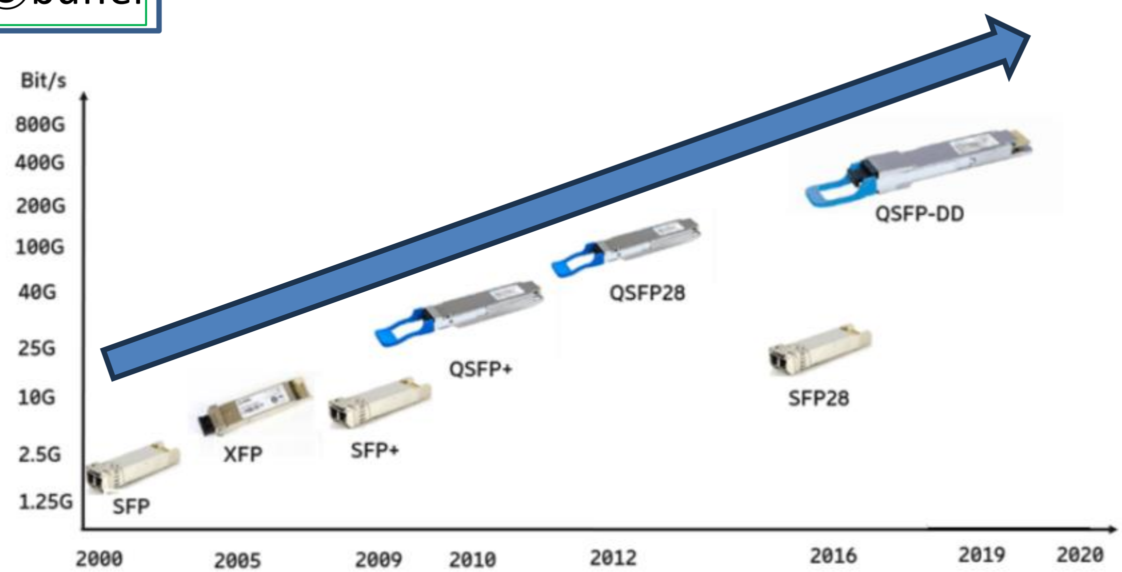
-receive detailed data from detector frontend



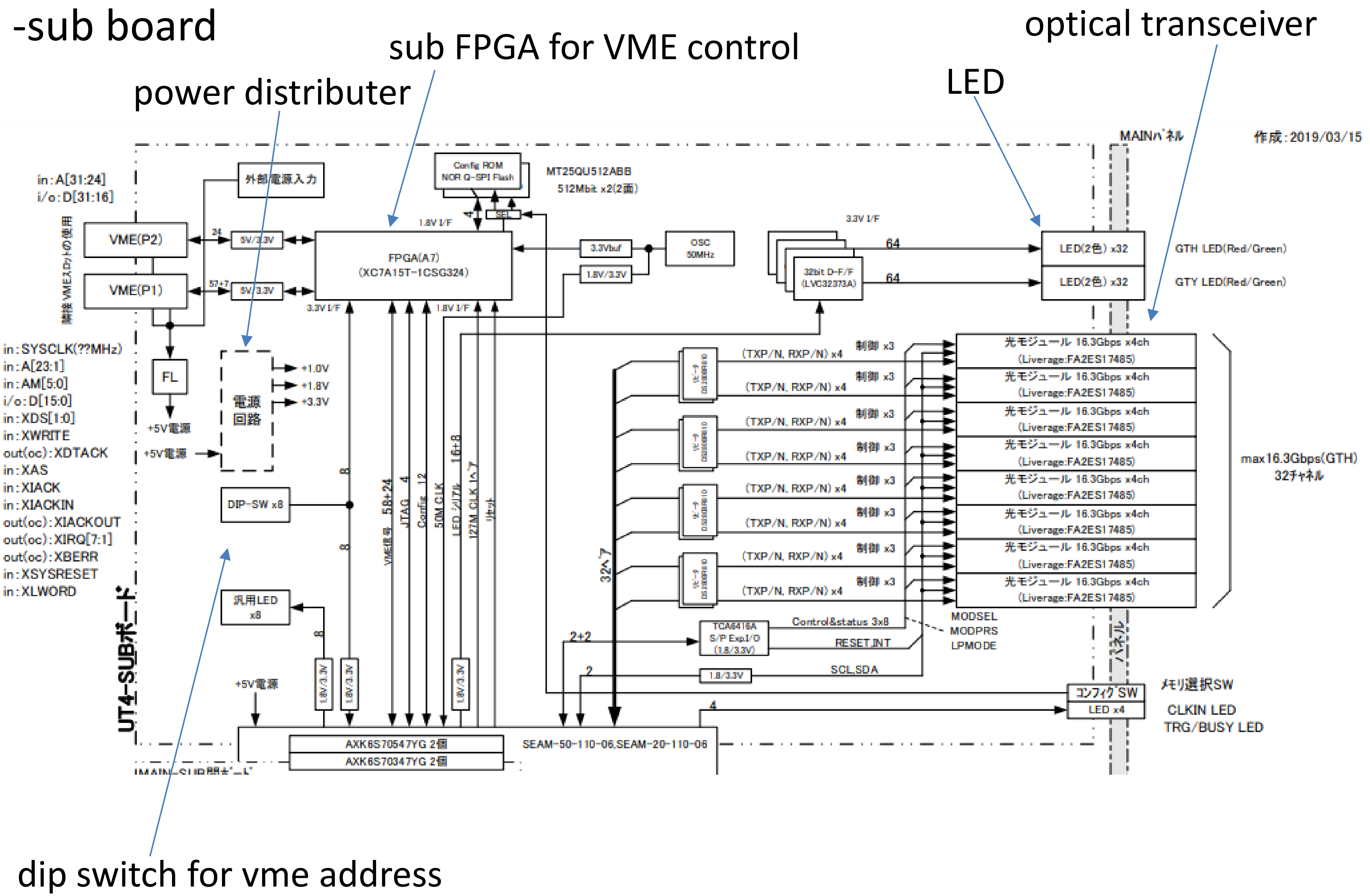


Product Teardown Image of an Optical Transceiver

(Source)

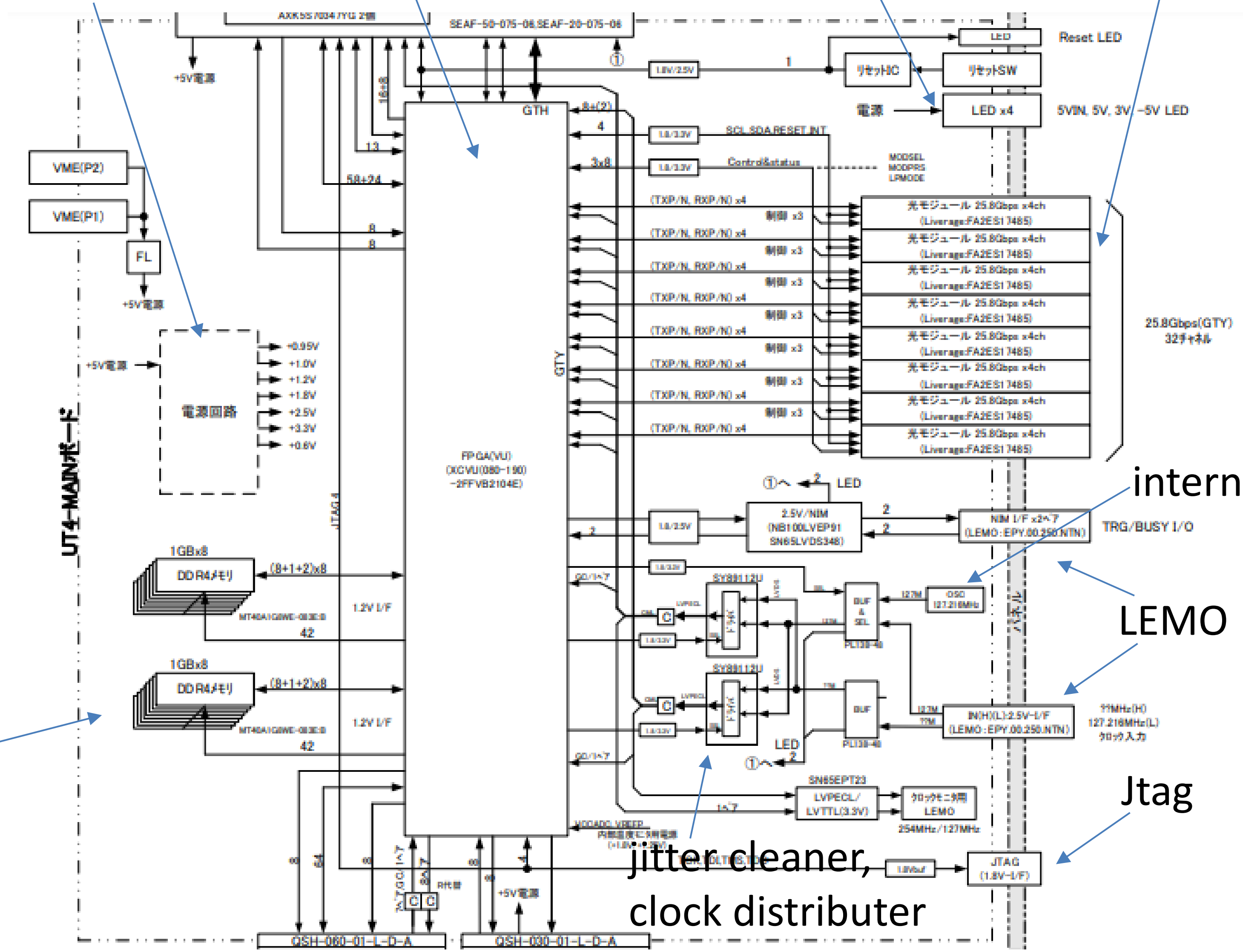


Universal Trigger board



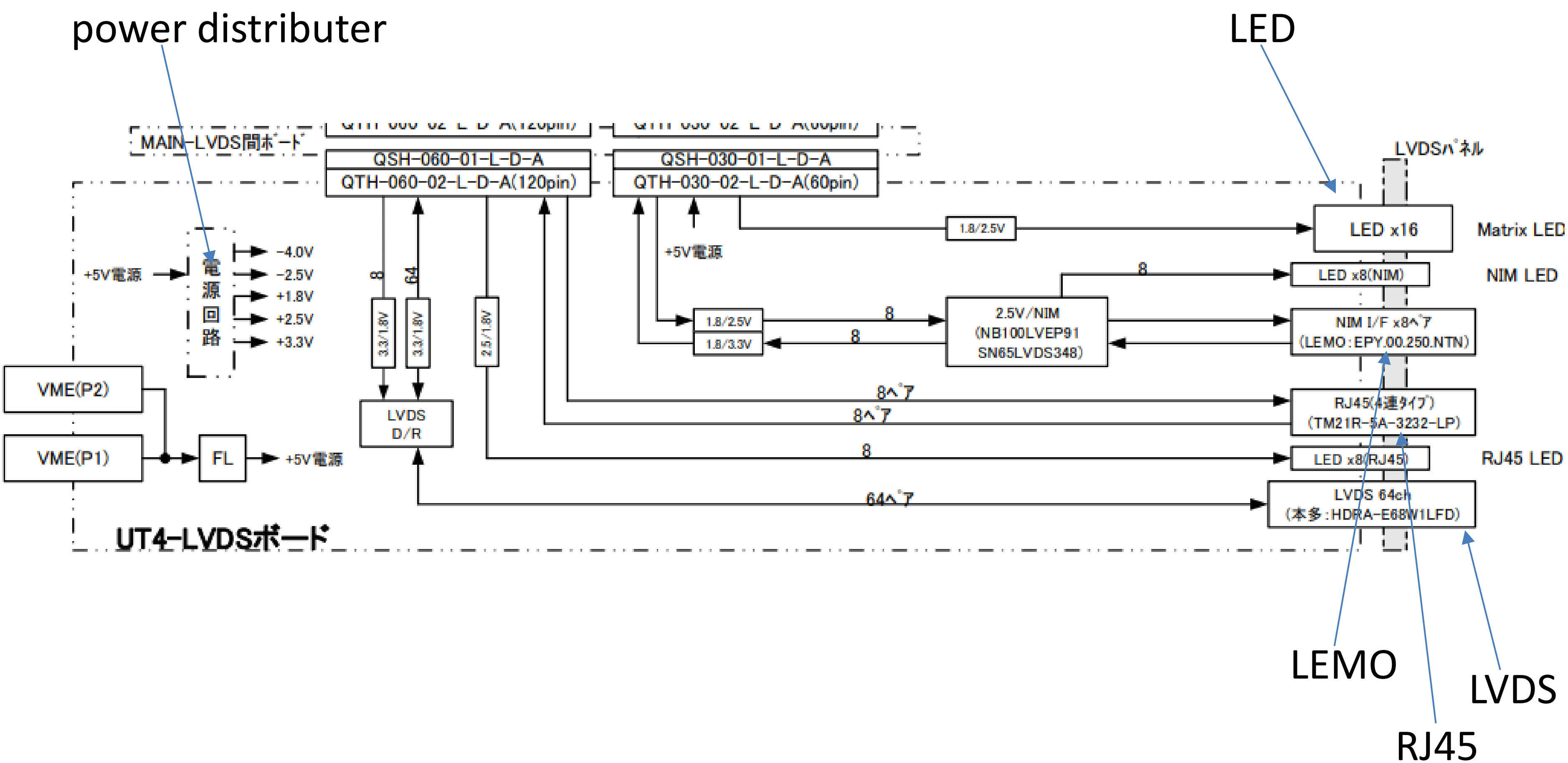
Universal Trigger board

-main board



Universal Trigger board

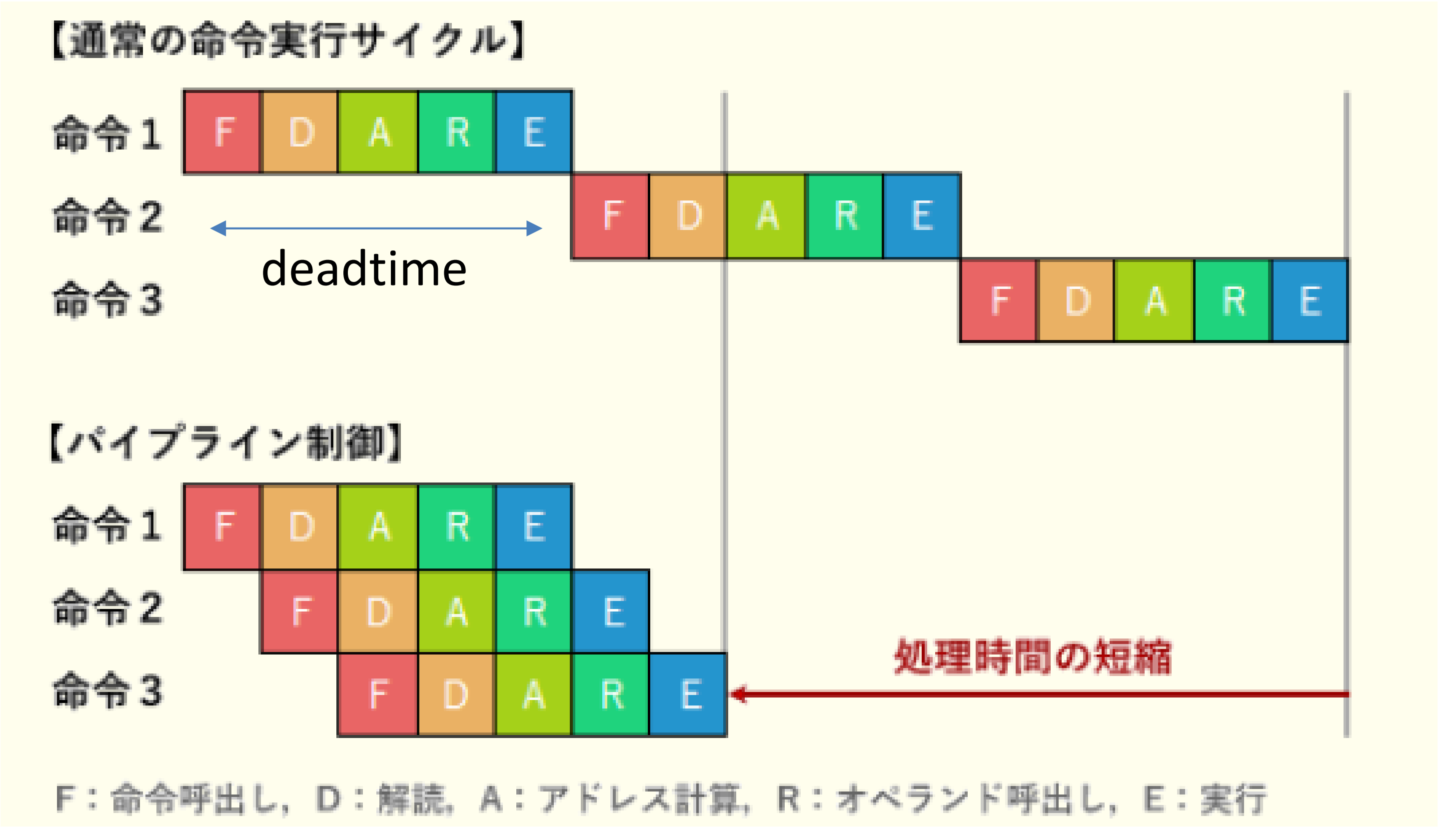
-LVDS board



Pipeline processing

-"Pipeline processing" is used for all logic to achieve no deadtime requirement

-All Belle II trigger logic is implemented by using the pipeline processing
  -...except for KLM/TOP Merger



no deadtime

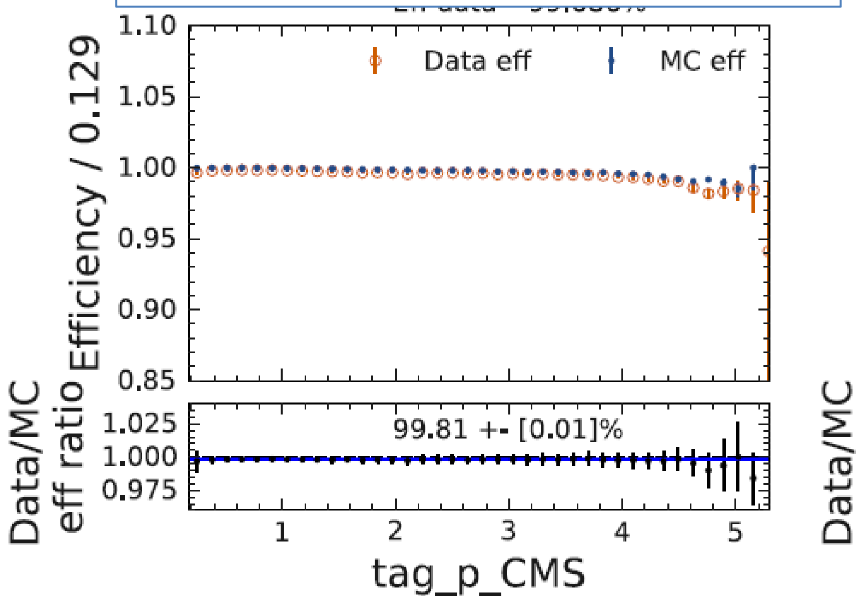
TSIM

-Trigger logic is simulated on basf2 software, in order to estimate trigger efficiency of signal and background. (Trigger simulation, TSIM.)

-Since MC14, most of trigger logic has been implemented with good data/MC agreement

-Example of tau 1x1 study

ECLTRG efficiency with tau 1x1, electron mode



Systematics of TRG for tau 1x1 analysis

Sys	e	μ
Data-MC	0.05	0.05
Ref trig	0.11	0.34
Exp dep	0.13	0.26
Total (%)	**0.124**	**0.437**

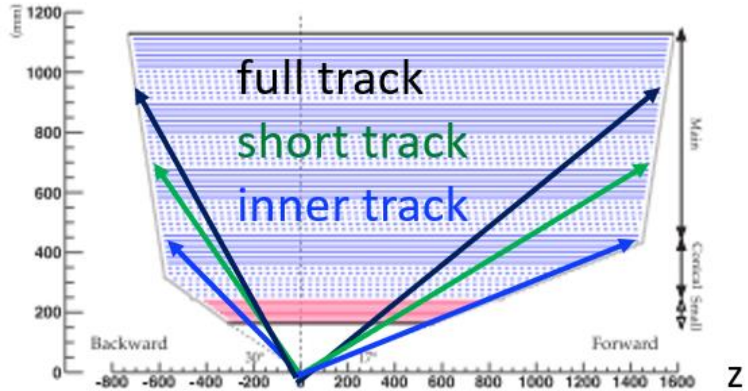
CDC trigger: inner track, short track

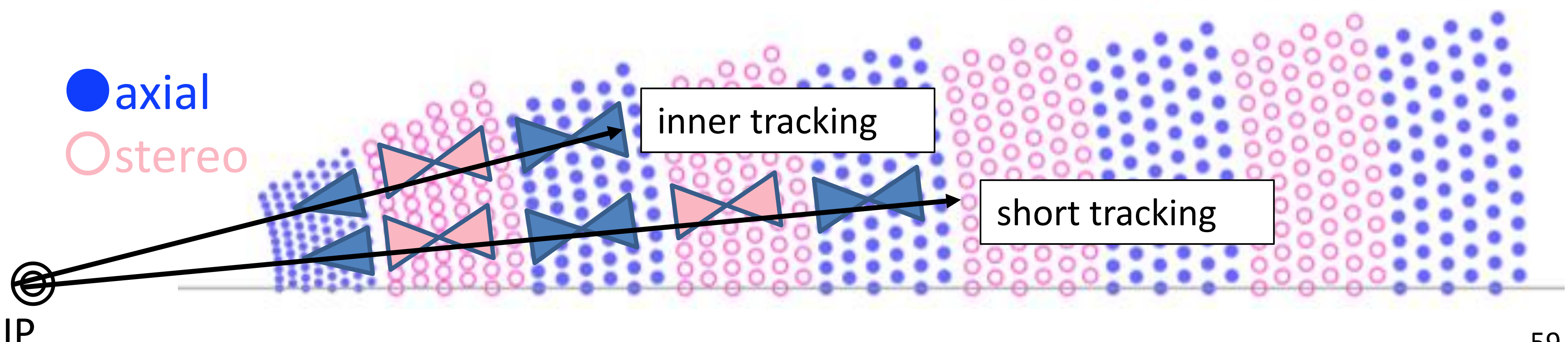
-Short(inner) track is reconstructed with coincidence of 5(3) TSFs on GRL

- -short: Look up table is made to search required ϕ pattern
- -inner: just require three TSFs in ±4 wire in ϕ

-Not initially planned at Belle II but added since 2020

- -large θ acceptance for low multi physics and two photon
- -no z measurement: high trigger rate

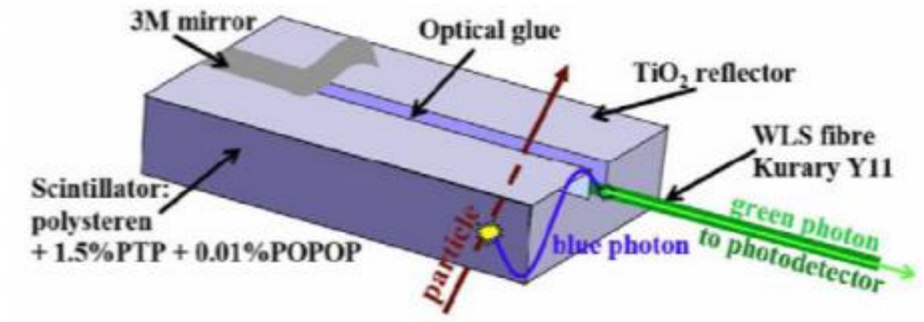




KLM

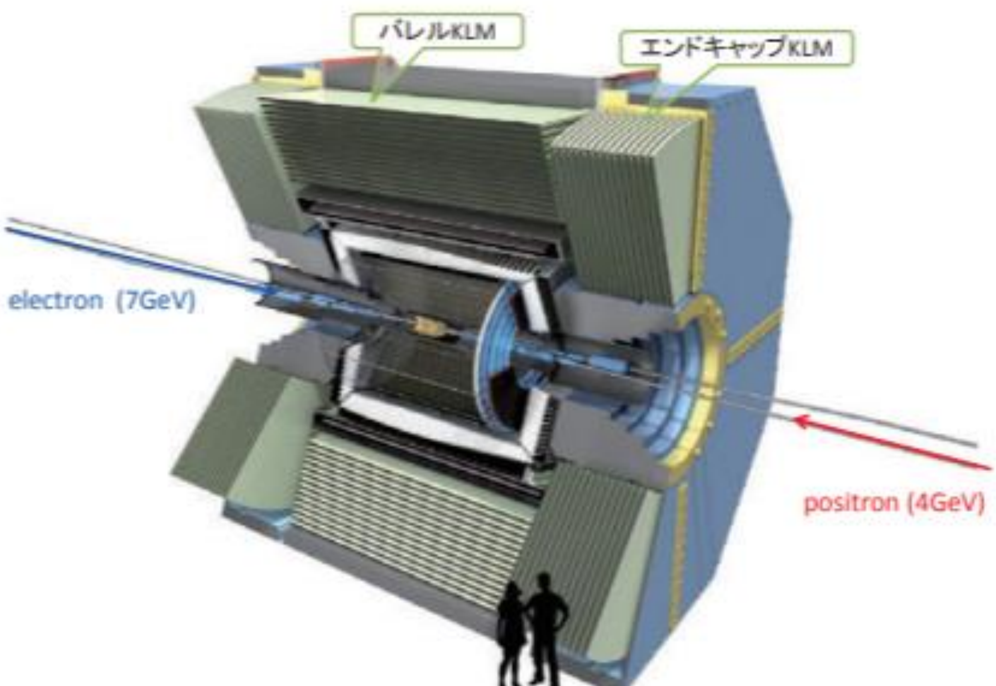
-KLM:KL/μ検出器

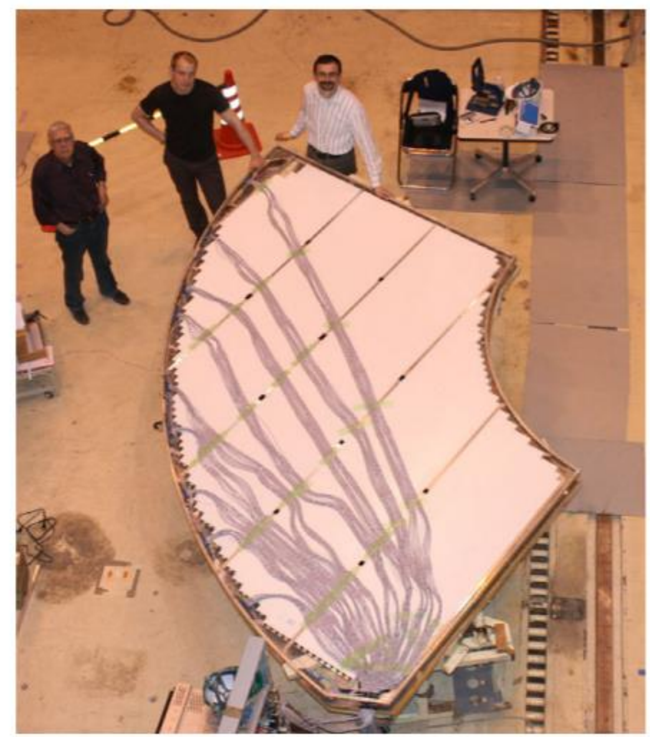
- -μの同定
- -K_L^0の検出



-鉄+プラスチックシンチレータ or RPCのサンドイッチ構造×15

-BelleII でendcapとbarrelの一部をプラシンへ交換
(放射線による不感への耐性)



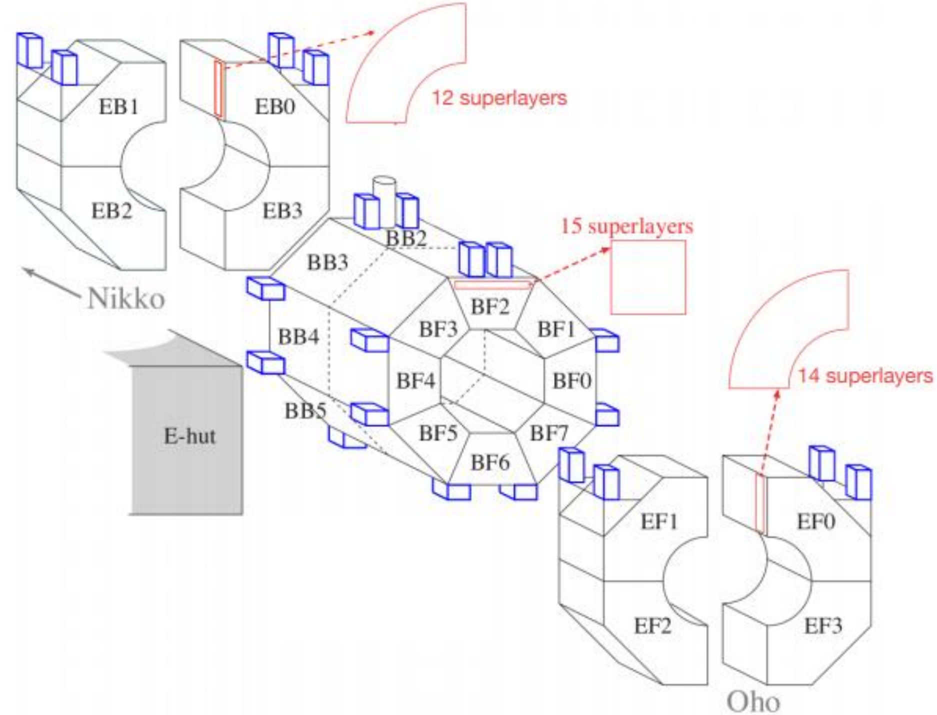


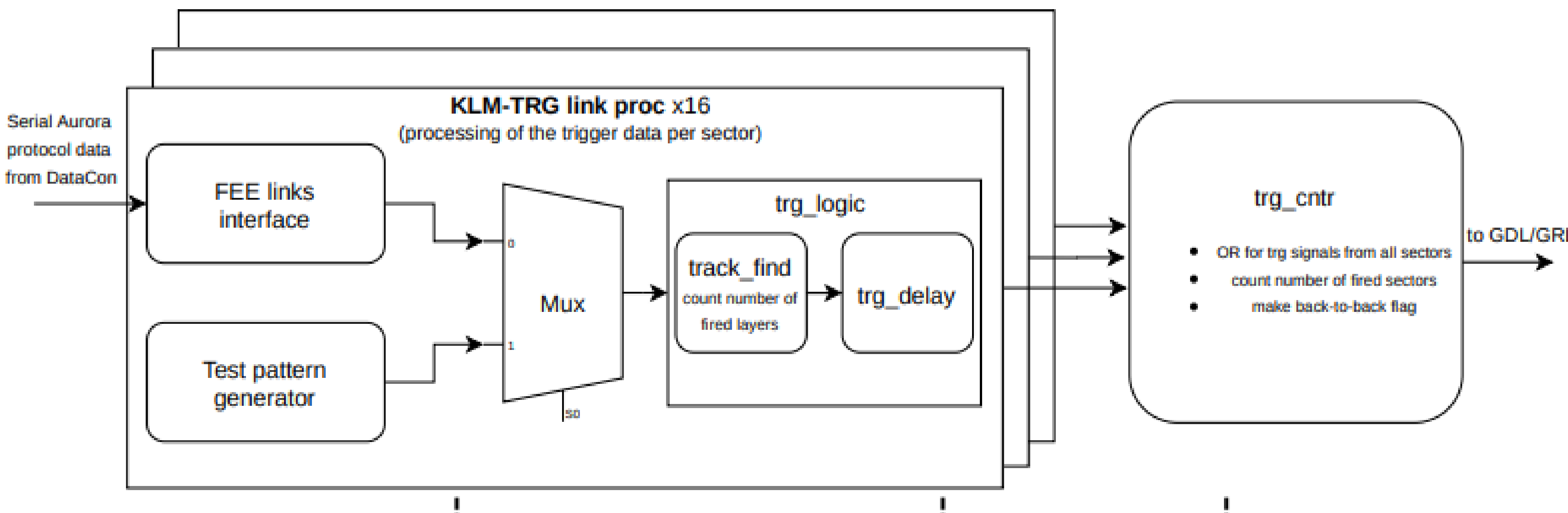
KLM Trigger

-Search muon in each sector

-Simply count number of hits:
if #hit>7, it is judged as muon

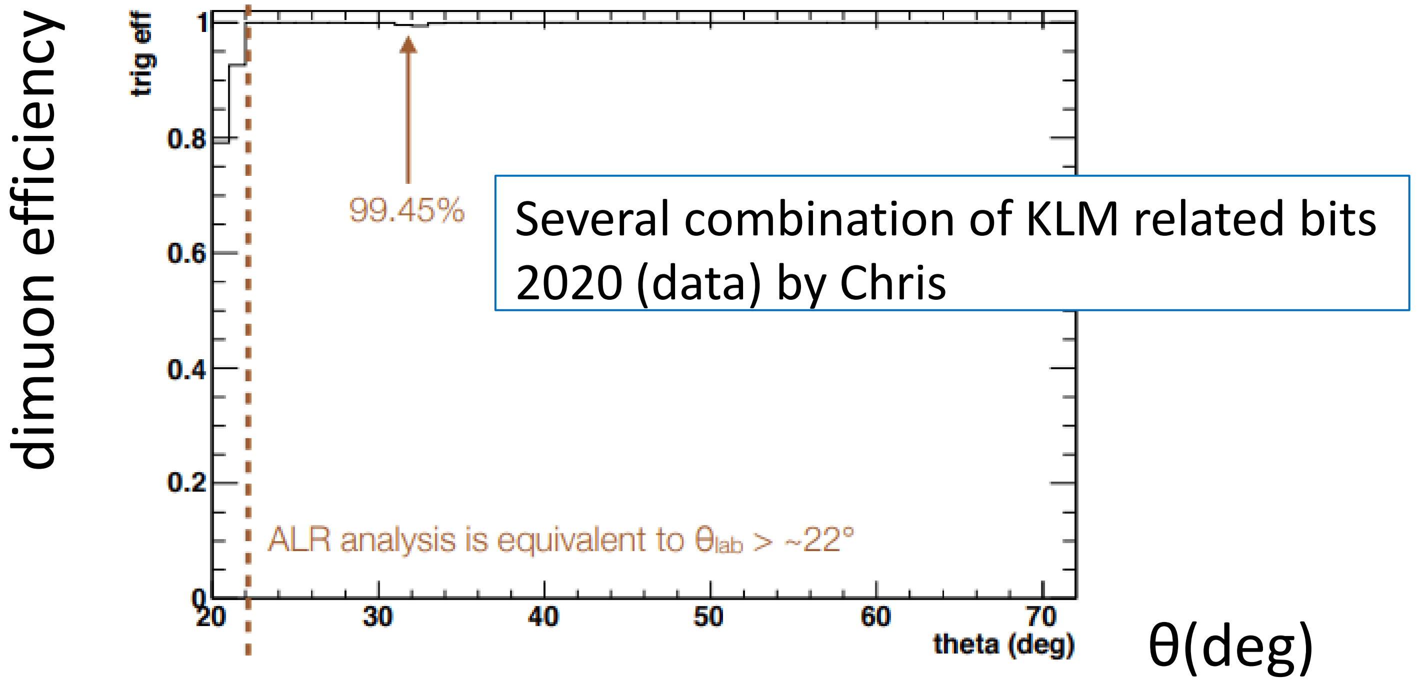
-Tracking development is on-going





Dimuon efficiency performance

-High efficiency for Dimuon with wide angle coverage



Event timing determination

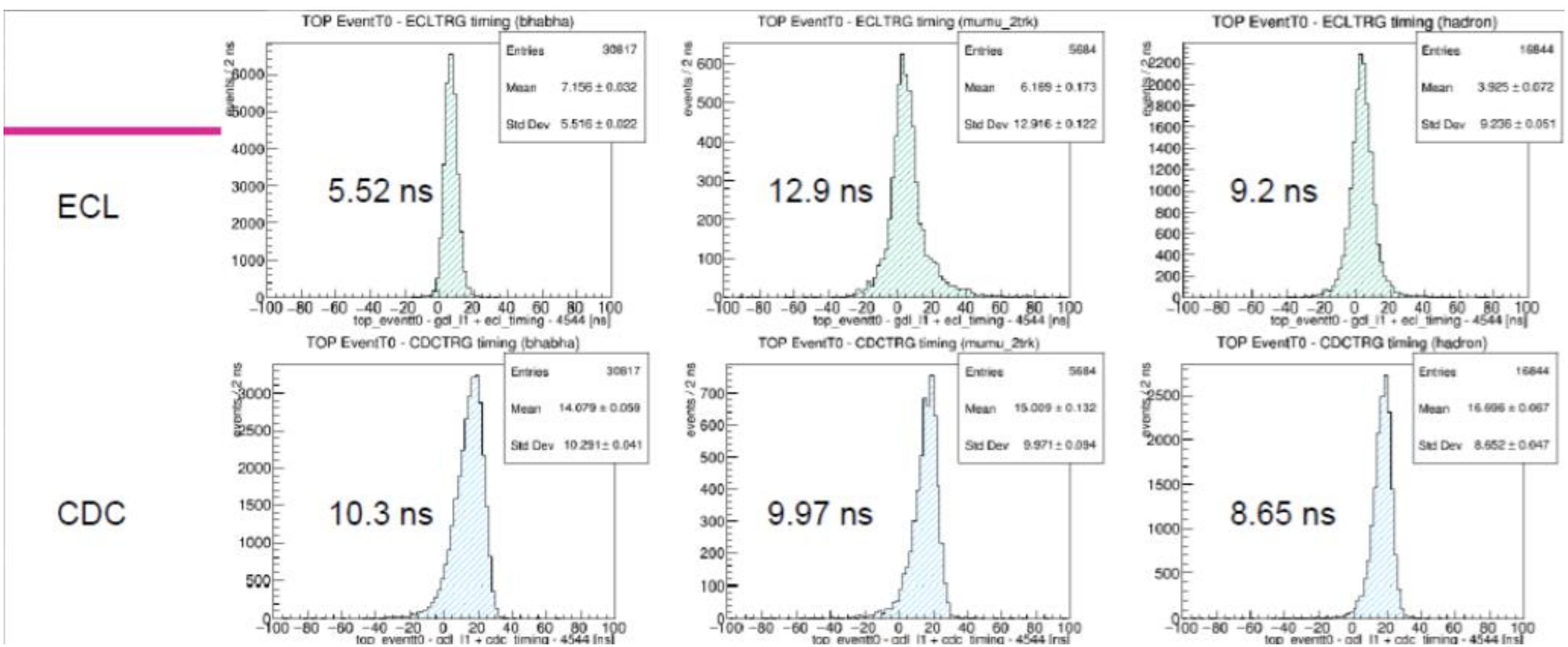
-Trigger timing is determined by ECLTRG, CDCTRG, TOPTRG

- -ECLTRG: timing of the highest energy TC
- -CDCTRG: median of the fastest timing of TS associated with 2D track
- -priority: ①ECLTRG ②CDCTRG ③TOPTRG

-Better timing resolution than requirement of 10ns

Event timing resolution

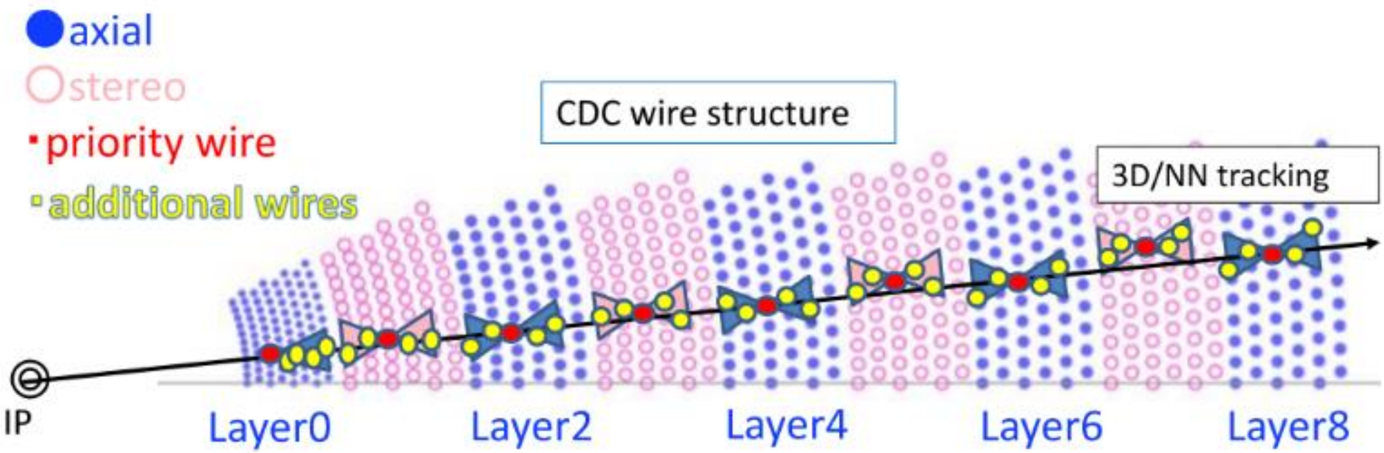
Bhabha μμ hadron



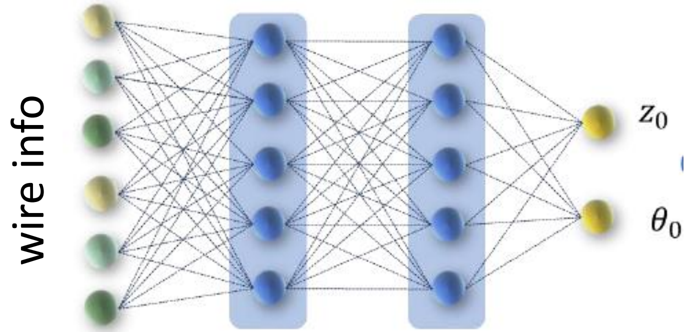
Short term upgrade

-advanced trigger logic to reduce background trigger rate

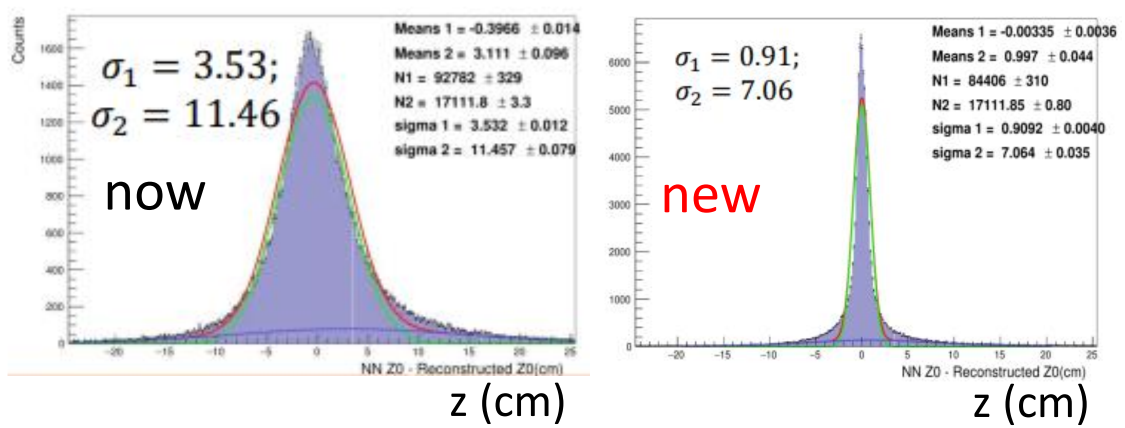
- -new FPGA(UT4,UT5) to improve CDCTRG tracking, by using all wire hits
- -new tracking algorithm (deep learning, high level Hough transformation)



Deep learning 3D tracking



comparison of z resolution



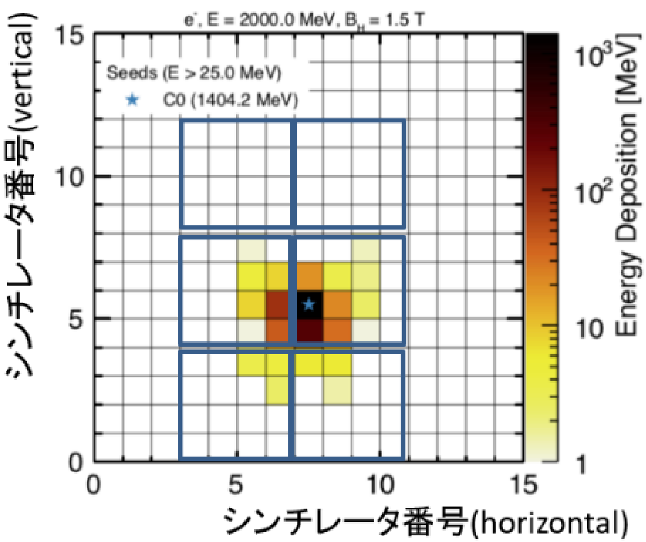
Long term upgrade

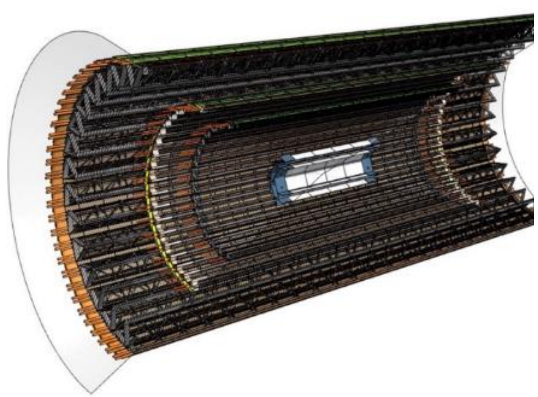
-Upgrade trigger with Detector upgrade

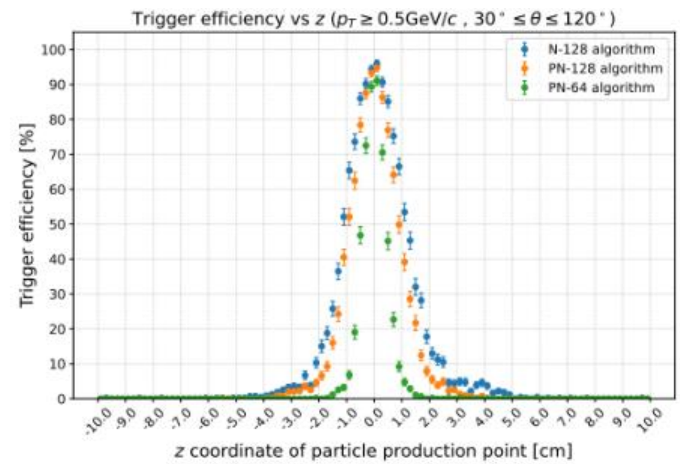
- -new CDC frontend board (~2026): send TDC and ADC of all wires
- -new ECL readout board (long shutdown 2？): read Crystal one by one
- -new VXD (long shutdown 2 ?): implement VXD trigger functionality

□ 従来の読み出し(4x4本)

□ 新読み出し(1本)







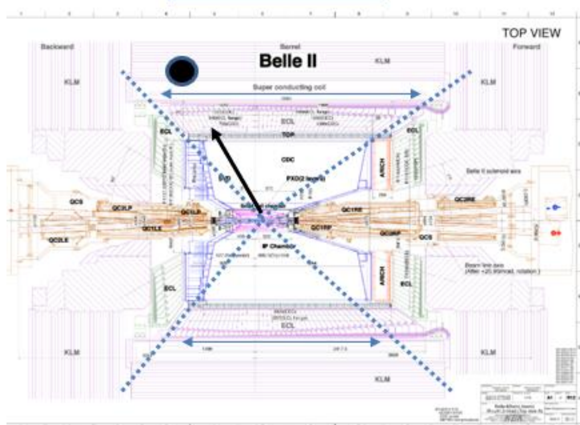
List of output bits: muon

-CDC-KLM, ECL-KLM matching trigger

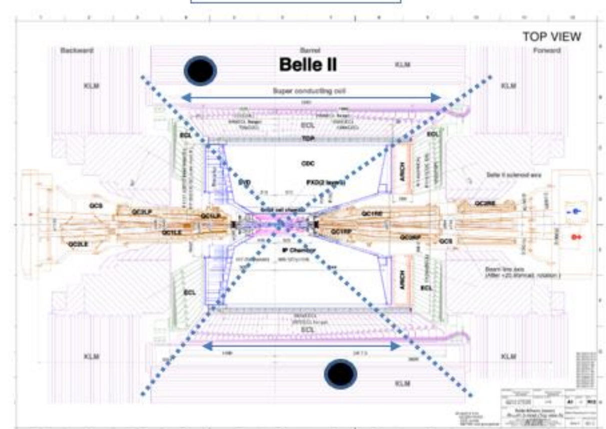
Physics target	bit name	condition	Raw rate (kHz)	Exclusive rate (kHz)
Single muon	cdcklm1-2	#CDC-BKLM matching>=1	0.27	0.15
	ecleklm1	#CDC-EKLM matching>=1	0.42	0.30

Physics target	bit name	condition	Raw rate (kHz)	Exclusive rate (kHz)
Muon pair	mu_b2b	#BKLM cluster>=2, $\Delta\phi$>90 deg.	0.35	0.32
	eklm2	#EKLM cluster>=2	0.04	0.04
	beklm	#EKLM cluster=1, #BKLM cluster=1	0.20	0.18
	lml10	ECL 160 <$\Delta\phi_{CM}$< 200 deg, 160 < $\Sigma\theta_{CM}$ < 200deg, no 2GeV(CM) CL in an event	0.49	0.36
	eclmumu	ECL 160 <$\Delta\phi_{CM}$< 200 deg, 165 < $\Sigma\theta_{CM}$ < 190deg, E<2GeV	0.30	-

cdcklm1



mu_b2b

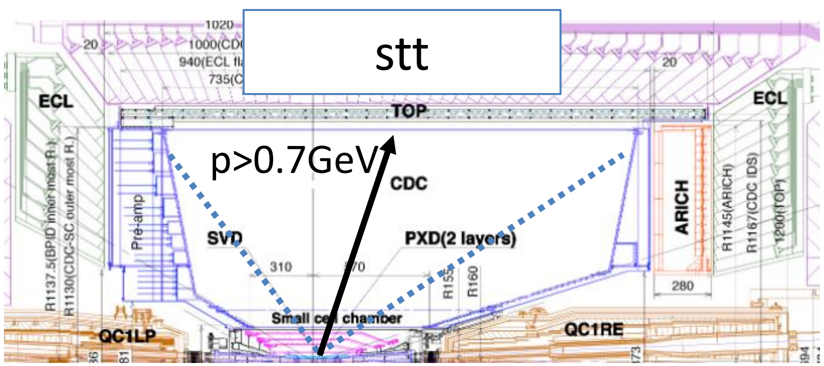


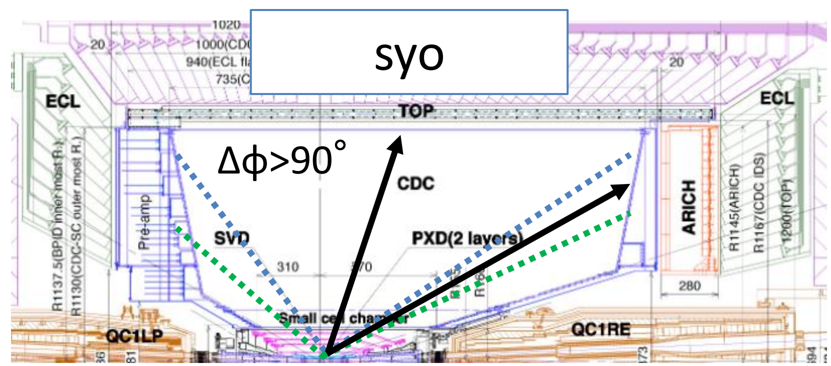
List of output bits: τ

-CDC-KLM, ECL-KLM matching trigger

2021c

Physics target	bit name	condition	Raw rate (kHz)	Exclusive rate (kHz)
τ	stt	CDC #full track>=1, |z|<15cm, p>0.7GeV	1.74	0.96
	syo	CDC #full track>=1, |z|<15cm, #short track>=1, Δϕ>90deg.	0.74	0.38
	yioiecl1	CDC #full track>=1, |z|<15cm, #inner track>=1, Δϕ>90deg.	0.37	0.08
	lml12	NCL ≥ 3, at least 1 CL ≥ 500 MeV(Lab)) (with θID = 2 - 16)	0.17	0.03
	ecltaub2b3	under commissioning	-	-



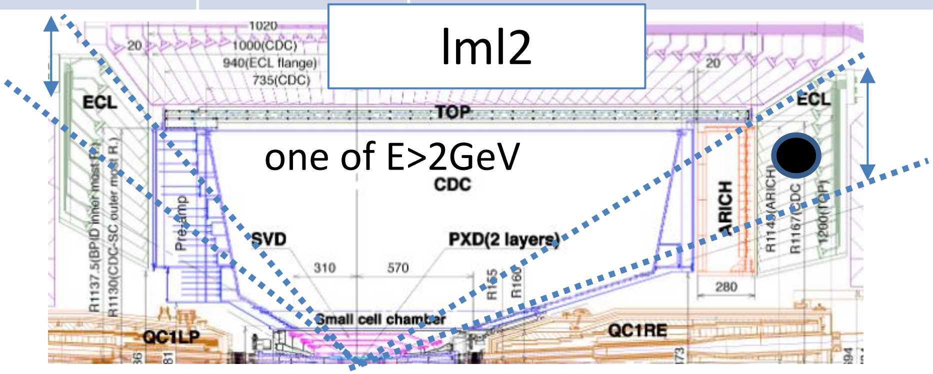


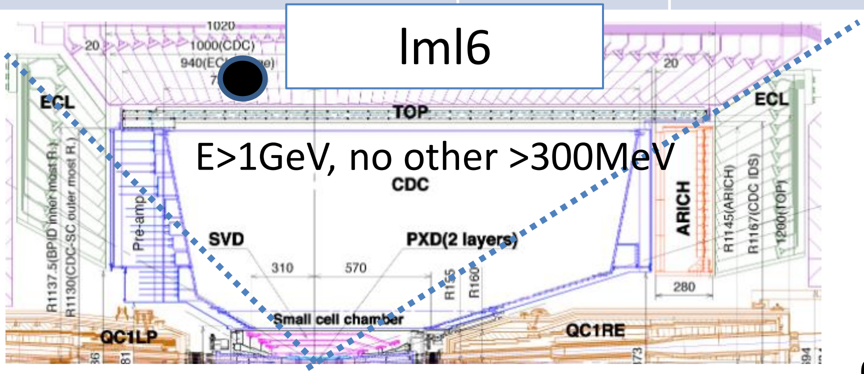
List of output bits: lowmulti/dark

-Mainly ECL based photon trigger

2021c

Physics target	bit name	condition	Raw rate (kHz)	Exclusive rate (kHz)
Z’	fy30	CDC #full track>=2, Δϕ>30deg, #|z|<20cm >=1	1.59	0.14
ISR,π0 FF	lml2	ECL one CL ≥ 2 GeV(CM) with θID = 2, 3, 15 or 16	0.18	0.01
single γ	lml6	ECL only one CL ≥ 1 GeV(CM) with θID = 4 - 15 and no other CL ≥ 300 MeV(Lab) anywhere	0.18	0.03
single γ	lml7	ECL only one CL ≥ 1 GeV(CM) with θID = 2, 3, or 16 and no other CL ≥ 300 MeV(Lab) anywhere	0.15	0.04
ALP	lml8	ECL 170° < ΔϕCM< 190° , both CL > 250 MeV(Lab), no 2GeV(CM) CL in an event	0.08	0.05
ALP	lml9	ECL 170° < ΔϕCM< 190° , one CL < 250 MeV(Lab), one CL > 250 MeV(Lab), no 2GeV(CM) CL in an event	0.34	0.28
dark photon	lml16	ECL only one CL ≥ 0.5 GeV(CM) with θID = 6-11 and no other CL ≥ 300 MeV(Lab) anywhere, #CDC full track==0	0.32	0.23





Change of prescale

List of high-rate physic trigger bits

discarded bit name	alternative bit name	Change of logic	Raw rate reduction (kHz)	Exclusive rate reduction (kHz)	Physics target
stt	sttecl	apply CDC-ECL matching	2.0->1.0	1.0->0.4	tau
cdcklm seklm	ycdcklm ecleklm	require NN track	1.1->0.53	0.83->0.36	single μ(barrel) single μ(endcap)
syo, syb	syoecl, sybecl	apply CDC-ECL matching	1.8->0.40	0.46->0.10	tau, PID
yioiecl1	--	disable	0.5->0	0.3->0	endcap two track
hie	hie3	additional Bhabha veto to endcap	2.0->1.2	1.5->0.8	B, τ, single photon with E>1GeV
lml2	--	prescale by 10	0.61->?	0.34->?	γ with wide θ range
lml7	--	disable	0.38->0	0.25->0	single photon sideband
lml9	--	disable	0.67->0	0.49->0	ALP
lml10	eclmumu	acceptance affected	1.1->0.63	0.70->0.51	μμ
lml13		disable			
lml16	--	prescale by 10	1.0->0.1	0.66->0.6	single photon with E>0.5GeV

CDC-ECL matching

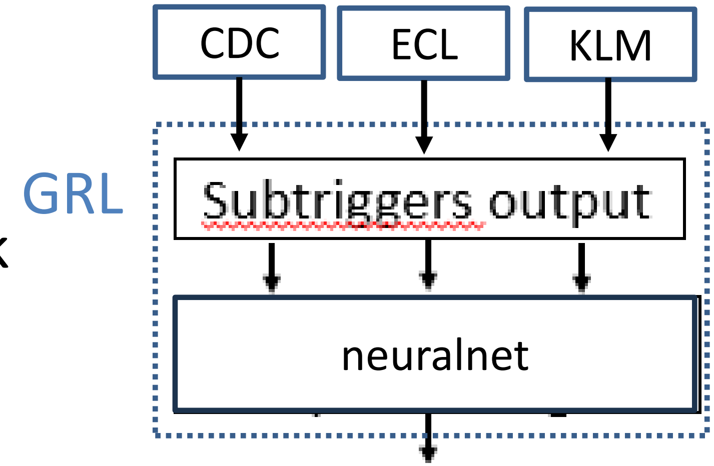
new Bhabha veto

GRL

-GRL: Global reconstruction logic

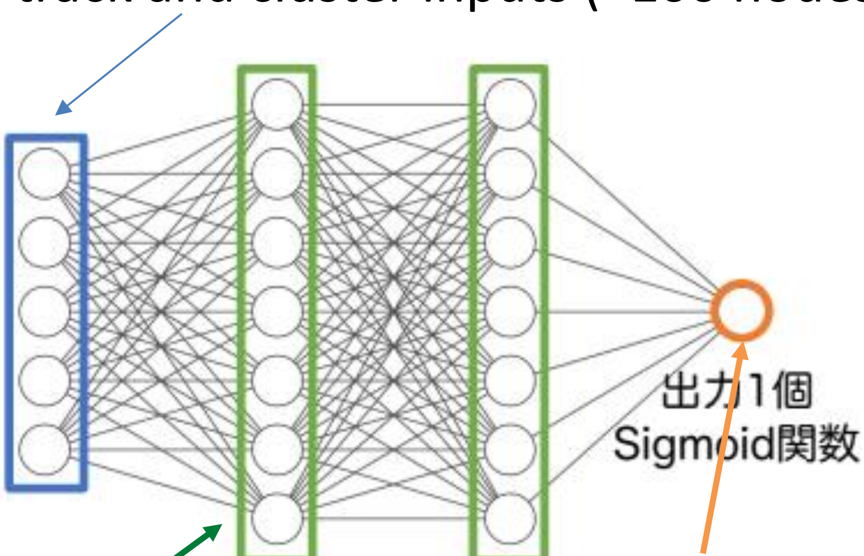
-take ϕ matching of CDC/ECL/KLM/TOP

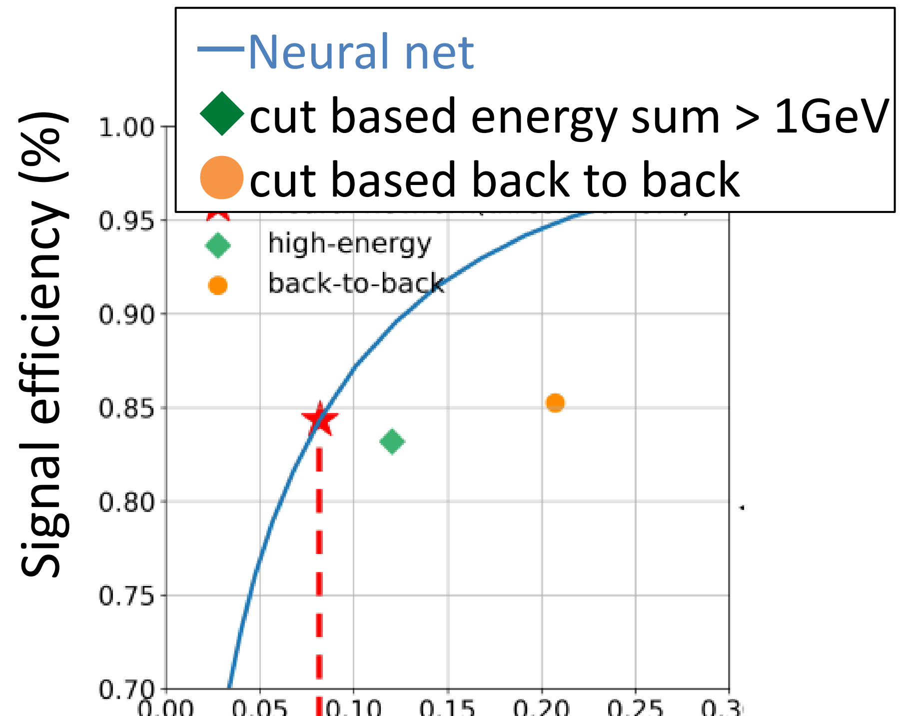
-event classification by using neural network



CDCTRG,ECLTRG,KLMTRG

track and cluster inputs (~100 nodes)





hidden layer

hidden layer (1 node)

TSIM

- -TSIM has been developed and can be used for physics analysis
  - -KLMTRG core logic modified with release06 to be consistent with firmware
  - -most of trigger bits are implemented with release06
  - -~5% data/MC agreement for signal efficiency estimation (tau)

- -Useful links
  - -Available and missing trigger bits in TSIM release05
  - -How to generate signal MC with release06
    - - example code
    - - release-06-00-05 or later with global tag of "L1_config_exp_22_run_290"

- -Available event variables
  - -L1FTDL(name),L1FTDLBit(bitnumber) returns if the output bit satisfied w/o prescale.
  - -L1PSNM(name),L1PSNMBit(bitnumber) returns if the output bit satisfied w/ prescale.
  - -L1Input(name),L1InputBit(bitnumber) returns if the input bit satisfied
  - -source code: analysis/variables/src/TriggerVariables.cc

- -Make Jira ticket and notify us if you have any TRG software request ☺