

Polarized Source Development Update

CsTe thin-film heterojunction development

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2/26/2025 B2GM

1 . 2024-5 Winter Experiments

- Following procedure of Cultrera [citation], we have tried adjusting the procedure for CsTe cathode production.
 - Cathode preparation updated:
 - Wet etching method changed from SemicoClean to HCl
 - Increased cathode baking (temp + time)
- Also repaired thin-film deposition monitor and WL splitter control via LabView

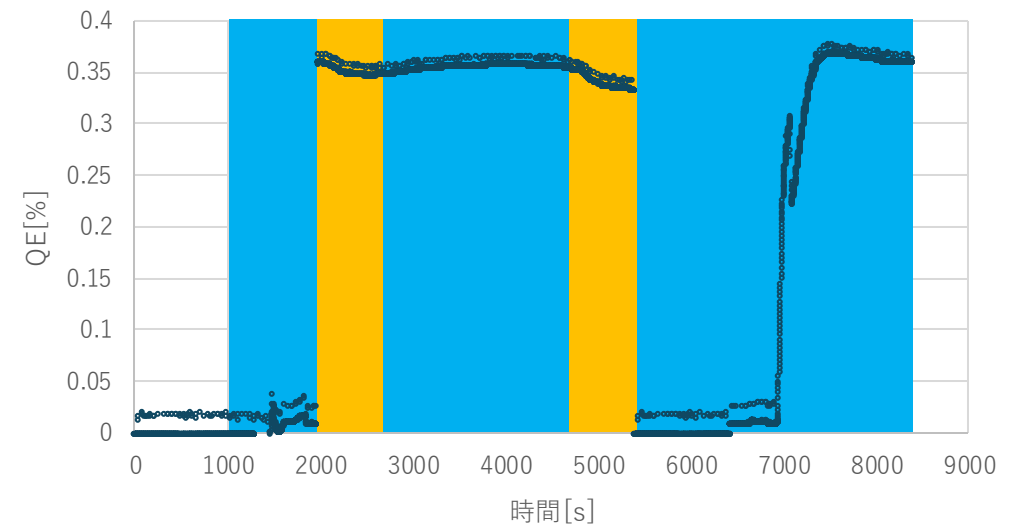
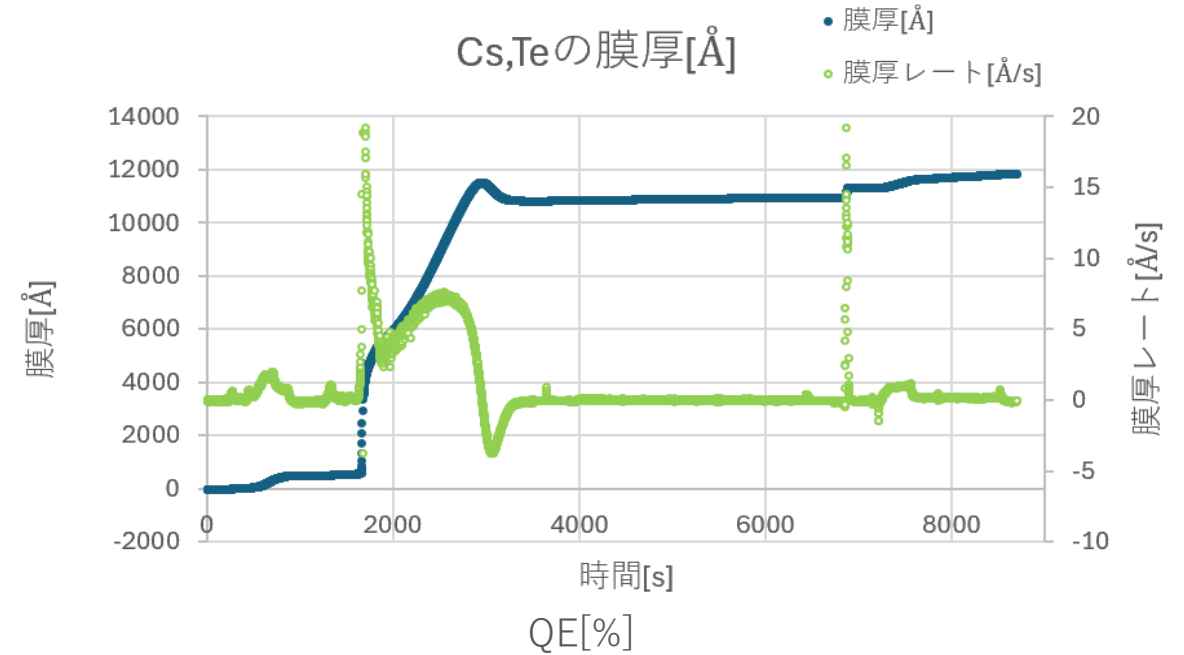
2. Procedure

- Cathode Prep:
 - Wet etching of GaAs cathode with 4% HCl solution (5')
 - Indium solder onto base and insertion into vacuum chamber
 - Nitrogen flush of chamber interior followed by baking ($\sim 200^\circ$) for 72-96 hours
 - Cathode annealing performed at ~ 400 - 500° for 12 hours
 - Had previously been at lower temp. for less time
- Cs deposit on cleaned cathode face to demonstrate viability
- Thin layer of Te followed by Cs, followed by another thin Te layer and final Cs deposition
- QE measurement: 532 nm, 780 nm laser; 300-900 nm spectrum (Xe lamp)

4. Deposition

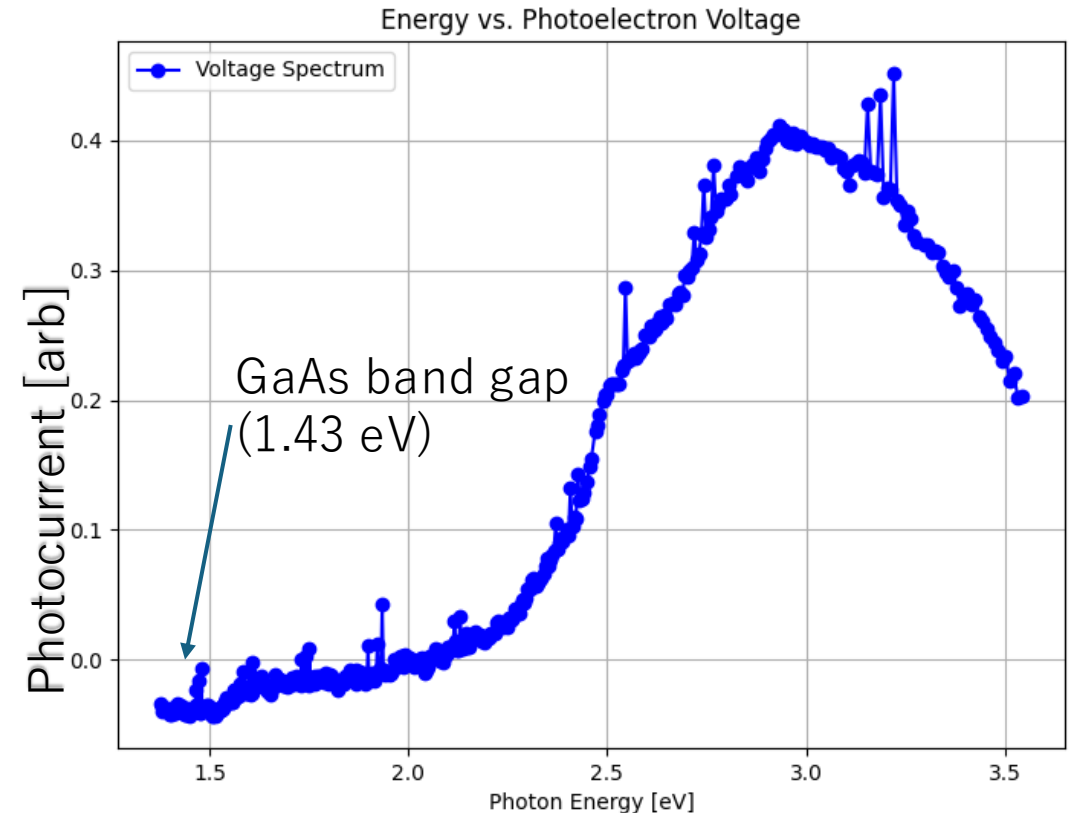
Deposition carried out under illumination of 5 mW 532 nm laser at ambient temperature ($\sim 30^\circ$)

- Initial Cs deposition:
 - dispenser put out a brief spike of Cs vapor that remained in the chamber longer than expected. QE measurement confirmed to saturation.
- Te deposition:
 - Initial deposition didn't show initial QE drop despite monitor showing deposition. Possibly interference from residual Cs in the chamber?
 - Second Te deposition showed the expected QE drop
- Further Cs showed return to saturation.



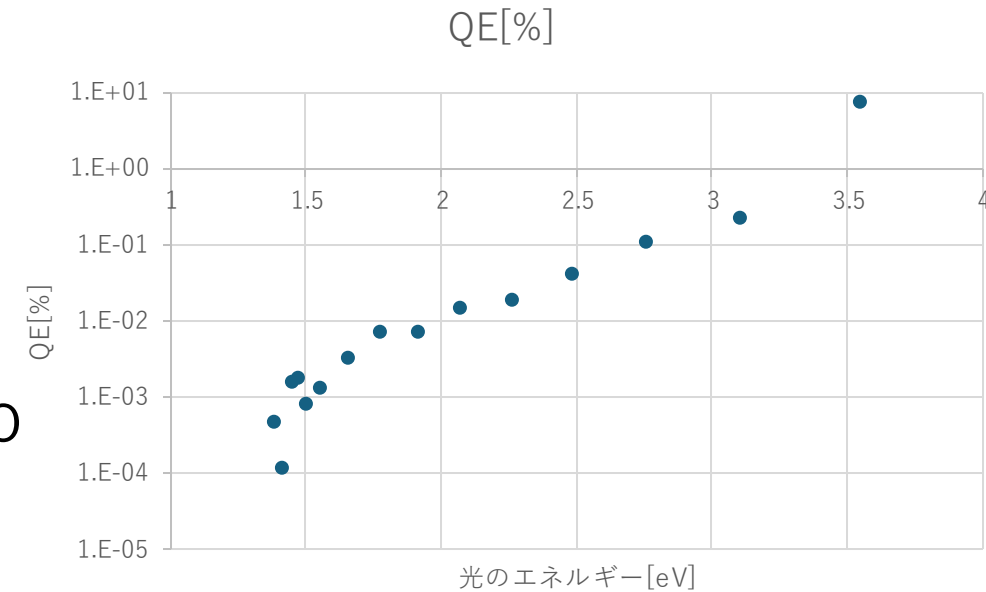
5. Results: Raw Spectrum

- Despite the thick layer of Cs and (possibly?) Te, cathode showed QE across the spectrum from 300-780 nm
- Raw photocurrent response shown at right
- Peak shown in UV, falling off at lower photon energies



6. 350~900nm QE spectrum

- QE at the GaAs band gap (1.43 eV) measured at the order of $10^{-3}\%$
- Shorter WL's showed increasing QE to the $\sim 1\%$ level



7. Conclusions and Future Work

- Excessive Cs (and Te?) deposit early still showed a QE response consistent with GaAs NEA activation.
 - Reproduction of results with improved control of Cs deposition to confirm this result.
 - Thickness of 1st Te layer unclear – how much of the measured deposition came from residual Cs vapor is difficult to say.
- Measure the effect of the Te base layer thickness on the cathode QE response
 - Similar study to be done with Sb

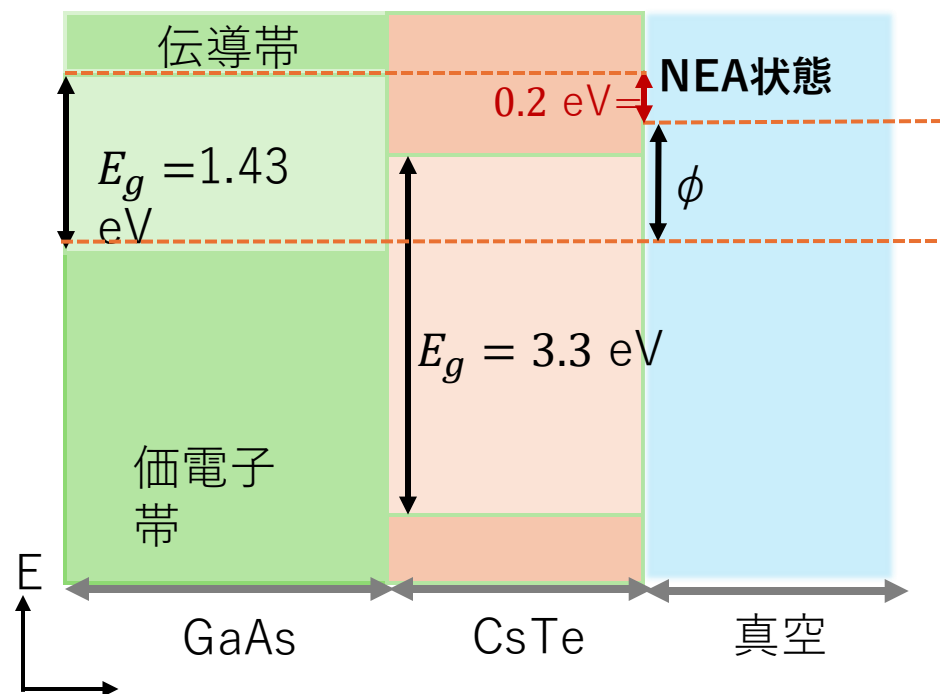
- BACKUP MATERIAL

2. ヘテロ接合によるNEA-GaAsフォトカソード

- ・ **NEA-GaAsフォトカソード** : GaAs半導体表面に真空条件でCs と酸素を蒸着したもの
Cs-O蒸着は耐久性が低い
→Cs-Te, Cs-K-Te, Cs-K-Sbなどを蒸着すると耐久性の高いNEA表面を作れることが発見された
(ヘテロ接合)
- ・ **NEA(Negative Electron Affinity)** : 電子親和力 (真空準位と伝導帯の底の差) がマイナス

→光を入射すると、真空準位より高いエネルギー状態になるため容易に電子を外部に引き出せる。

- ・ **NEA状態を作る条件** : GaAsのバンドギャップ E_g より小さい仕事関数 ϕ となる薄膜を蒸着→NEA状態が実現



2. 序論

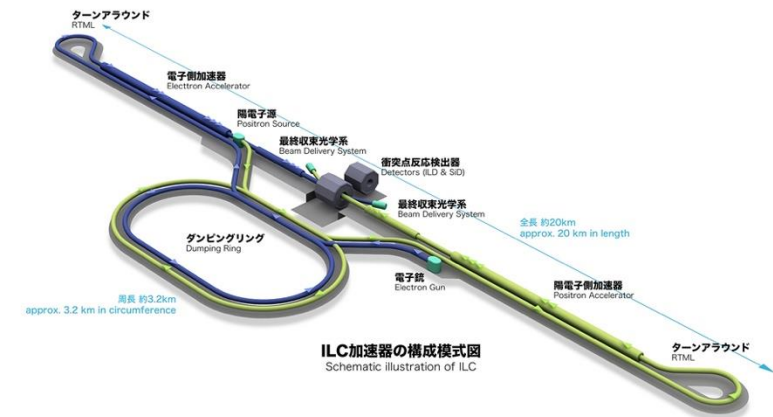
- ・ リニアコライダーはルミノシティ(衝突確率)が低い
- ・ 詳細な観測のためにスピン偏極電子が求められている

→ より高性能な電子源が必要

NEA-GaAs フォトカソード

高い量子効率

90%を超えるスピン偏極度



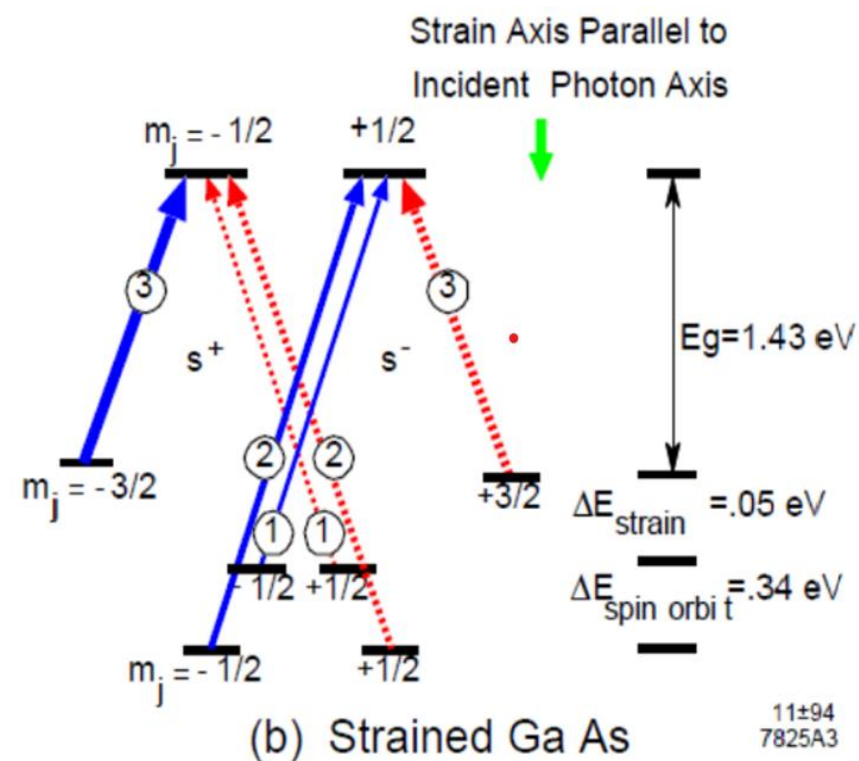
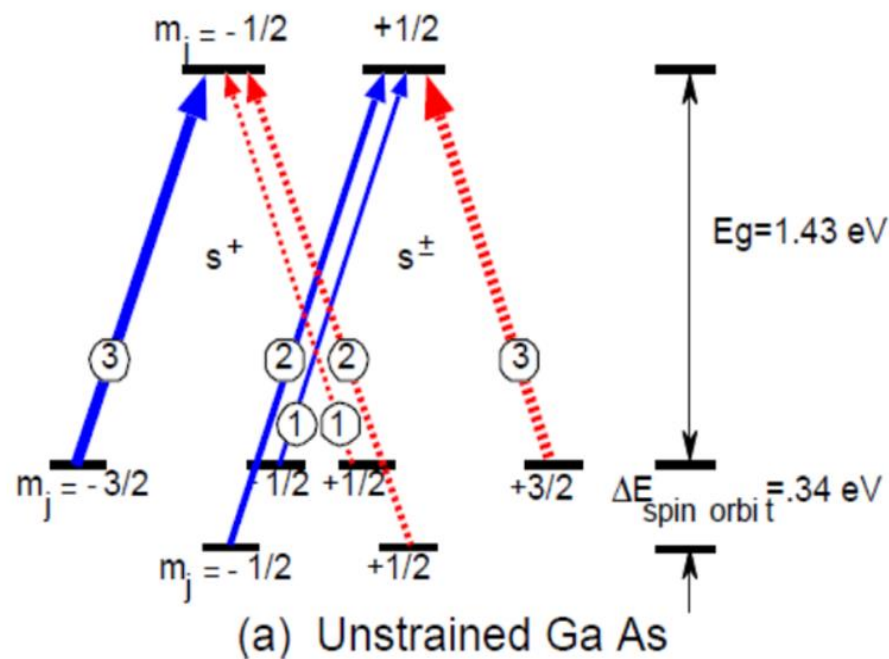
3. スピン偏極電子

- 円偏光した光レーザー(波長700~800nm)を照射するとエネルギー選択則によりスピン偏極電子が発生する

右巻き光子による励起を考えると・・・

伝導帯の角運動量 $J=1/2$

価電子帯： $J=3/2$



スピン偏極電子

- ビーム偏極度は

$$P = \frac{N_+ - N_-}{N_+ + N_-} \quad (N_{\pm} \text{は電子のヘリシティ状態の密度})$$

- GaAs 結晶→電子偏極度： 50%
- 歪み GaAsや超格子 GaAs→90%程度
- 偏極電子は光子のエネルギーをバンドギャップに限りなく近づけることで得られるがそれでは電子は飛び出ない
→NEA状態が必要

3. 実験方法

- 蒸着 1×10^{-9} Pa 程度の極高真空状態
- 蒸着源 粒状の Sb、線状ディスペンサーの Cs、K
- 水晶膜厚計(INFICON : Q-pod)にて膜厚を測定しながら蒸着
- 蒸着中、532nmのレーザーを照射
- 蒸着後には、300~900nmの波長を入射し量子効率の変化をみた