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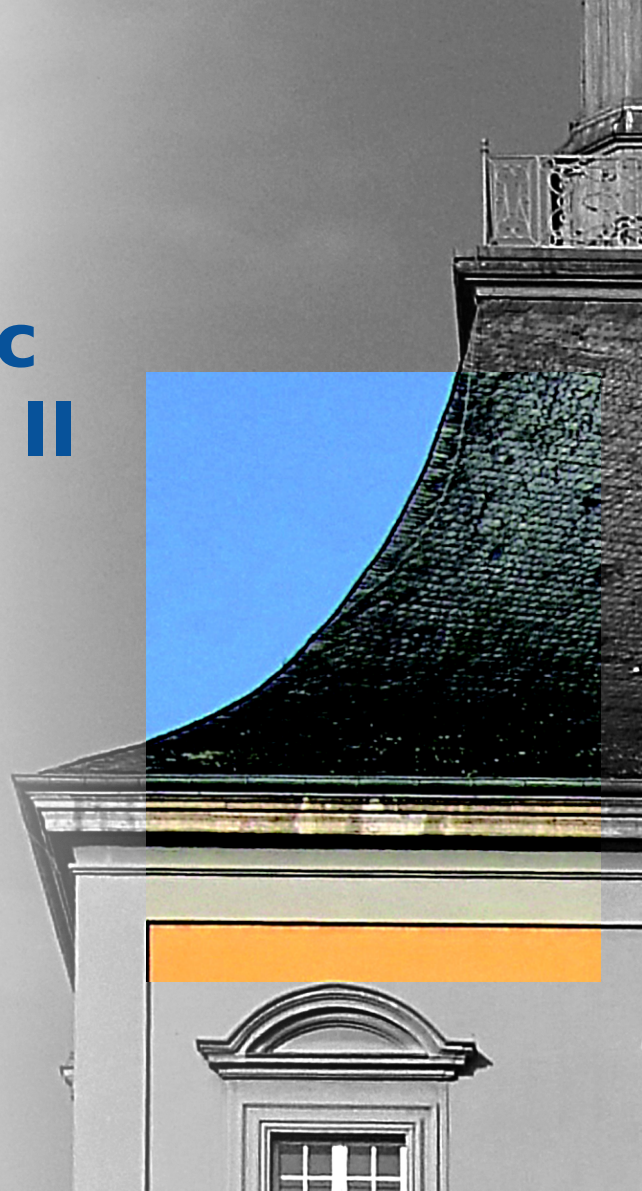
Design of the OBELIX Monolithic Active Pixel Sensor for the Belle II VTX Upgrade



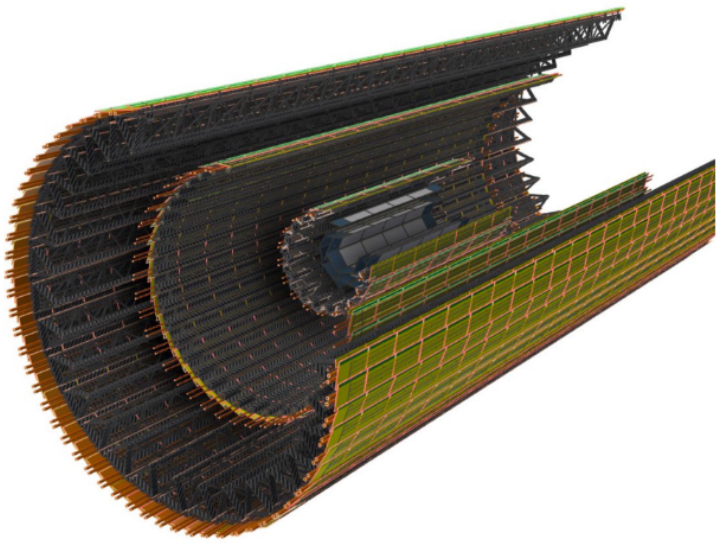
Belle II Germany Meeting 2025

Alexander Walsemann

Physikalisches Institut der Universität Bonn

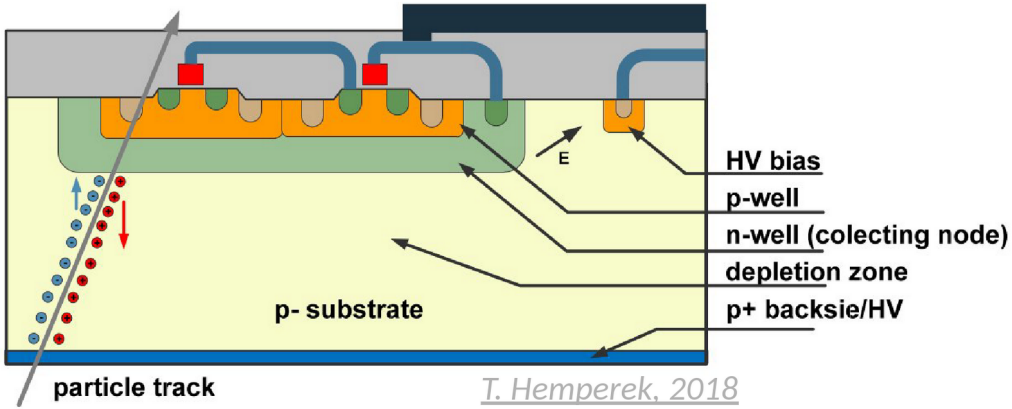
VTX Detector Design

- VTX Upgrade planned for LS2
- 6 Layers with Depleted Monolithic Active Pixel Sensors
  - **O**ptimized **BEL**le II p**IX**el sensor
- Identical pixel chips used for all layers
  - No separation into pixel and strip sensor
  - Different expected hit rates and power budget for L1-2 and L3-6
  - Different feature sets and cooling used for L1-2 and L3-6
- L1-2: Self supported all-silicon ladders with 4 chips each



Depleted Monolithic Active Pixel Sensor

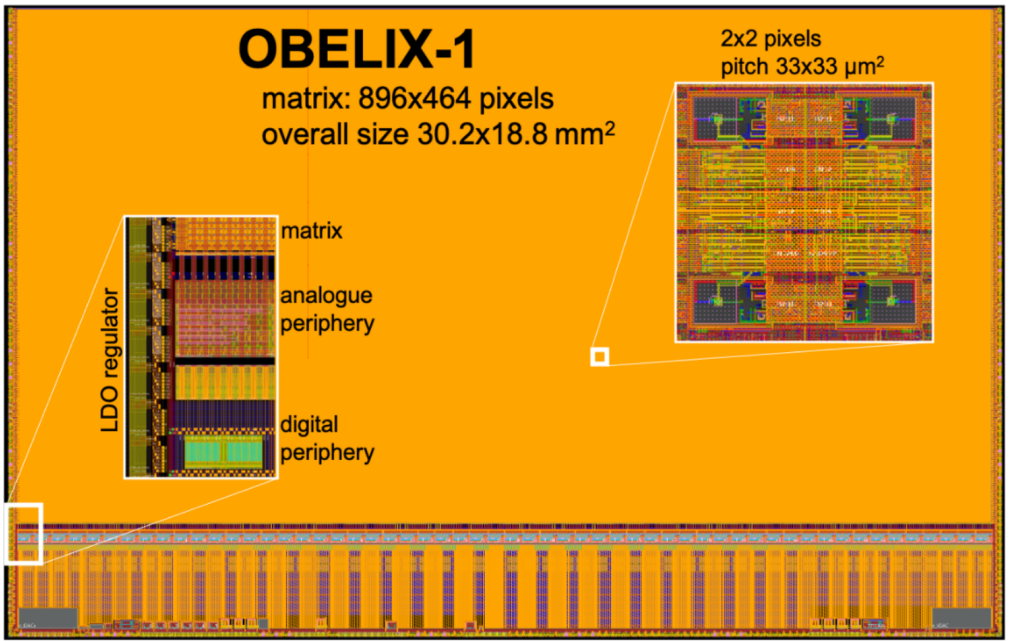
- Avoid error-prone bump or wire bonding in hybrid sensors
  - Fast module production and lower cost
- Lower material budget: Thinner sensor
  - Sensor thickness < 50 µm
- Processes offers high-resistivity substrate
  - Bias voltage capabilities (HV)
- Compared to MAPS:
  - Enhanced charge collection
  - Increased radiation tolerance



T. Hemperek, 2018

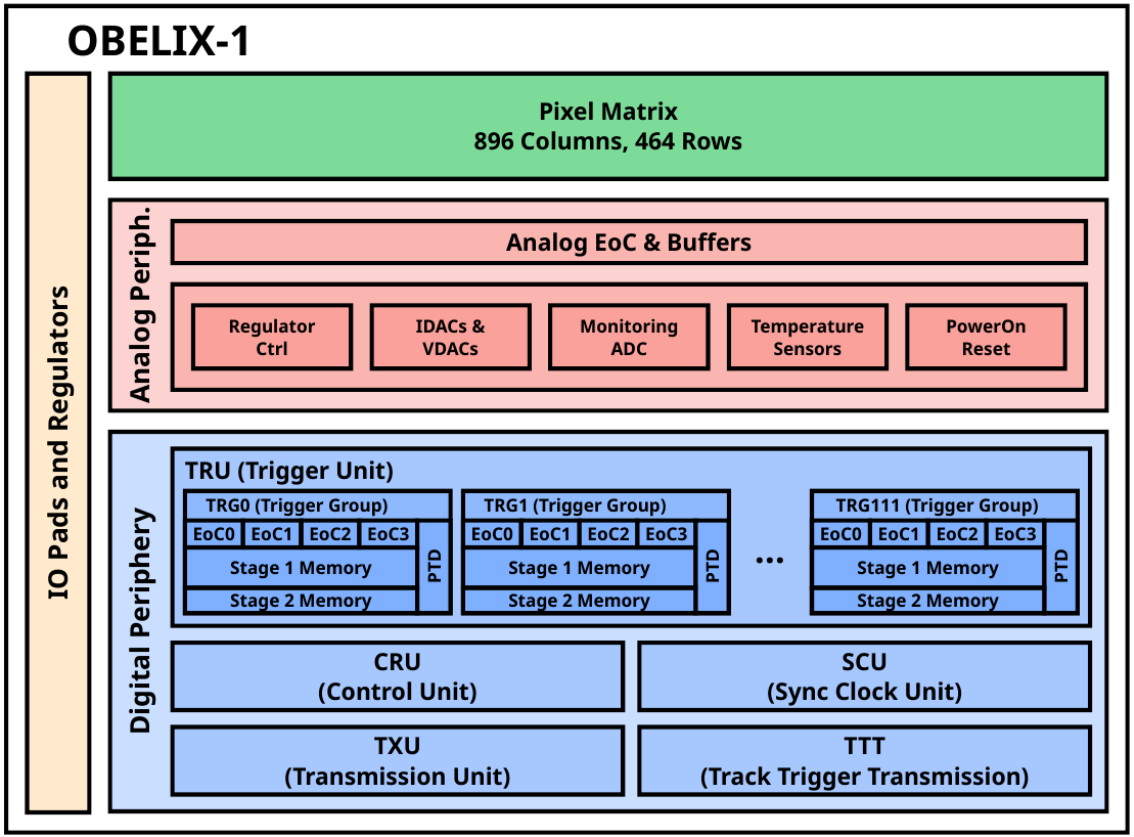
The OBELIX Chip

- **O**ptimized **BEL**le II p**IX**el sensor
  - 180 nm TowerSemi CMOS process
- The OBELIX chip is based on TJ-Monopix2
  - Matrix inherited, size adjusted
  - 464 rows and 896 columns
- Chip size: 30 x 19 mm²
- Power: < 300 mW/cm²
- Hitrates up to 120 MHz/cm²



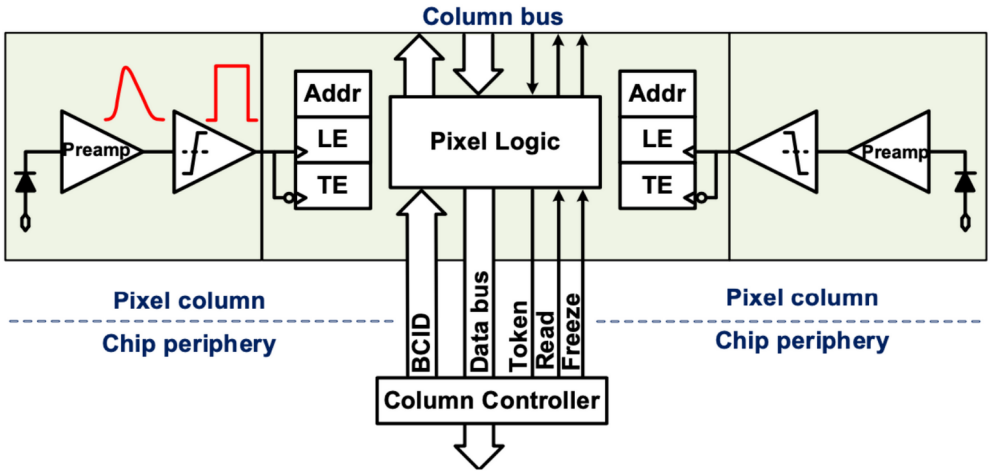
OBELIX Block Diagram

- Analog:
  - Column drain architecture from TJ-Monopix2
  - Monitoring ADC
  - Temperature sensors
- Supply via on-chip LDOs
- Digital periphery:
  - TRU: Pixel readout, trigger processing
  - PTD: Precision timing



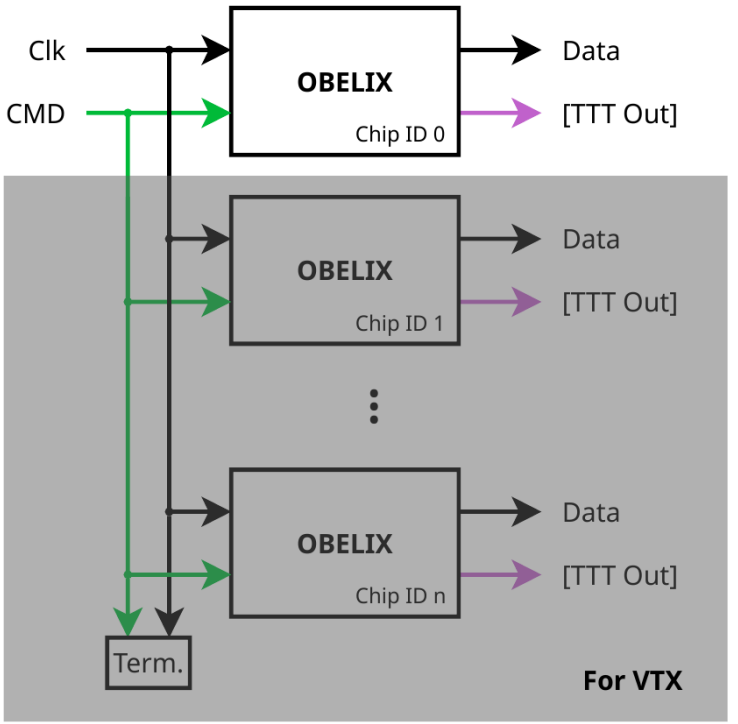
OBELIX Frontend & Readout

- Small collection electrode with electronics outside charge collection well
- 7 bit ToT information @ 50 ns
- In-pixel threshold tuning
- Readout organised in double columns
  - 448 Double columns
- Single flavor frontend
- Low voltage swing BCID driver
  - Reduce transient currents and BCID crosstalk



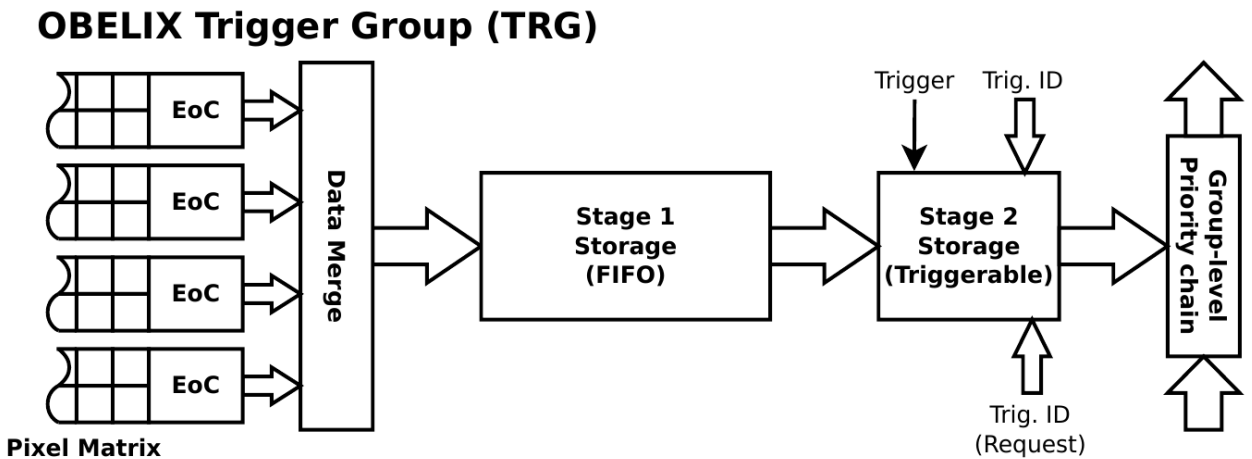
OBELIX Data and Command Connections

- Clock and CMD: Shared LVDS inputs
  - 5 bit ChipID: Up to 31 chips per bus
  - In VTX: Foreseen max. Chips 12 per module
- All slow and fast control runs over CMD line
  - 160 Mhz CLK / CMD data rate
  - 16 bit words, DC balanced
- Individual data outputs per chip
  - Double Data Rate (320 Mhz, 8b/10b encoded)

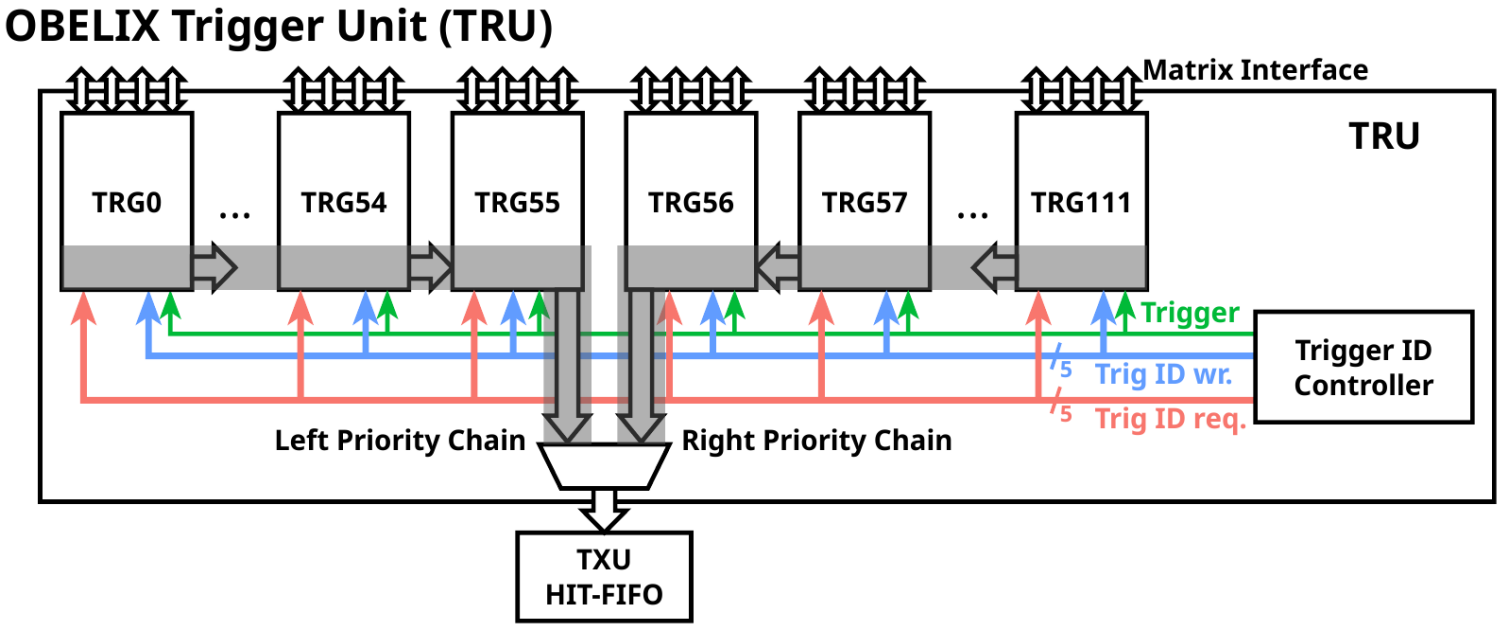


OBELIX Trigger System

- Trigger group connected to 8 columns (4 DC)
- Two stage memory for trigger association
  - Stage 1: Pre-trigger buffer (SRAM), 128 Hits
  - Stage 2: Associative memory to match trigger with ID, 32 Hits
- Trigger latency 10 µs
  - Trigger rate of > 30 kHz



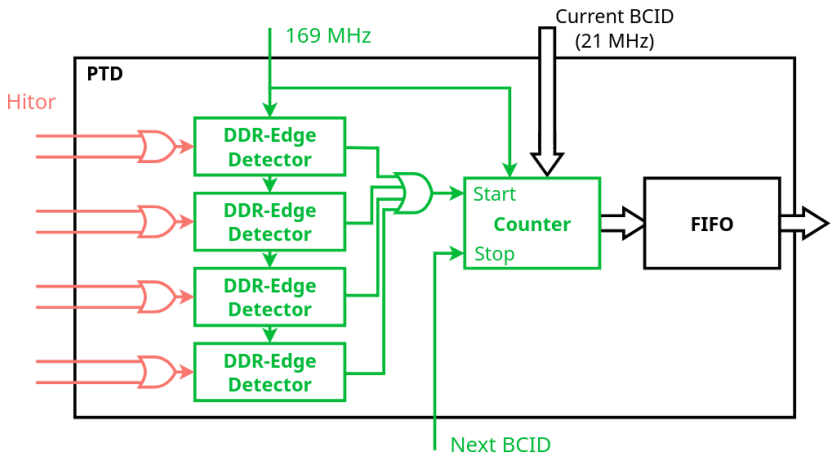
OBELIX Trigger System

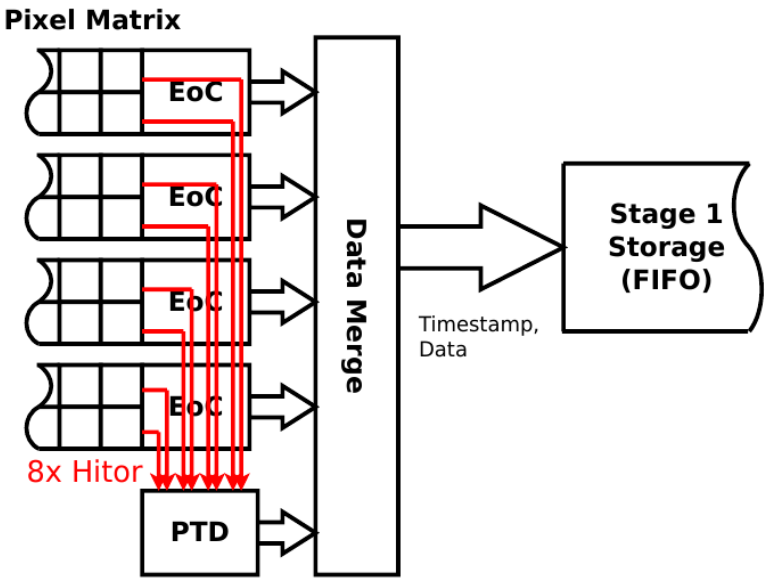


- Memory of triggered modules contains Trigger ID for readout
- Trigger memory organized in 112 trigger groups

Peripheral Time to Digital converter

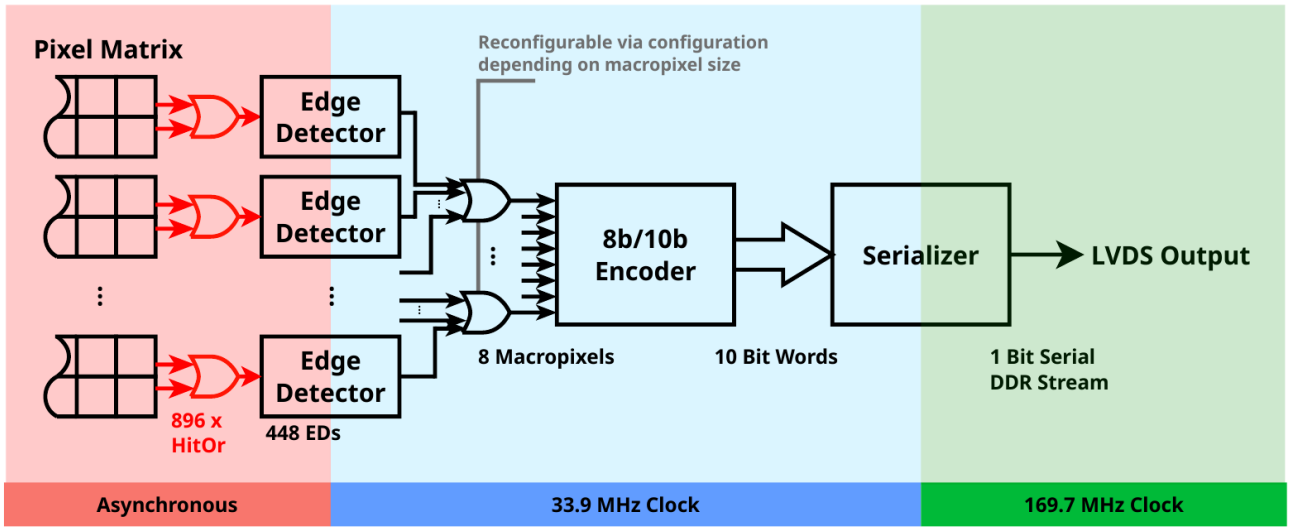
- PTD: Allow more precise timing than Timestamp (47 ns)
- Sampling: 2.95 ns period (169.7 MHz DDR)
- Calibration necessary
- High power consumption: disabled in iVTX





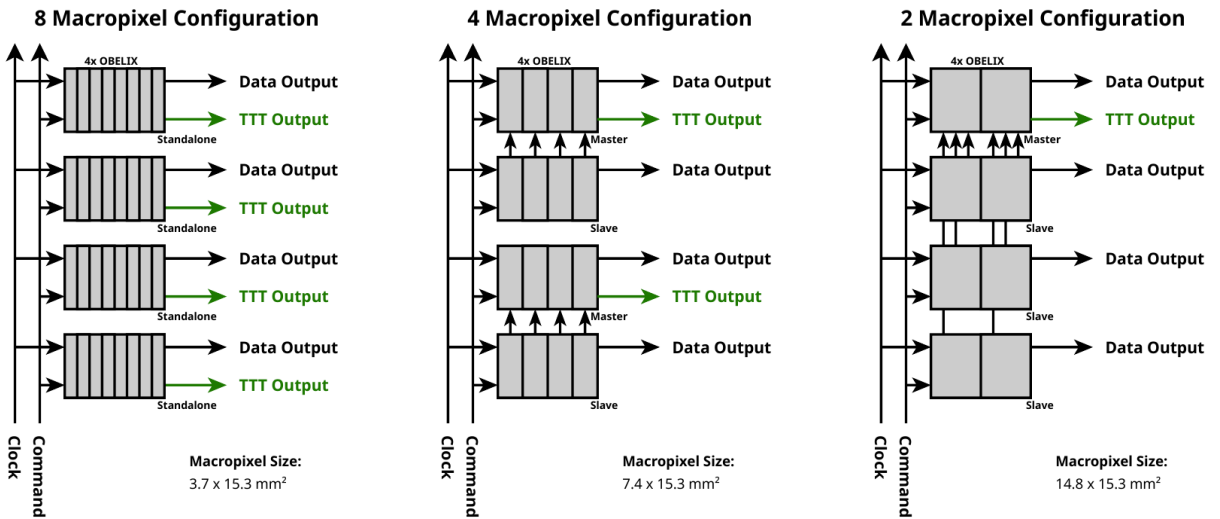
Track Trigger Transmission

- Trigger Output: VTX could contribute to L1 trigger system
- Completely independent from normal readout (parallel operation)
- No data frames, each byte sent one time bin (macropixel bit is set for hit)
- Time binning: 29.6 ns



TTT – System Configuration

- TTT allows for 8 macropixels
- Different Layers in VTX need different resolution
- 8 Macropixels can be shared between up to 4 chips
- Data format stays the same
- Reduced wire count



Summary and Current Status

- New on-chip features of OBELIX:
  - Larger matrix
  - Voltage regulators
  - Trigger logic
  - Precision timing module
  - Fast transmission for trigger contribution
  - Provisions for Monitoring via ADC and temperature sensors
- Implementation and verification is entering final stage
- Submission currently planned for the end of the year