Upgrade of the Belle II Vertex Detector with depleted monolithic CMOS active pixel sensors

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On behalf of the Belle II VTX collaboration

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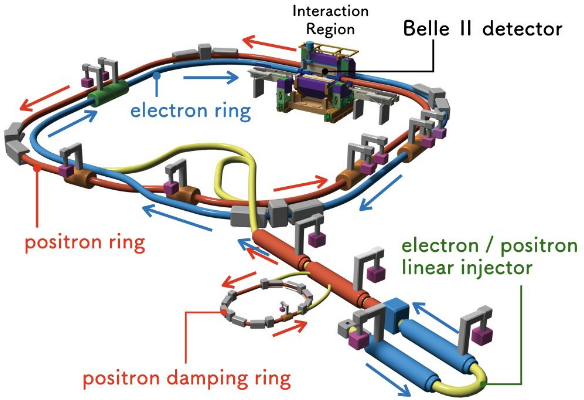
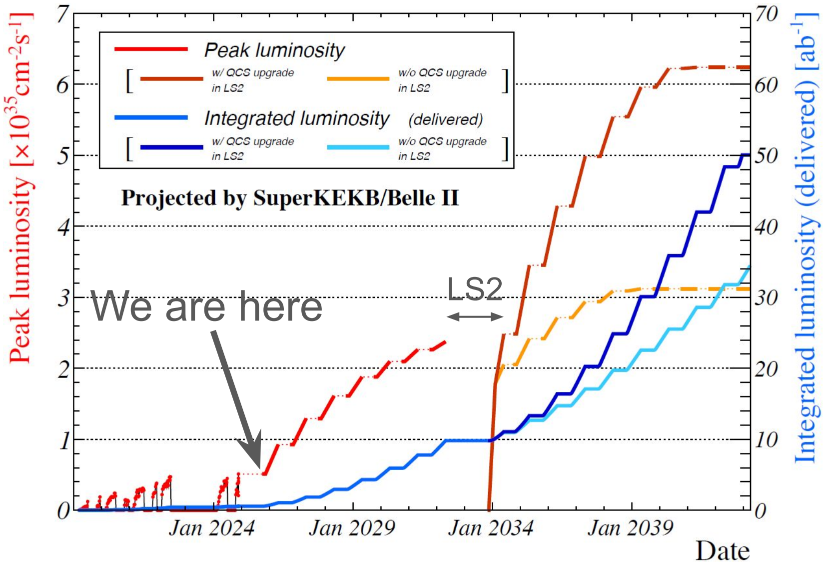
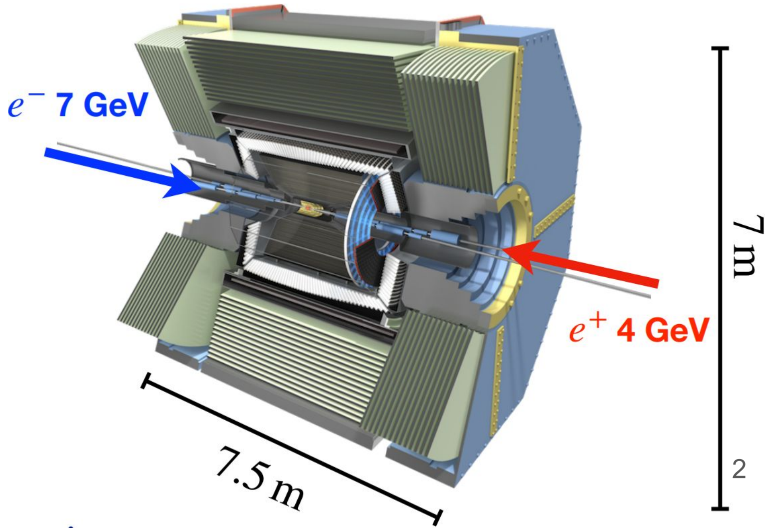
Belle II experiment at SuperKEKB

- B-Factory: e+e- collisions at Y(4S) resonance
- SuperKEKB at luminosity frontier aiming for 50 ab^{-1}
  - Luminosity Record: 5.1 x 10^{34} $cm^{-2}s^{-1}$
  - Target Luminosity: 6 x 10^{35} $cm^{-2}s^{-1}$
- Reaching the target luminosity will require IR redesign
- Long Shutdown 2 planned for 2032, TDR in 2027





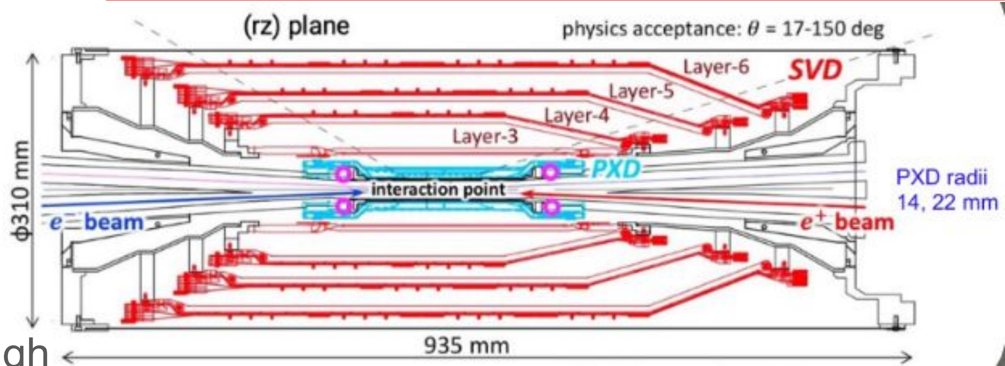


Current vertex detector (VXD)

- 2 layers Pixel Detector (PXD) using DEPFET pixels
- 4 layers Silicon Vertex Detector (SVD) using double-sided strip sensors
- Excellent performance at current occupancy <1%

- Sensor thickness 300μm, 0.75% X_0/layer
- 3ns time resolution
- strip length up to 12 cm
- CO_2 cooling
- Occupancy limit 6% (Layer 3)

SVD



- Background extrapolations at target luminosity have large uncertainties
- Expecting **performance degradation** in high background scenario at target luminosity
  - PXD layer 1: up to 2% occupancy and 32 MHz/cm^2
  - SVD layer 3: up to 9% occupancy and 9 MHz/cm^2

- Sensor thickness 75μm, 0.25% X_0/layer
- 20μs integration time
- Pixel pitch 50-70μm
- CO_2+N_2 cooling
- Occupancy limit 3%

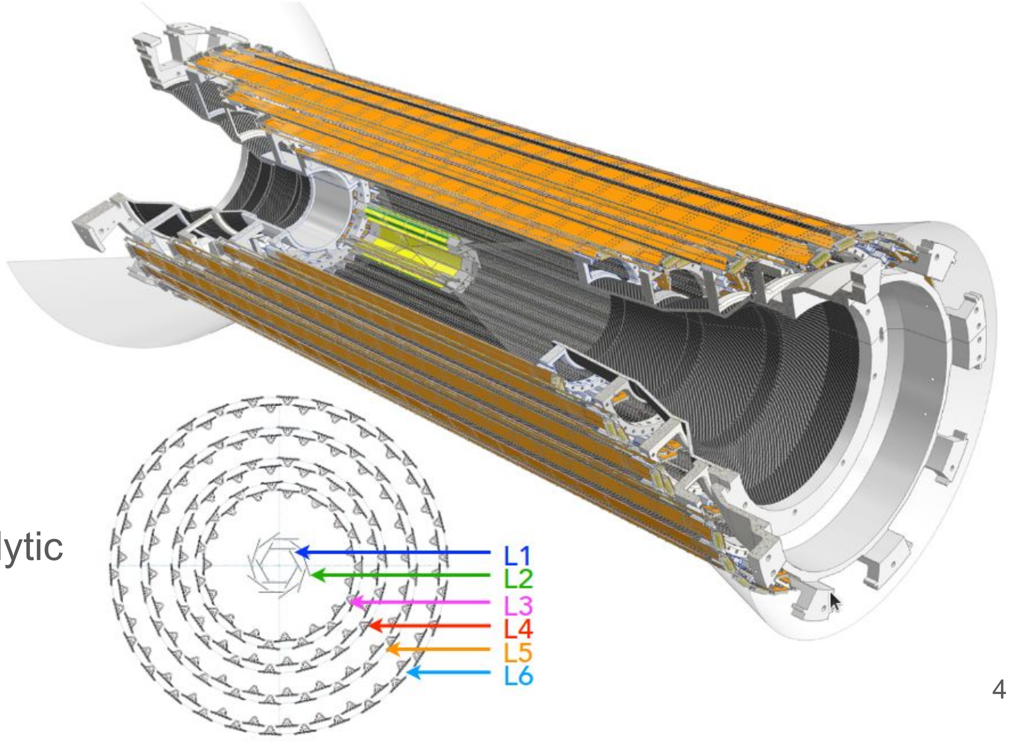
PXD

VTX proposal

Requirements:
- Radiation
  - TID: 100 Mrad
  - NIEL: $5x10^{14}$ neq/cm^2
- Hit rate up to 120 MHz/cm^2
- Resolution < 15 µm
- Integration time 50-100 ns
- Operation simplicity and reduced services
- Material budget <= 3.5% X_0

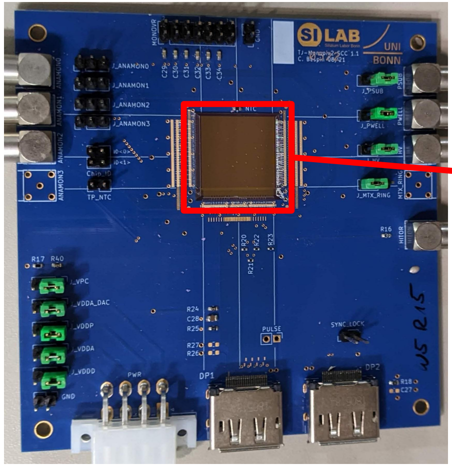
- Water cooling for **oVTX**
- **iVTX** cooling options under investigation
  - Initially prefered: air cooling
  - thermal conduction with thermal pyrolytic graphite
  - Liquid cooling using thin Al-pipes

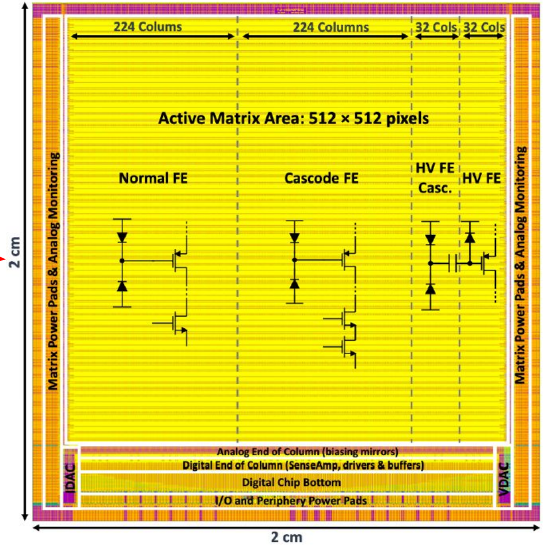
- 6 straight fully pixelated barrel layers
- **OBELIX** chip for all layers
- **Power dissipation:** 200-300 mW/cm^2 for hit rates from few to 120MHz/cm^2
- **iVTX**: L1+L2 self-supported, ~0.3% X_0/layer
- **oVTX**: L3-L6 with carbon fibre support structure, ~0.6% X_0/layer



TJ-Monopix2 as predecessor of OBELIX

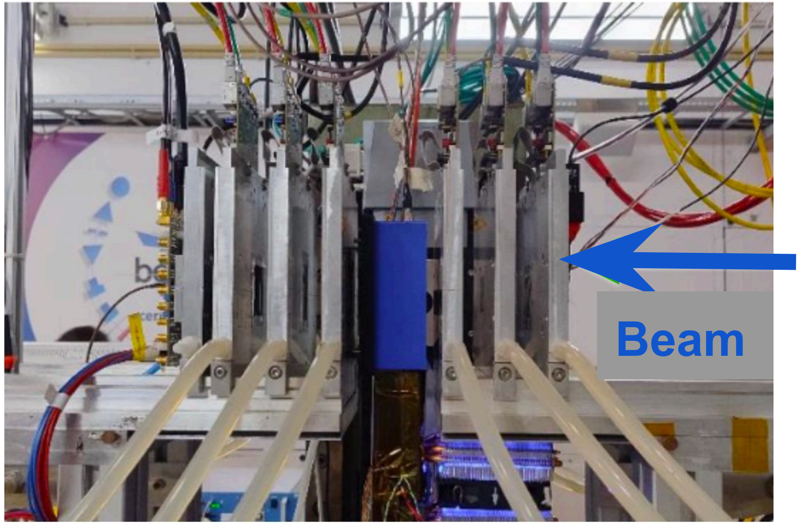
- Depleted Monolithic Active Pixel (DMAPS)
  - Modified 180 nm TowerSemi CMOS process
- Modified development for ATLAS ITK outer layers
- 512x512 pixels (2x2 cm^2) with 33x33 μm^2 pixel pitch, 25 ns integration
- 7 bit ToT, 3 bit in-pixel threshold tuning
- 4 front-end flavours: DC and AC input coupling, additional transistor in amplifier
- Carry over analog pixel design to OBELIX

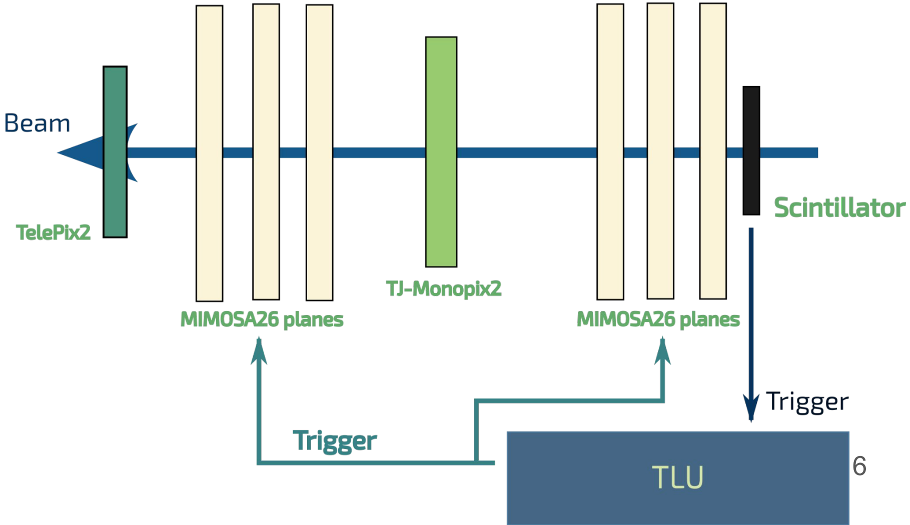




TJ-Monopix2 Test Beam 2025

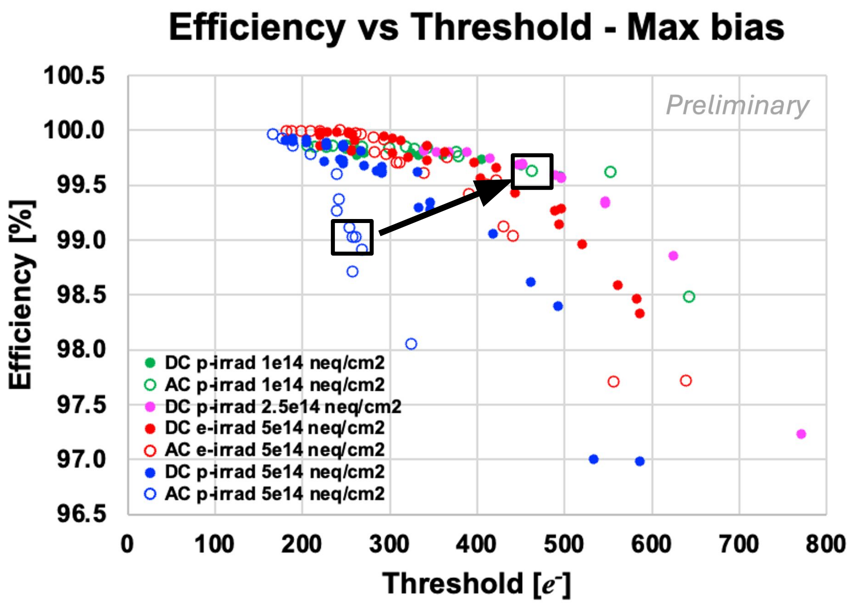
- At DESY II test beam facility: 3-5 GeV electrons
- Focus on performance degradation due to irradiation and temperature
  - Important for decision of cooling solution
- Using Peltier device for heating and cooling in 10°C - 50°C range
- 3 p-irradiated sensors 1-5 x 10^{14} neq/cm^2, 1 e-irradiated 5 x 10^{14} neq/cm^2





Test Beam 2025 - preliminary results

- Efficiency degrades with larger irradiation: Less irradiated chips show higher efficiency, even at higher thresholds
- p-irradiated exhibits smaller efficiency than e-irradiated at same fluence
  - Suggests larger bulk damage by p-irradiation
- AC-coupled frontends has smaller efficiency at same threshold and fluence



Temperature range 10°C-50°C and different FE settings

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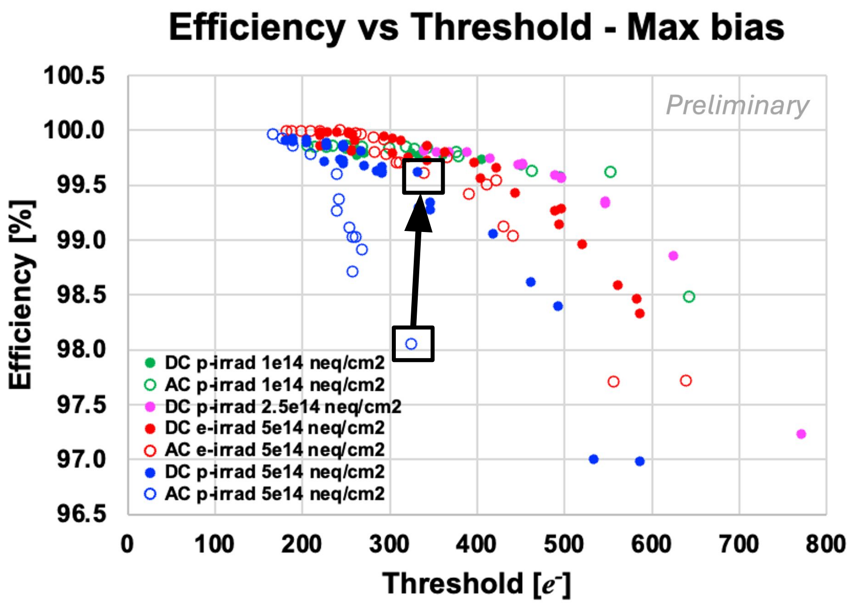

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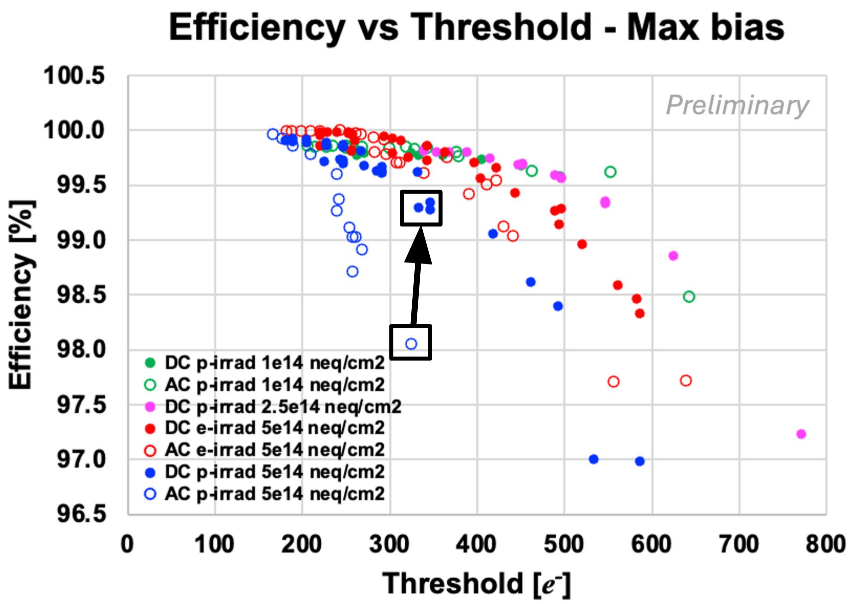
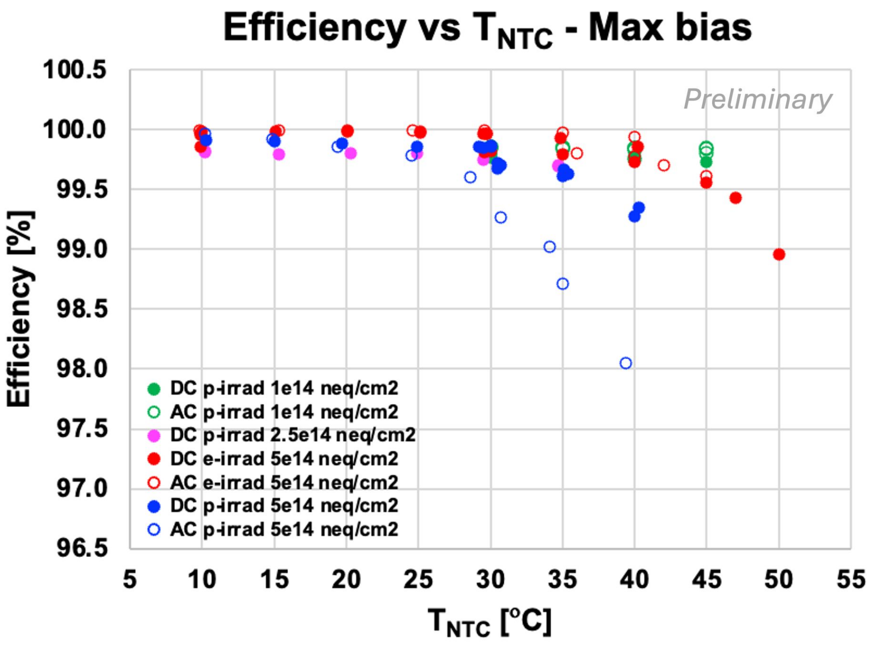


Temperature range 10°C-50°C and different FE settings

Test Beam 2025 - preliminary results

- Efficiency degrades at higher temperatures
- Effect largest for high fluences and AC-coupled FE
- Difficulties operating above 40°C due to noise and increased leakage current
- After irradiation also threshold increase with temperature → higher leakage current causing a faster discharge of the collecting electrode



Using consistent settings per chip and front-end

OBELIX sensor design

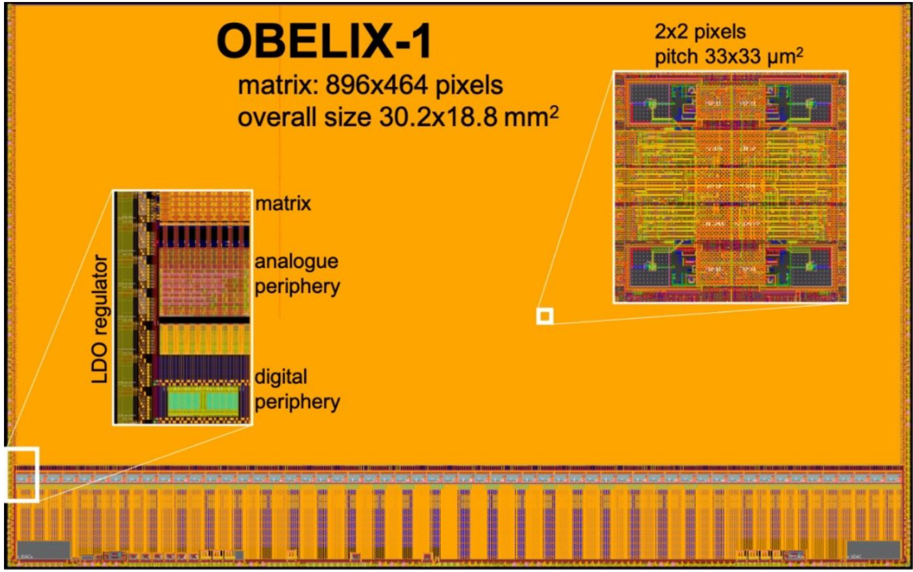
- Analog design inherited; OBELIX-1 with 2 frontends

Belle II application specific changes:

- Trigger logic and buffer memory
- On-chip LDO voltage regulators

Specifications:

- Chip size: 30 x 19 mm2
- Pixel size: 33 x 33 μm^2
  - 464 rows, 896 columns
- Time stamping: 50 to 100 ns
  - PTD: Fine time stamping ~5ns
- Allows ~10 μs trigger latency at 30kHz
- Hit rates up to 120 MHz/cm^2



Summary

- SuperKEKB pushing for 6 x 10^{35} $cm^{-2}s^{-1}$ likely requires IR redesign
- Proposing upgrade for current VXD using OBELIX DMAPS 180nm CMOS chips
- Lab tests and test beam campaigns on TJ-Monopix2 to validate performance
- Test beam in March 2025 with irradiated DUTs up to maximum fluence and improved temperature control
  - Efficiency after irradiation shows temperature-dependent degradation, especially for AC-coupled frontend
  - DC-coupled frontend after irradiation maintains >99% efficiency up to ~40 °C with threshold ~350e-
  - Stable operation with threshold ~200e- at lower temperature
- Aiming for submission in winter 2025 → preparing TDR in 2027 → commission upgraded detector for high luminosity operation after LS2 in ~2032

The measurements leading to these results have been performed at the Test Beam Facility at DESY Hamburg (Germany), a member of the Helmholtz Association (HGF)

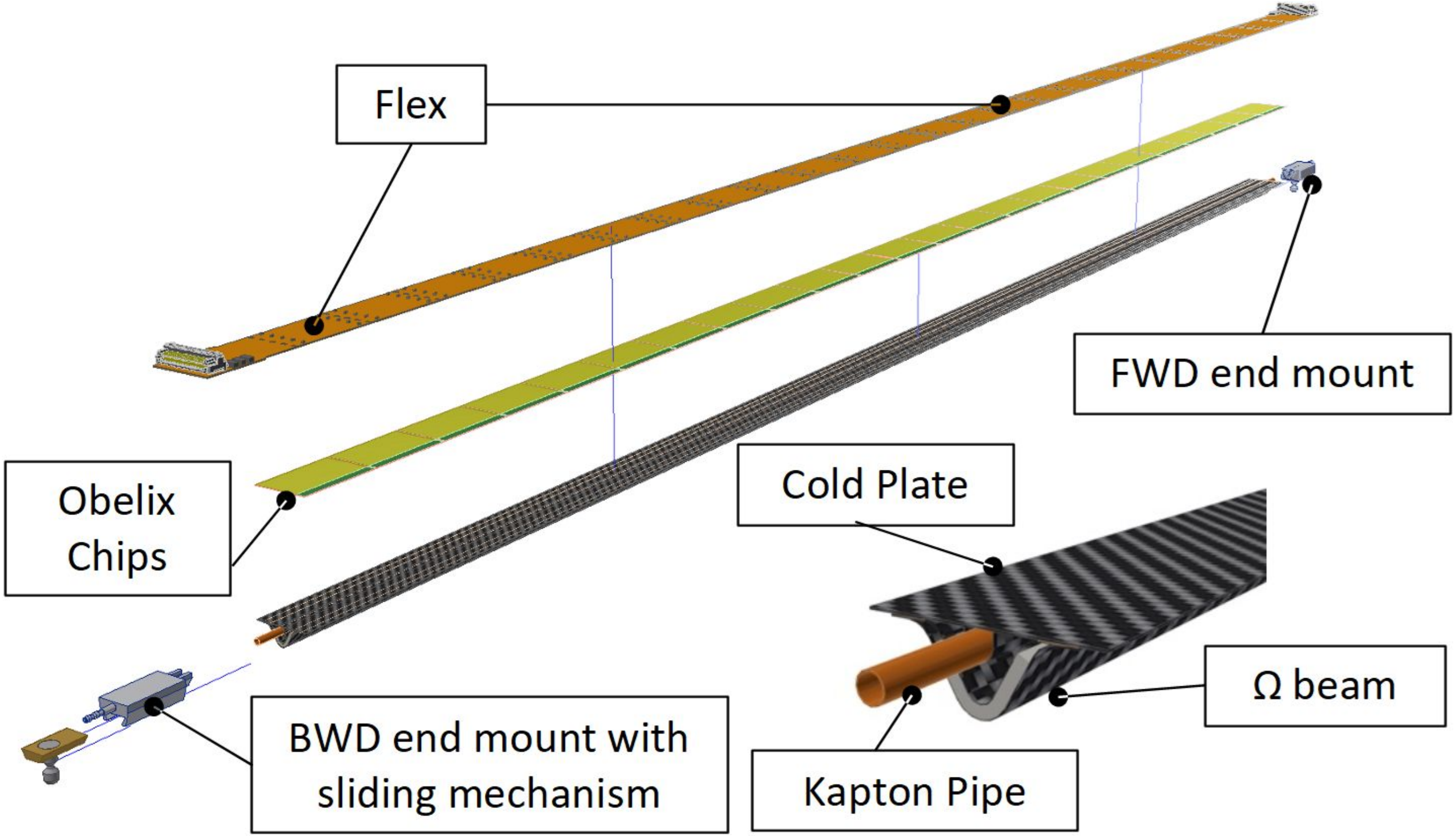
BACKUP

VTX Collaboration

VTX collaboration

IGFAE, Santiago	Jilin University	IJCLab, Orsay	IPHC, Strasbourg
University of Bergamo	KIT, Karlsruhe	RAL, Oxford	University of Tokyo
University of Bonn	IPMU, Kashiwa	INFN & University of Pavia	KEK, Tsukuba
University of Dortmund	Queen Mary University of London	INFN & University of Pisa	IFIC (CSIC-UV), Valencia
University of Göttingen	CPPM, Marseille	IFCA (CSIC-UC), Santander	HEPHY, Vienna

o-VTX Ladder mechanics



TTT module - Track trigger

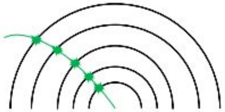
Is triggering with pixel sensor information feasible ?

Fast Track Reconstruction Algorithm

Look-Up Table

- Logic based on a **reference table** :
  1. **Pattern Table** :
     - Stored physical track patterns from simulation with their characteristics
  2. **Detector/Table pattern comparison** :
     - Triggered track if its pattern is recognized in the table

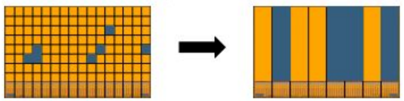
Example Pattern
$\theta = 37.2\,°, \varphi = 256{,}3\,°, p_T = 1{,}13$ Gev/c



Macropixels

Pixel :
- Design granularity
  - **896** x **464** per sensor
  - ~ 10^9 in the detector

Macropixel :
- Reduced spatial granularity
  - **8** x **1** per sensor
  - **~20k** in the detector



- **Reduction** in the number of combinations
- **Smaller** Pattern Table
- **Faster** to search through
- **Manageable** bandwidth for transmission

Patterns

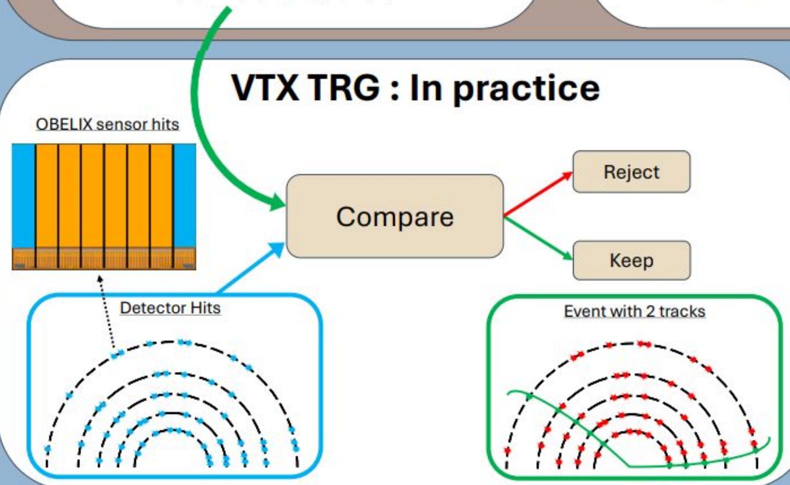
- **Pattern** : Bitword merging TTT information from all sensors
  - Current Geometry : 2552 Sensors ➡ **20416 bits**
- **LUT comparison** :

Online Hits 0011…100…110..01…1010
A pattern 0010…100…010..01…0010

- **Pattern Table :**

Index	Pattern	Θ (°)	Φ (°)	p_T (GeV/c)
1	001…010….0001	67	259	1.56
2	010…010….0001	125	23	0.89
…	……..	…	…	…
126304	100…010….0100	43	344	2.34
126305	100…010…0010	175	88	1.71

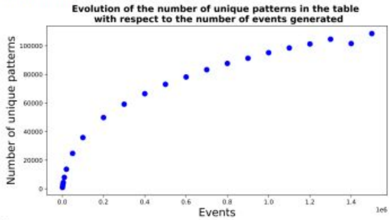
VTX TRG : In practice



Study case

1. Table generation
   - $10^6\ \mu^{\pm}$ => With 5 Layers, ~100k unique patterns

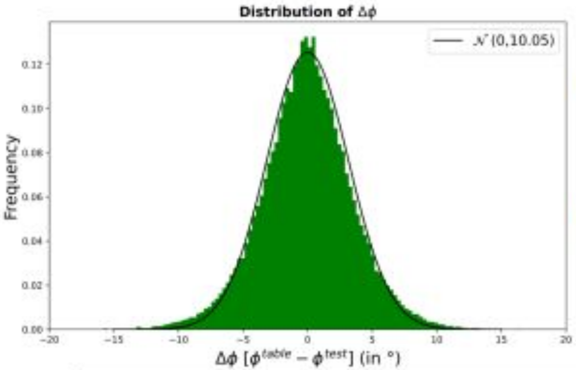
Table event characteristics	
Production point	$(x = 0, y = 0, z = 0)$
Range of momentum	0.2 GeV/c $\leq p \leq$ 3.0 GeV/c
Range of θ angle	$17° \leq \theta \leq 150°$
Range of φ angle	$0° \leq \varphi \leq 360°$



2. Test samples :
   1. Efficiency/Z-vertex acceptance : $10^5\ \mu^{\pm}$ with table characteristics / with z ∈ $[-10,10]$ cm
   2. Angle Accuracy : $10^5\ \mu^{\pm}$ with table characteristics
   3. Fake Trigger Rate : 10^6 background events, 3 BG Scenarios

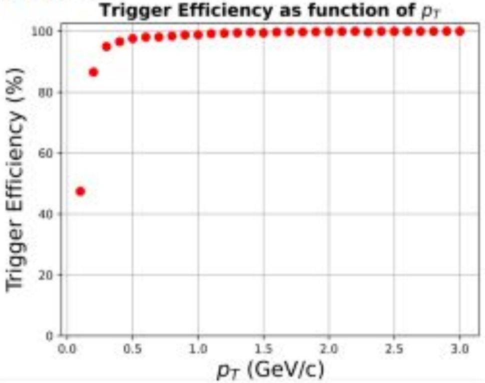
TTT module - Track trigger

Results

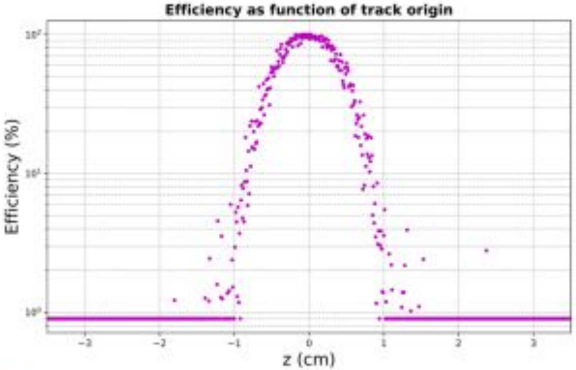


Φ Accuracy :
$\pm 3,18$ °

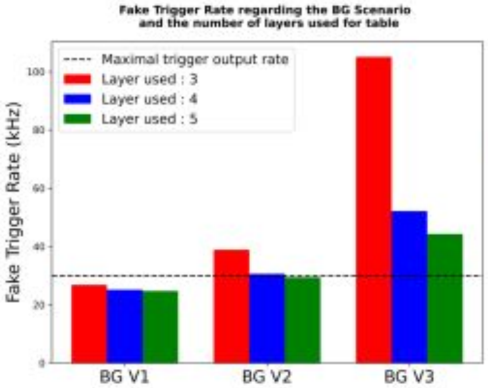
θ Accuracy :
$\pm 0,34$ °



Average Efficiency :
$98,14 \pm 0,03$ %



Z-vertex
Acceptance :
$|z| < 2,5$ cm



Cut :
“Number of track > 2 & p_T > 1 Ge

Best Case Fake Rate :
23 kHz

- ➢ Investigate better cuts