

BELLE II GERMANY MEETING - AUGUST 2025

# PXD EMERGENCY SHUTDOWN INVESTIGATION

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1

Motivation

2

Simulation of PXD signal path

3

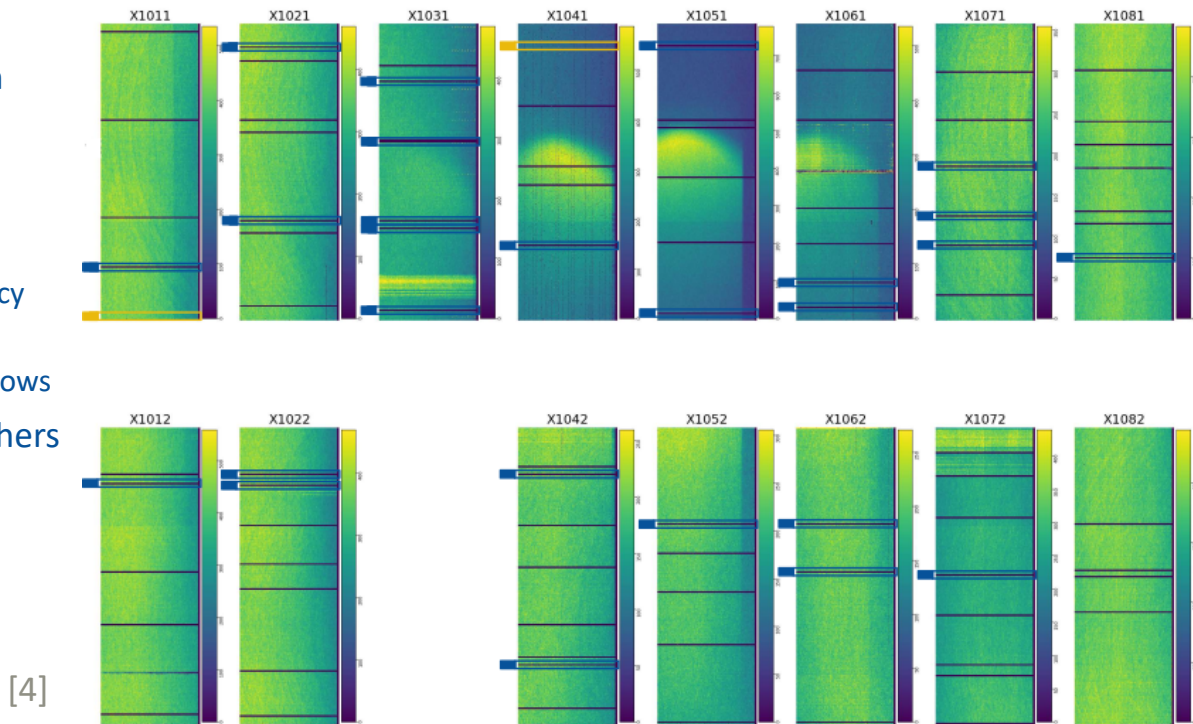
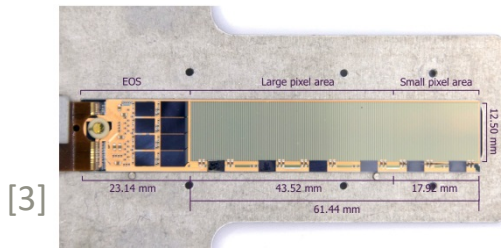
Lab-test: Fast-Shutdown signal transm.

4

Lab-test: Fast-Shutdown board modification

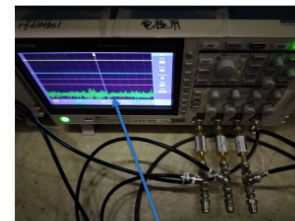
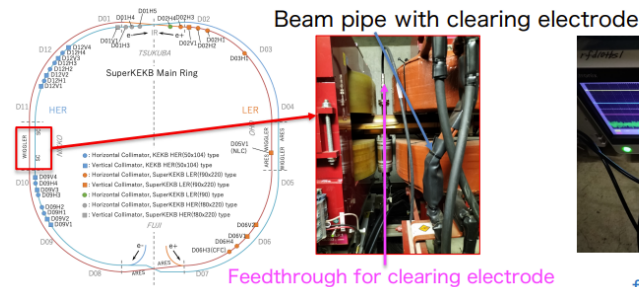
# MOTIVATION

- Switchers **vulnerable** to large radiation
- Example: Beam loss event in 2020
  - Estimated dose: 500 rad for PXD1 in 40  $\mu$ s
  - Increased number of **inefficient rows**
    - In total 89 inefficient rows  $\rightarrow$  efficiency drop of 3%
    - blue flags: freshly emerged inefficient rows
- Damage can be prevented when Switchers are turned off
- $\rightarrow$  Shutdown as fast and safe as possible

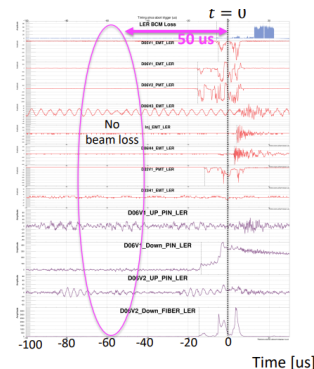
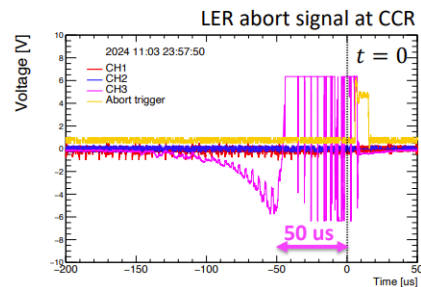


# BEAM LOSS DETECTION

- New sensors, improved signal transmission
  - Faster and earlier detection of SBLs
- Plan : Include signals into PXD interlock
  - Lower threshold to put PXD into safe OFF state
- Candidate : Signal in clearing electrode
- Signal detected close to area where pressure burst occurred
- Strong correlation with SBLs
- Cable routing started (amplification and integration still TBD)
- To benefit from faster detection, we must minimise PXD shutdown delay

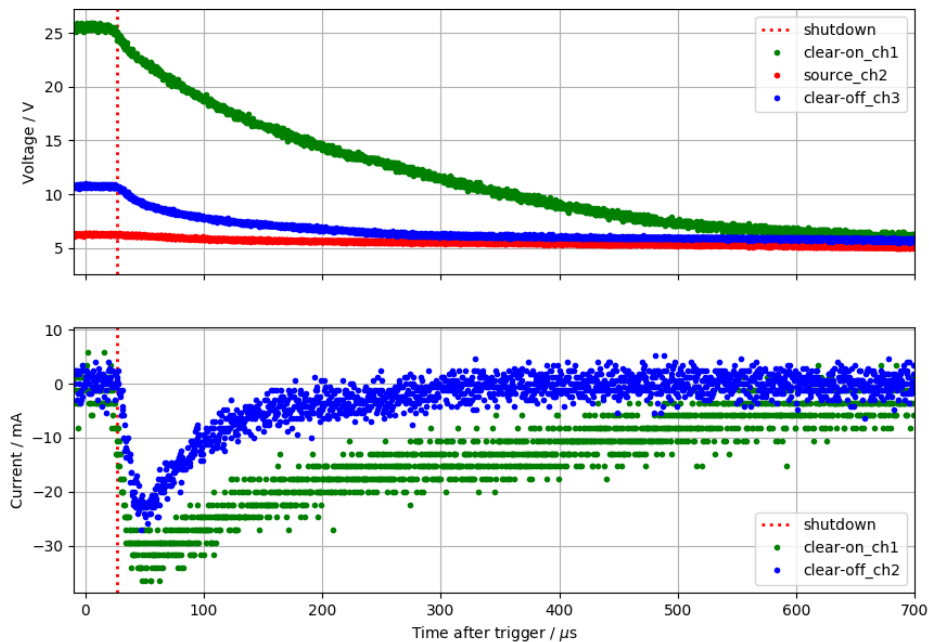


Monitor the signal from the feedthrough



# REGULAR SHUTDOWN

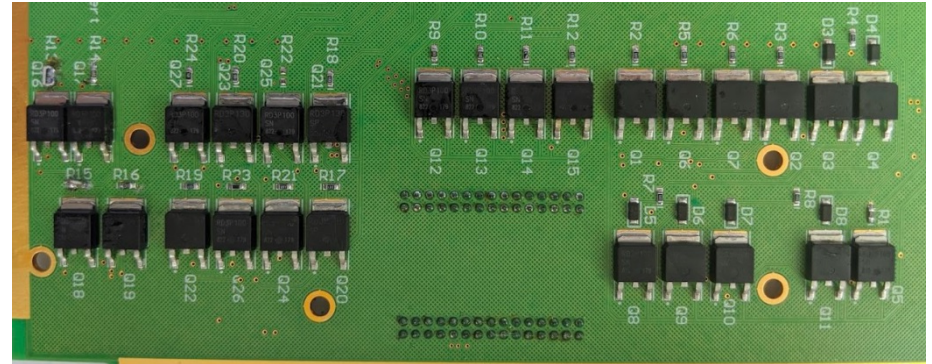
- Regular shutdown applied at PXD1:
  - Switch off power
- Example: Shutdown of Switcher voltages
- **Long discharge time** due to capacitors
  - Shutdown time in ms-range



[4]

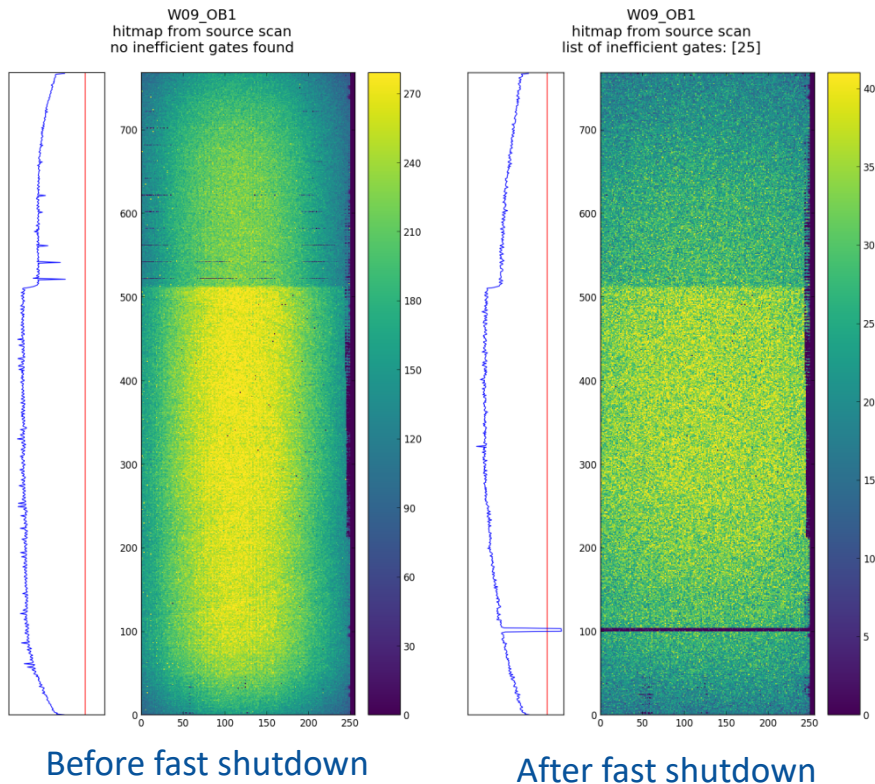
# FAST SHUTDOWN BOARD

- Idea:
  - Short all channels with FET (Field Effect Transistor) to respective ground
  - **Active pull-down**
  - Add resistor to influence pull-down time
- Problem:
  - Required resistor values unclear yet



# RESULTS FROM FAST SHUTDOWN

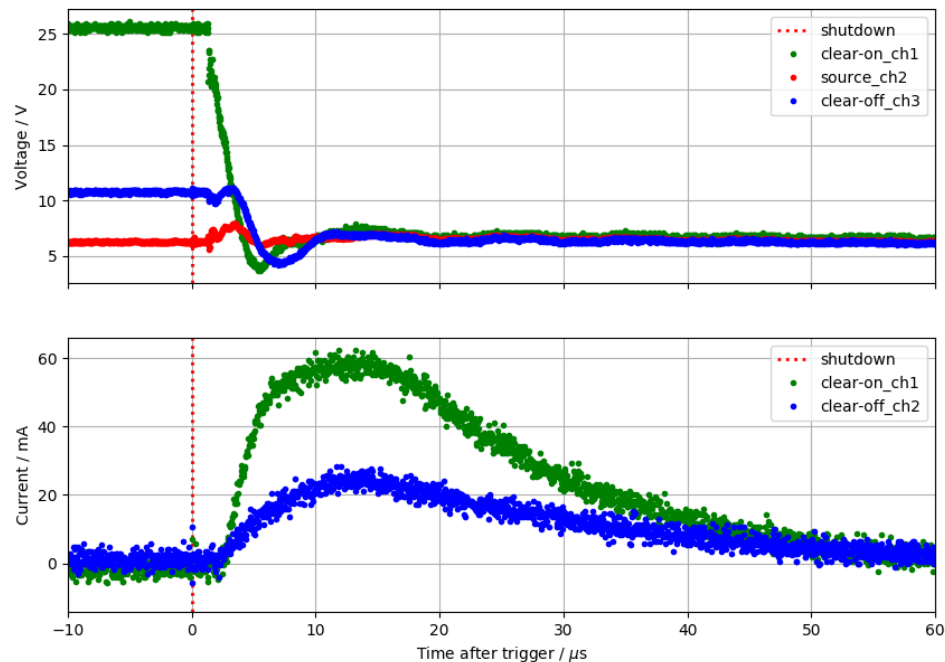
- Testing of **fast shutdown** board resulted in high Switcher currents
- Example:
  - Compare hitmaps before and after using fast shutdown board
  - Detected **inefficient rows**
- If done wrongly:
  - Fast shutdown has **same effects** as a beam loss event

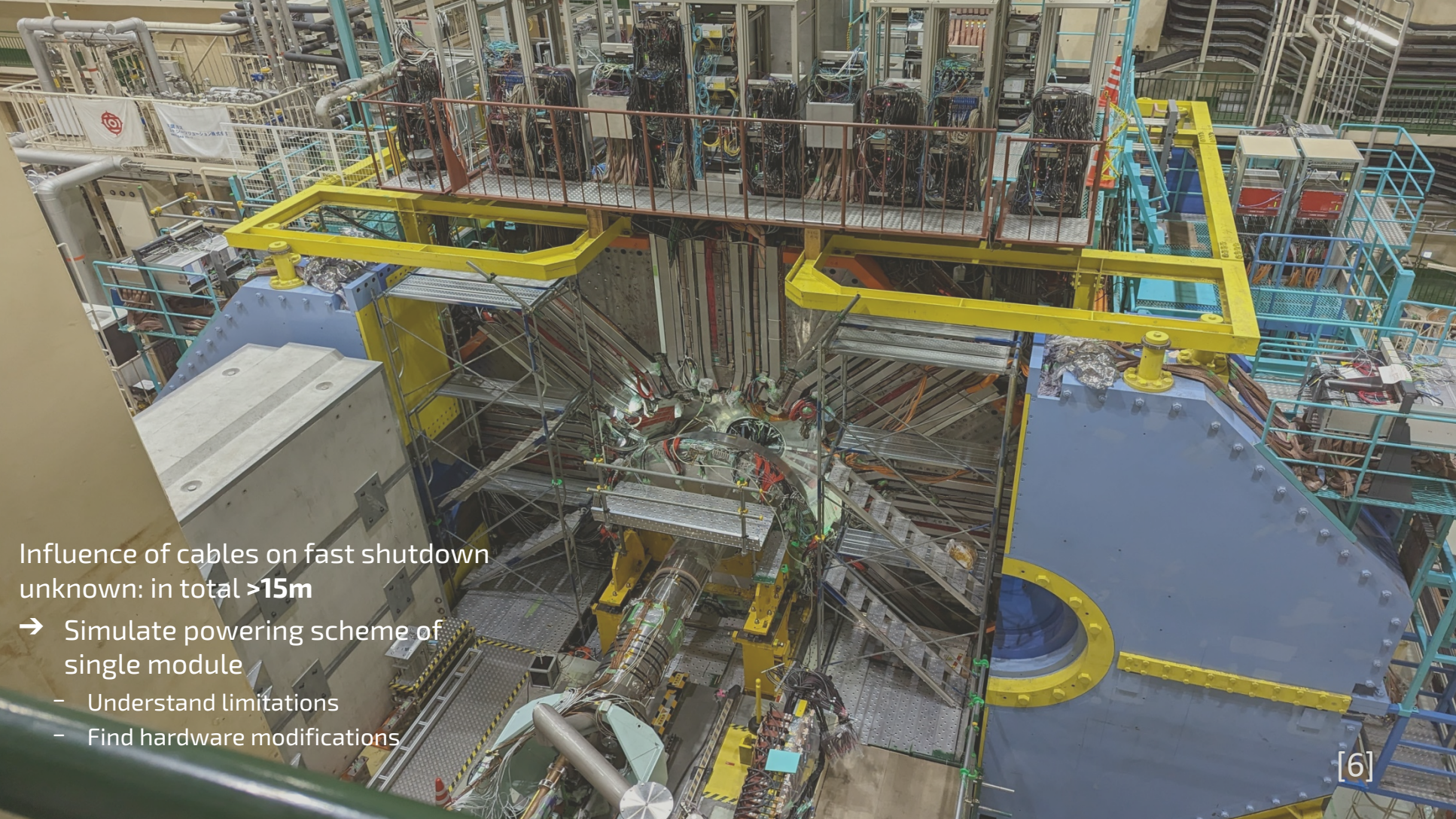


[5]

# FAST SHUTDOWN MEASUREMENT

- Example: Shutdown of Switcher voltages (Clear On/ Clear Off), **measured at Power Supply level**
- $R_{ClearOn} = 0\Omega$ ,  $R_{ClearOff} = 0\Omega$
- $V_{ClearOn}$  drops below  $V_{ClearOff} \rightarrow$  violation of shutdown sequence
- Testing on module is harmful

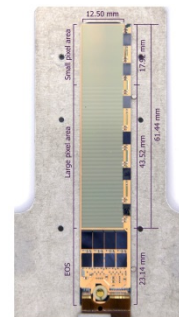
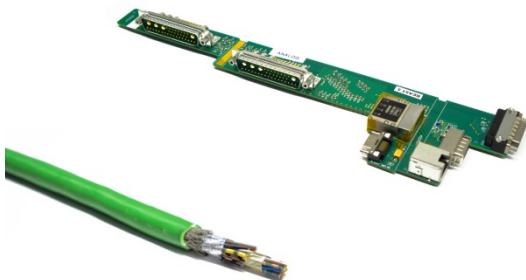
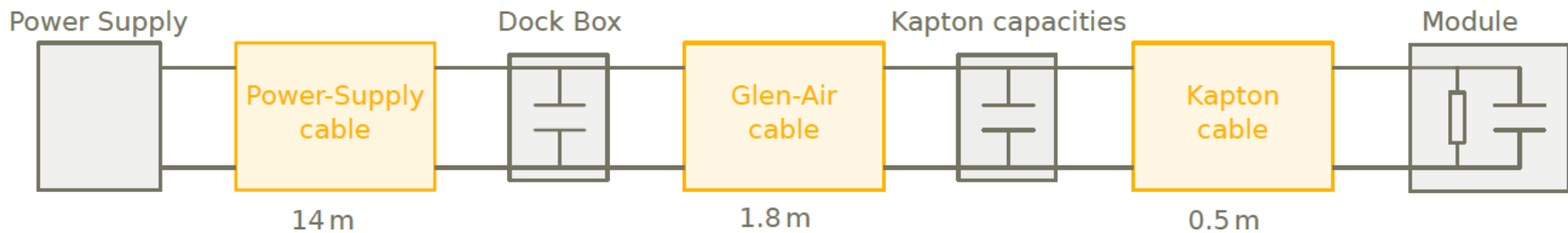




Influence of cables on fast shutdown  
unknown: in total **>15m**

- Simulate powering scheme of  
single module
- Understand limitations
  - Find hardware modifications

# SIGNAL PATH



[1]

1

Motivation

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Simulation of PXD signal path

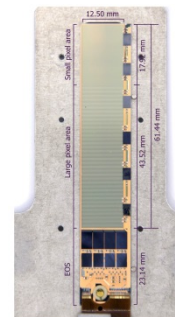
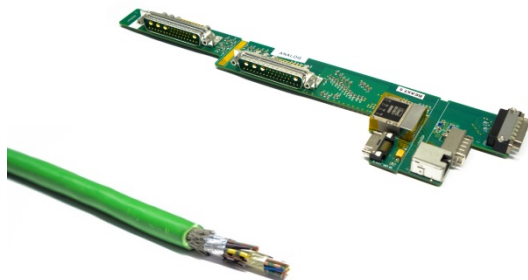
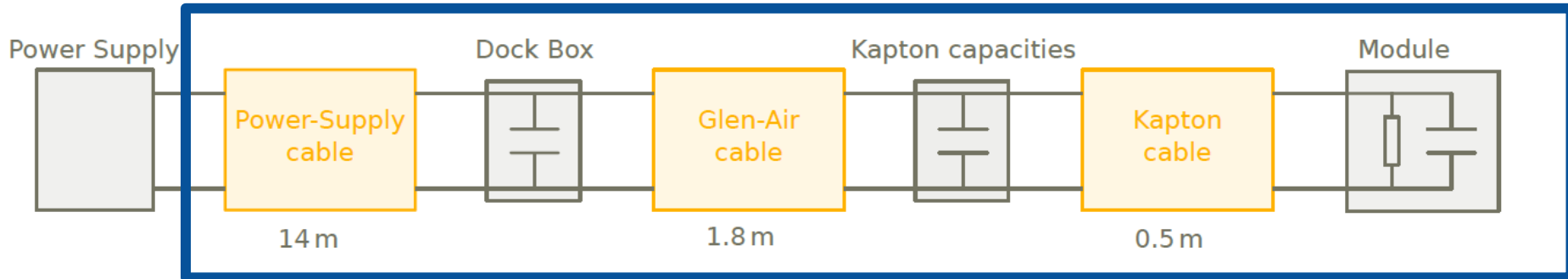
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Lab-test: Fast-Shutdown signal transm.

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Lab-test: Fast-Shutdown board modification

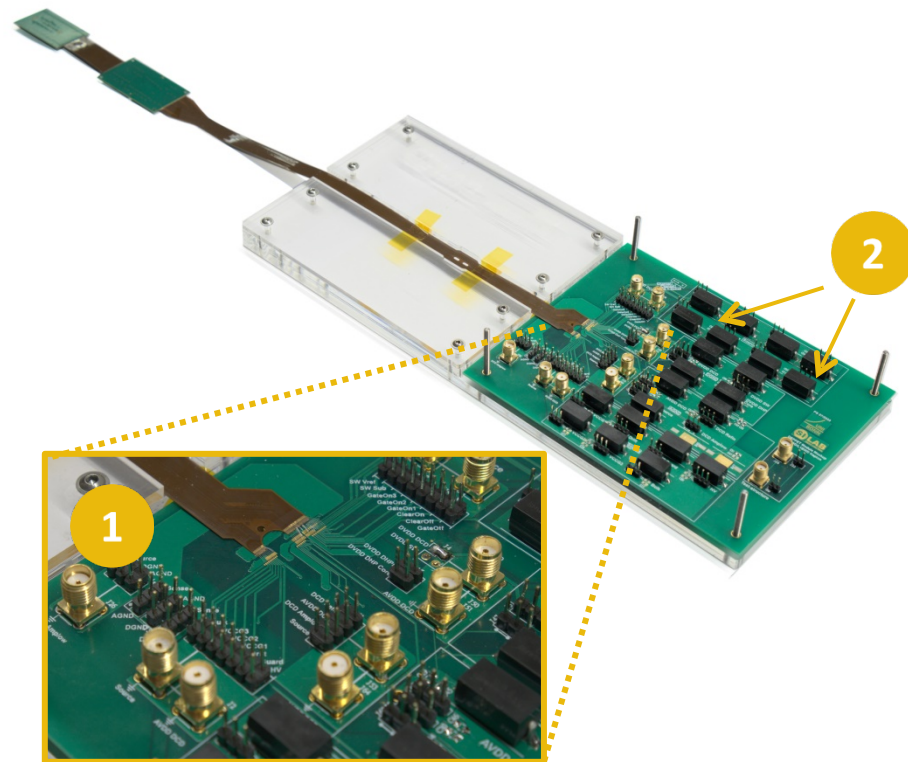
# SIGNAL PATH



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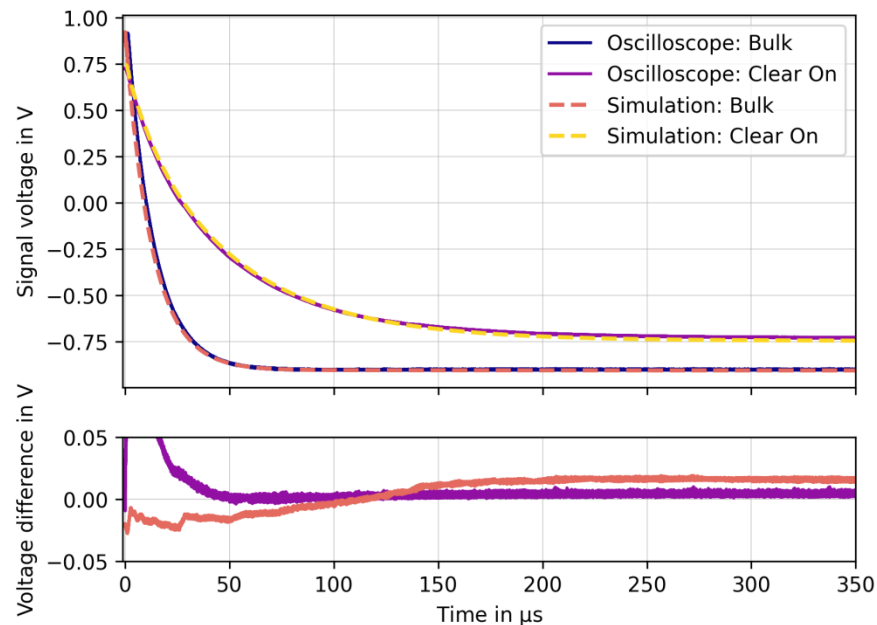
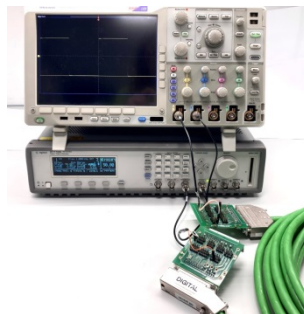
# MODULE MOCKUP

- Verification of simulation: **Module mockup PCB**
  - Connection to all of the lines of Kapton **1**
    - Wire bonding necessary
  - Module mockup **2**
    - Resistors and capacitors mimic module properties after the Kapton connection

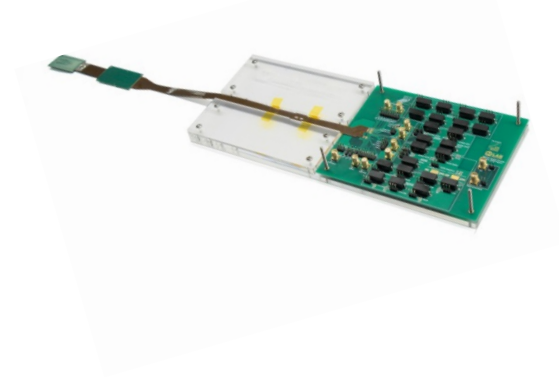
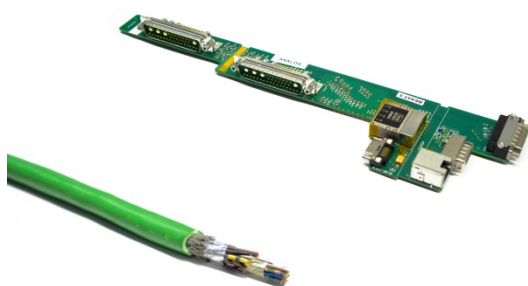
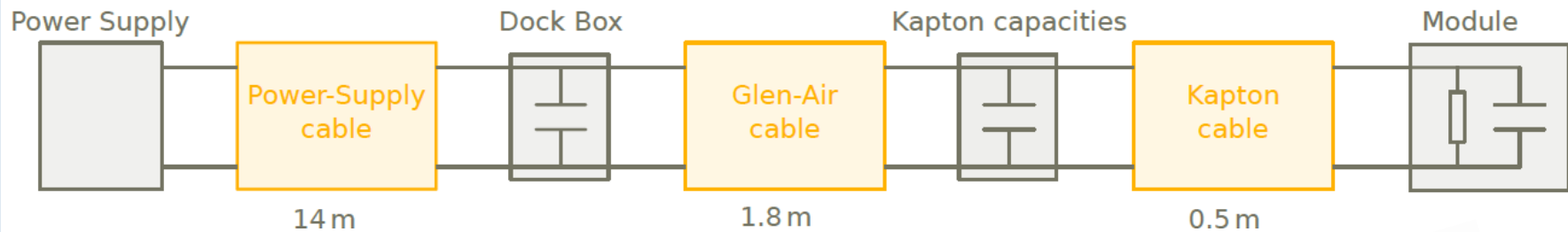


# FULL CABLE PATH: POWERING OF TWO LINES

- Simulated with HyperLynx
- PXD PS is not simulated
- Not only powered lines need to be simulated because of **capacitive coupling**
- Replication of load with custom made PCB
- Compared to reference measurement
- Average voltage deviation:
  - Bulk line.: 8.7 mV
  - Clear On line: 13.26 mV



# SIGNAL PATH

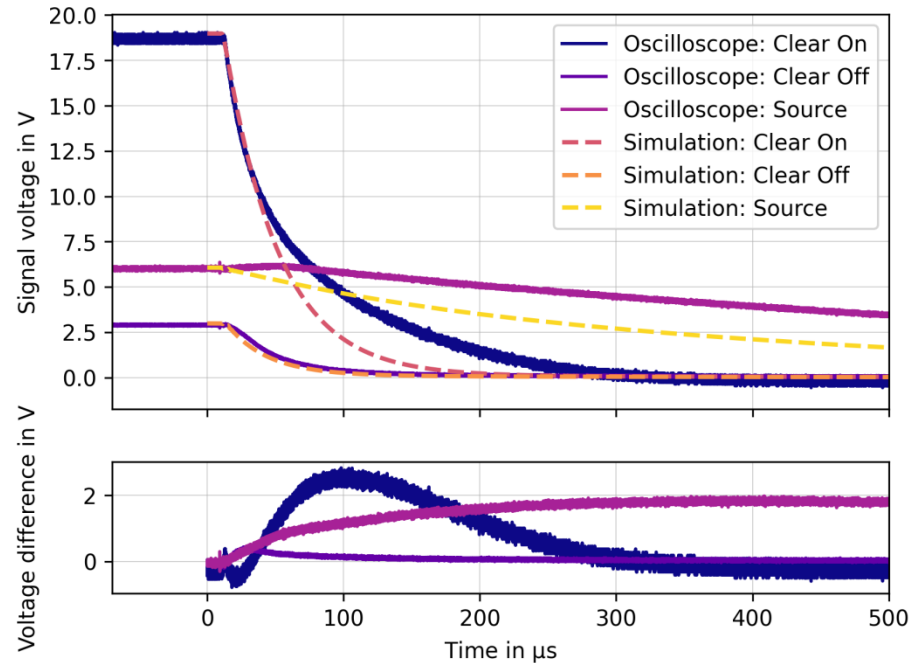
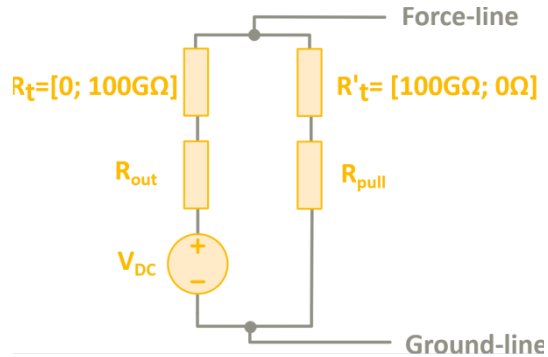


[1]

# SHUTDOWN PROCEDURE

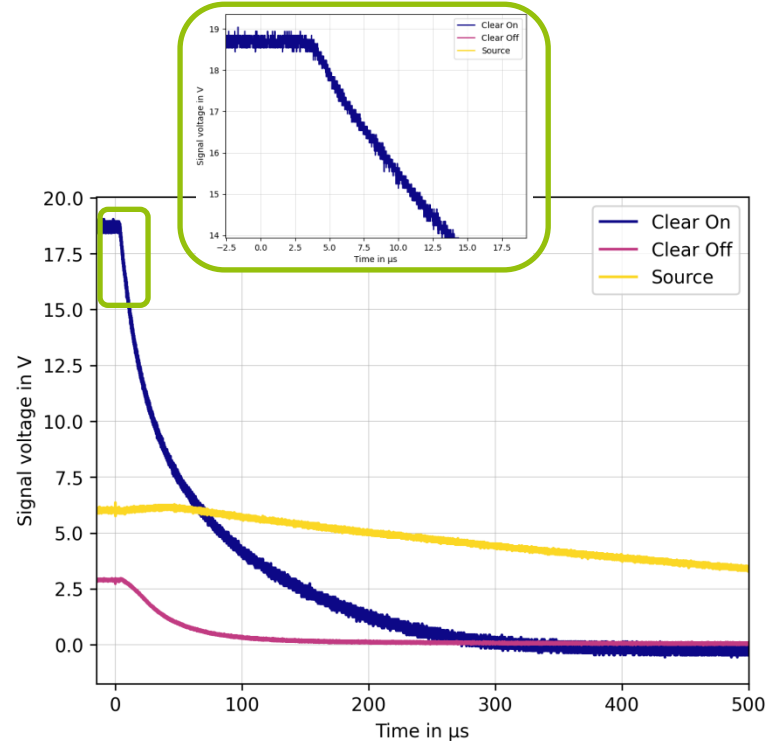
## ACTIVE SHUTDOWN

- Active shutdown → **short** force and ground line
- Simulate by **time dependent resistor** which switches from  $100\text{ G}\Omega$  to  $0\text{ }\Omega$



# ACCELERATION OF FAST SHUTDOWN

- Two areas for improvement:
  - Clear-On signal only drops slowly
    - generate steeper curve
  - Signal starts dropping  $\sim 4\mu s$  after the shutdown-signal was sent
    - decrease reaction time



1

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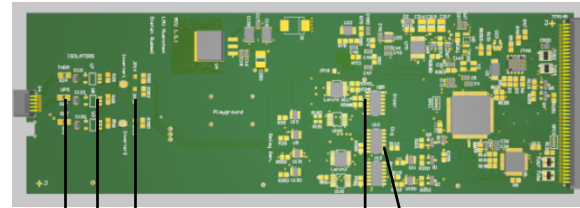
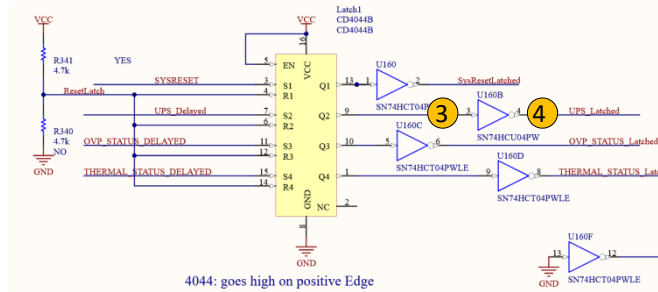
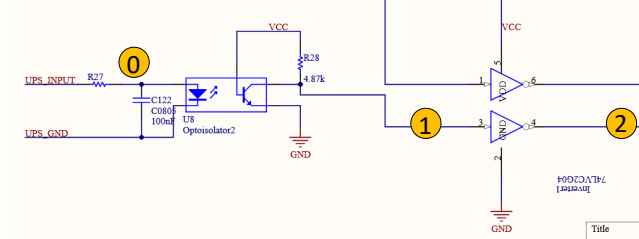
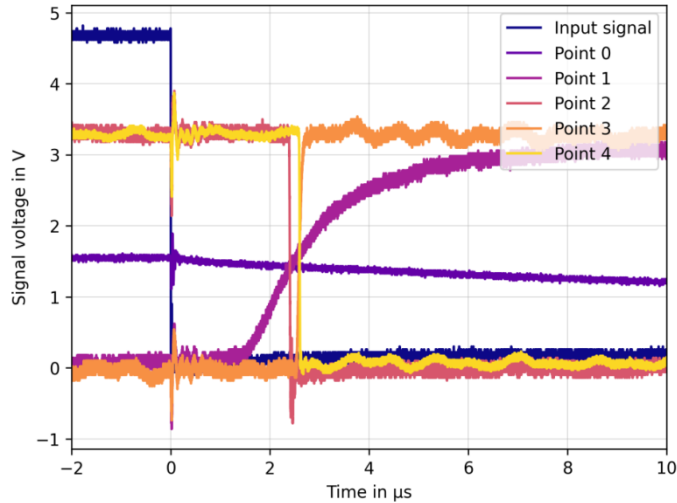
Lab-test: Fast-Shutdown signal transm.

4

Lab-test: Fast-Shutdown board modification

# TRANSMISSION OF SHUTDOWN SIGNAL

- 0 after R27
- 1 after optocoupler (PS8101-F3-A)
- 1 after inverter (74LVC2G04)
- 2 after NAND latch (CD4044B)
- 3 after inverter (SN74HCU04PW)
- 4 after inverter (SN74HCU04PW)



1

Motivation

2

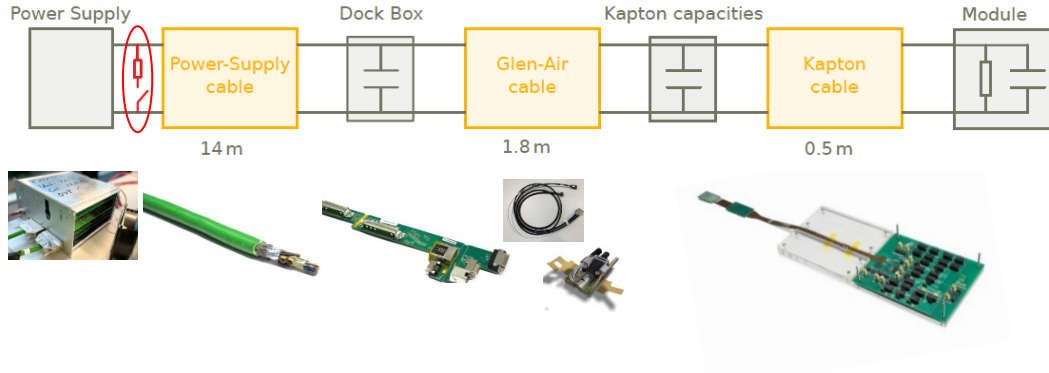
Simulation of PXD signal path

3

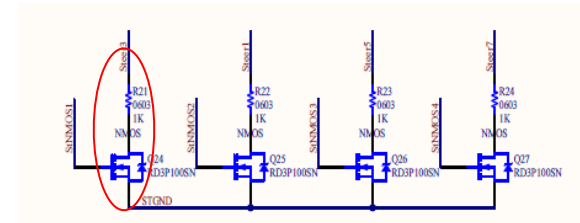
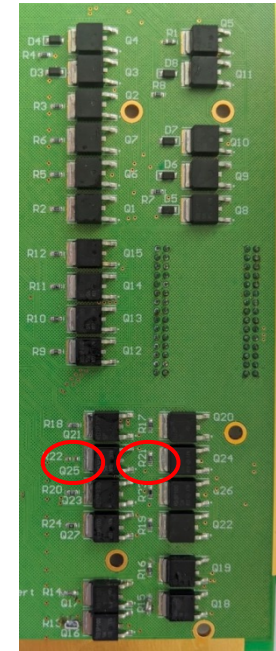
Lab-test: Fast-Shutdown signal transm.

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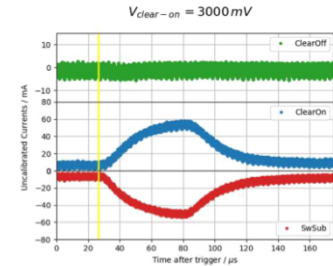
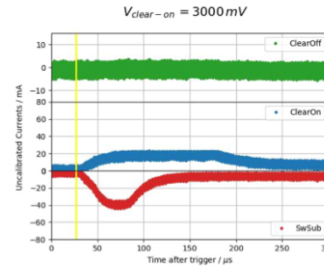
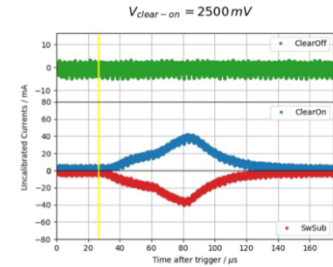
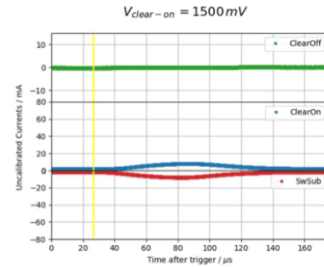
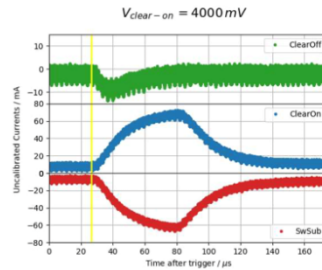
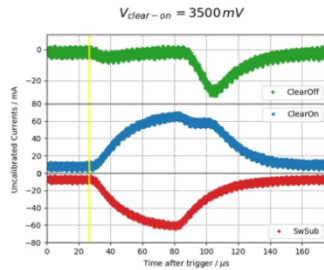
Lab-test: Fast-Shutdown board modification



- **How can the shutdown-time be influenced?**
- PS + Full cable path + Module Mockup
- External signal supplies fast shutdown signal
- Oscilloscope + active probes
- Measure Clear On and Clear Off voltage during fast shutdown with varying resistor values  $R_{on}$  and  $R_{off}$

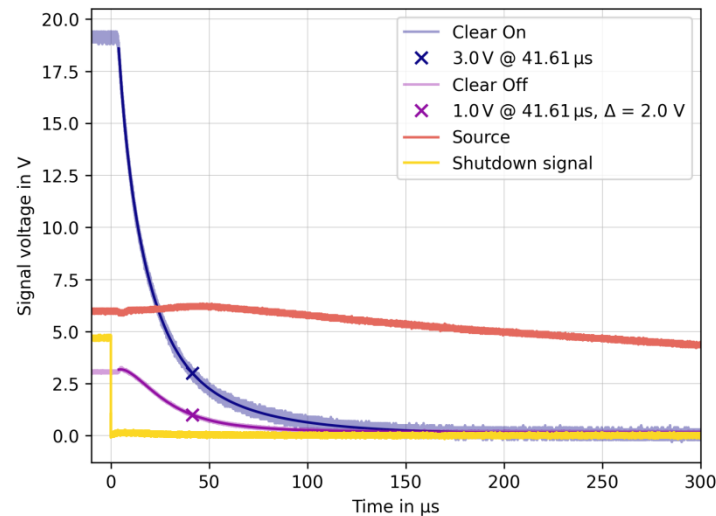


- Measured current in switcher (Clear On, Clear Off) for varying applied Clear On voltages
- Below  $V_{on} = 3V$ : no current flow between Clear On and Clear Off  $\rightarrow$  switcher is deemed 'safe'



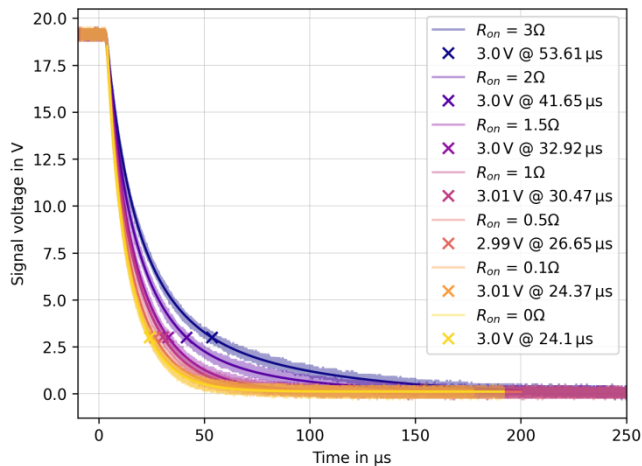
# EXEMPLARY MEASUREMENT

- $R_{on} = 2 \Omega$ ,  $R_{off} = 5 \Omega$
- 3V-limit
  - Showed earlier: starting at  $V_{on} = 3V$ , the modules seemed safe from irradiation
  - Time, at which Clear On voltage drops below 3V
  - Voltage of Clear Off at that time + voltage difference  $\Delta$
- Fast-Shutdown board only pulls down Clear voltages -> Source voltage drops much slower

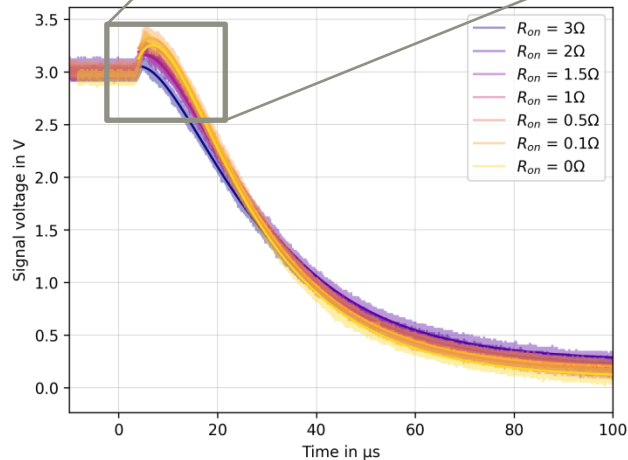


# INFLUENCE OF $R_{ON}$

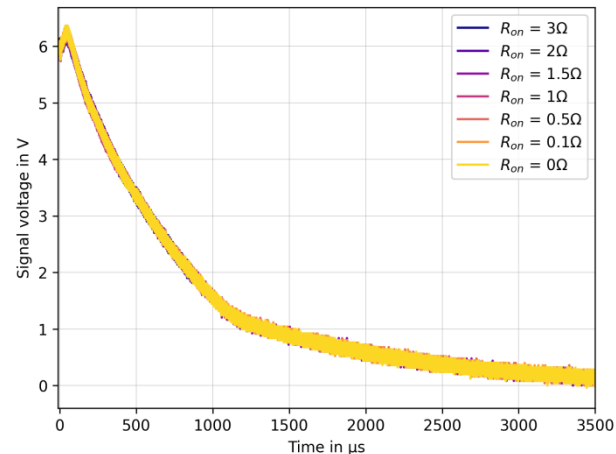
Clear On voltages during Fast shutdown,  $R_{off} = 5 \Omega$



Clear Off voltages during Fast shutdown,  $R_{off} = 5 \Omega$



Source voltage during Fast Shutdown,  $R_{off} = 5 \Omega$

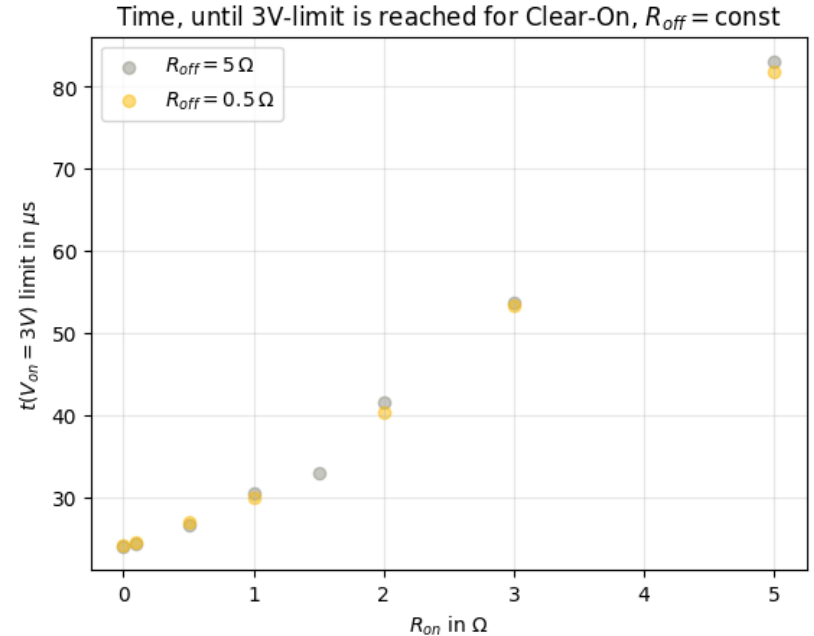


# DECAY TIME DEPENDENCE

- 3V-limit for different  $R_{on}$  values ( $R_{off} = 5\Omega$  or  $R_{off} = 0.5\Omega$  fixed)
- Would expect linear behaviour?

$$U = U_0 * \exp\left(-\frac{t}{RC}\right) \rightarrow R = -\ln\left(\frac{3}{19}\right) * \frac{1}{C} * t$$

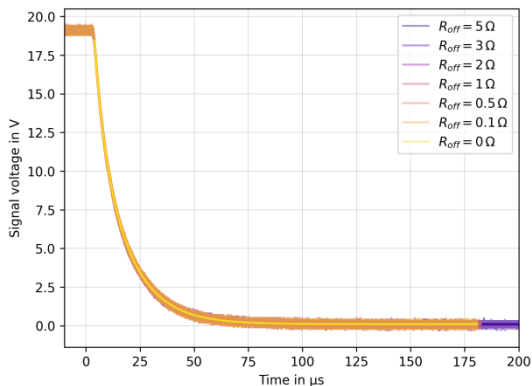
- Influence of regulator circuit in PS?



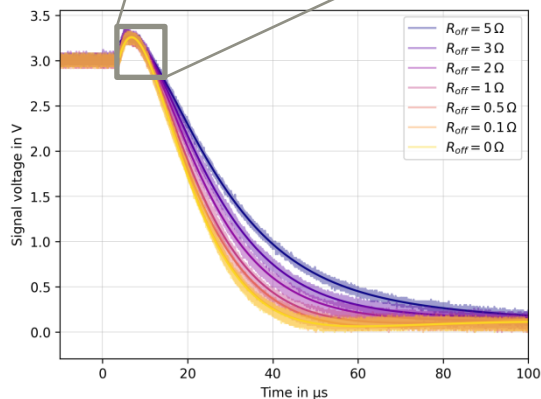
# INFLUENCE OF $R_{OFF}$

- Pull-Down Resistor studies
- Finished measurements with different  $R_{on}$  and  $R_{off}$  values
- Here: impact of  $R_{off}$ :  $R_{on} = 0.5 \Omega$

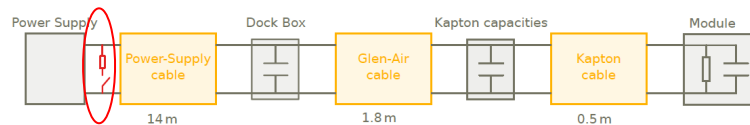
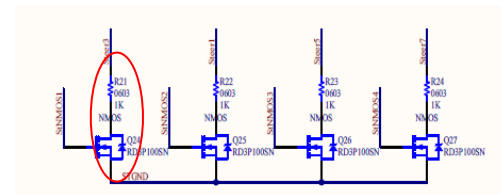
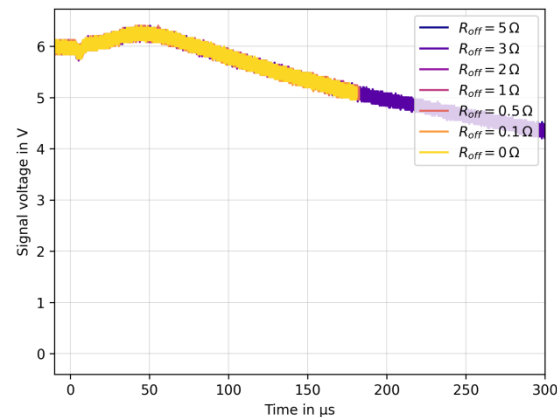
Clear-On voltages during Fast shutdown,  $R_{on} = 0.5 \Omega$



Clear-Off voltages during Fast shutdown,  $R_{on} = 0.5 \Omega$

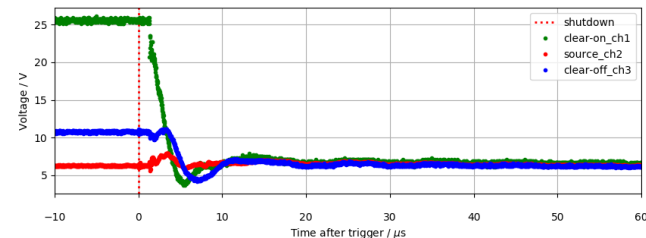


Source voltages during Fast shutdown,  $R_{on} = 0.5 \Omega$

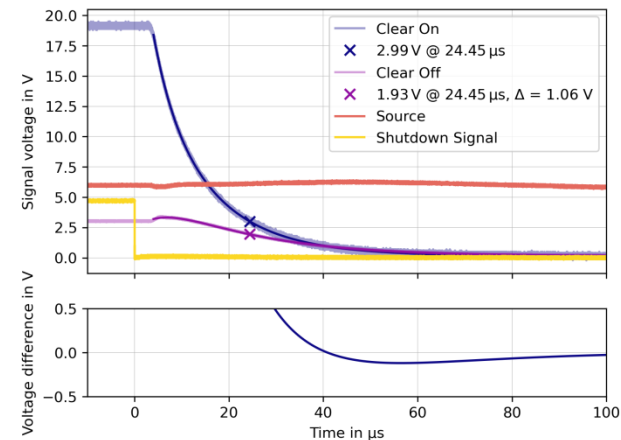


$$V_{ON} < V_{OFF} ?!$$

- Asic requirement: Clear On voltage should never drop below Clear Off voltage
- Could be observed in the past for  $R_{on} = R_{off} = 0\Omega$ 
  - Measured on Hybrid5 (full system demonstrator)
  - Not full cable path included → less realistic
- So far: observed with  $R_{off} = 5\Omega$  &  $R_{on} < 0.5\Omega$ 
  - Not as severe as before

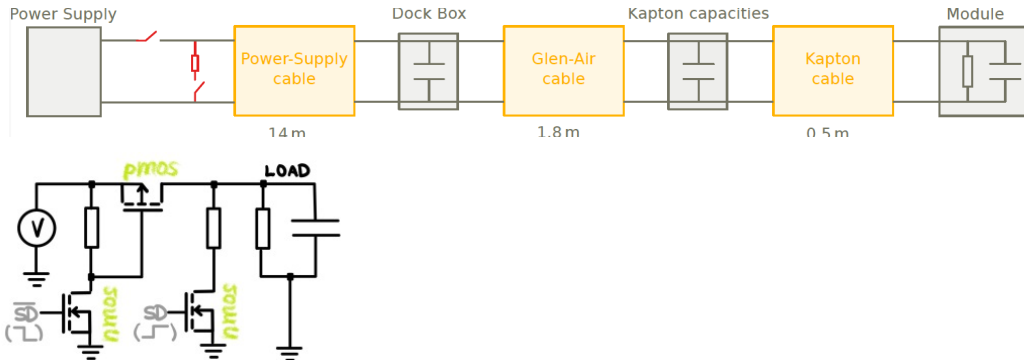


R-test: FAST shutdown | w/ probes ( $R_{on} = 0.1\Omega$ ,  $R_{off} = 5\Omega$ ); AGND grounded

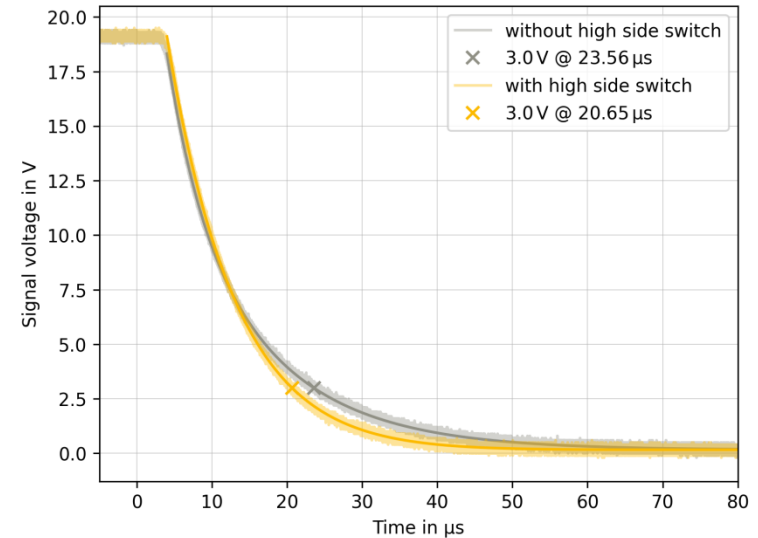


# NEW IDEA: HIGH SIDE SWITCH

- Separate PS from load by implementing a switch in series
- Reduce influence of regulator inside of PS
- Shown design only works for positive, high enough voltages
- Pmos steered via nmos
- Faster shutdown of Clear-On voltage due to high side switch?

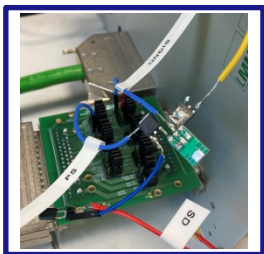


Active shutdown: Clear On vs Source

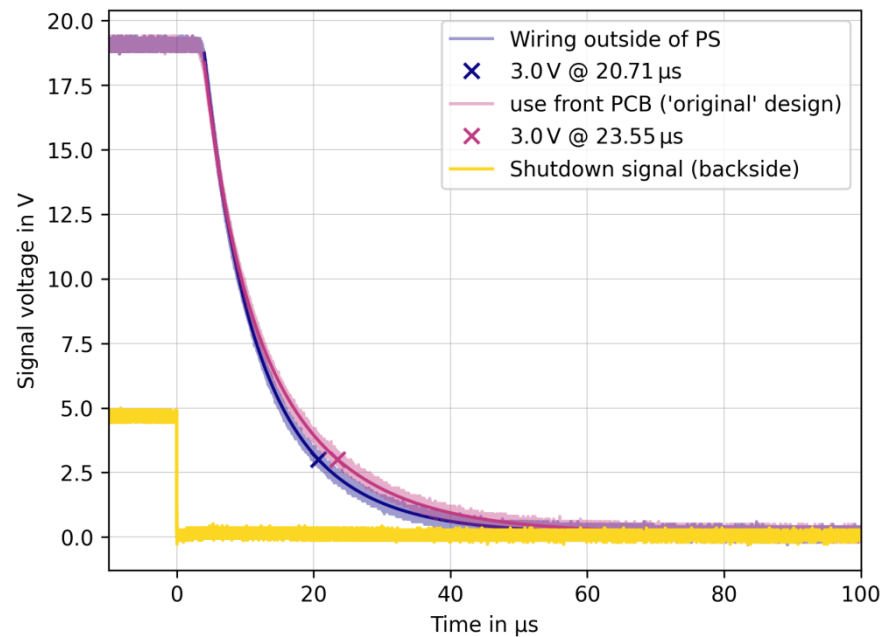
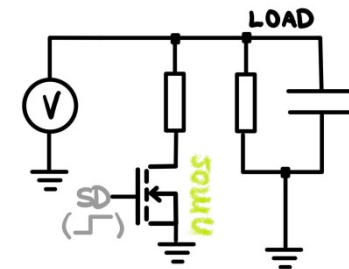
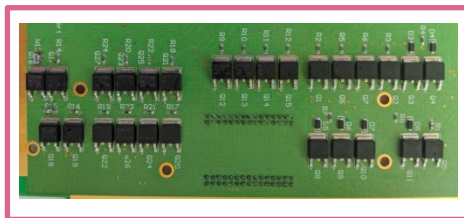


# INFLUENCE OF FRONT PCB

- Sped up fast shutdown seems to come from **not using front PCB**, not from opening the force line
- Assumptions:
  - Resistance of traces on front PCB?
  - Inductance of traces on front PCB?

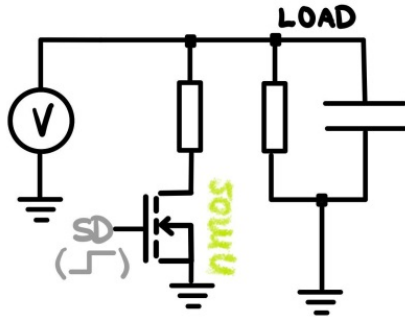


VS

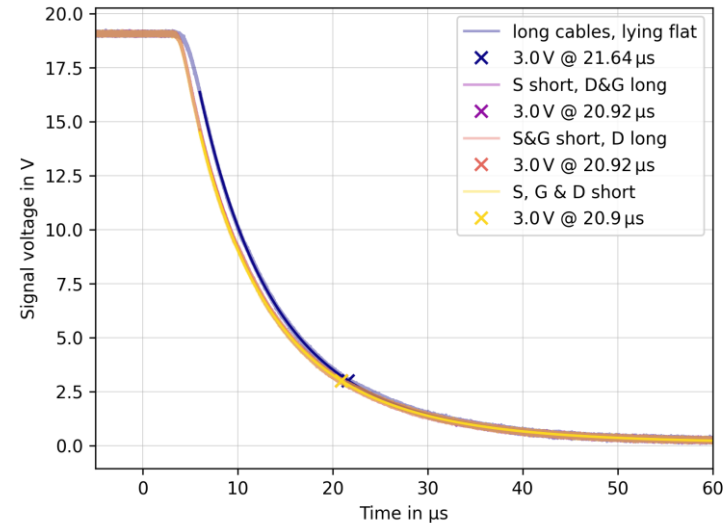


# INFLUENCE OF CABLE PARAMETERS

- Test fast shutdown of Clear On with different cable lengths for drain, gate and source of nmos
- Fast shutdown implemented outside of PS, not on fast shutdown board
- Cable length (resistance?) plays a role
- Inductance plays a role, measurements still ongoing



Clear On - Fast shutdown outside of PS; no high side switch  
varying long cables for Gate (G), Drain (D) and Source (S), AGND grounded



# SUMMARY AND CONCLUSION

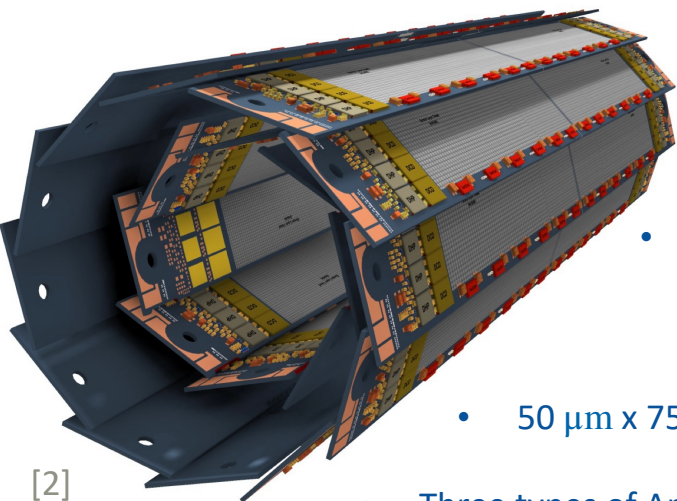
- Fast shutdown → avoid PXD damage due to beam loss events
- Simulation of PXD powering net
- Discrepancies between simulation and measurement for **Power Supply**
- **Lab-tests:**
  - Varying combinations of pull-down resistors
  - Faster transmission of shutdown signal within Power Supply

- Test Beam Campaign at MAMI in October 2025?
- Production of new Fast Shutdown boards
- Installation at KEK (summer 2026?)

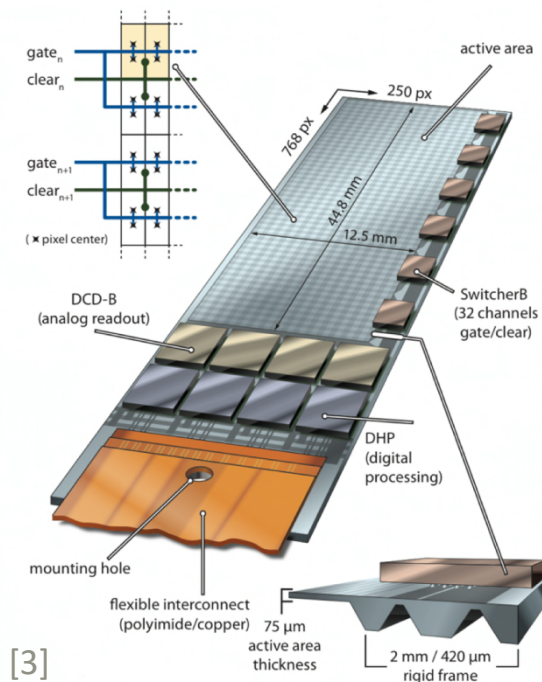
**THANK YOU!**

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# BELLE II PIXEL DETECTOR (PXD)

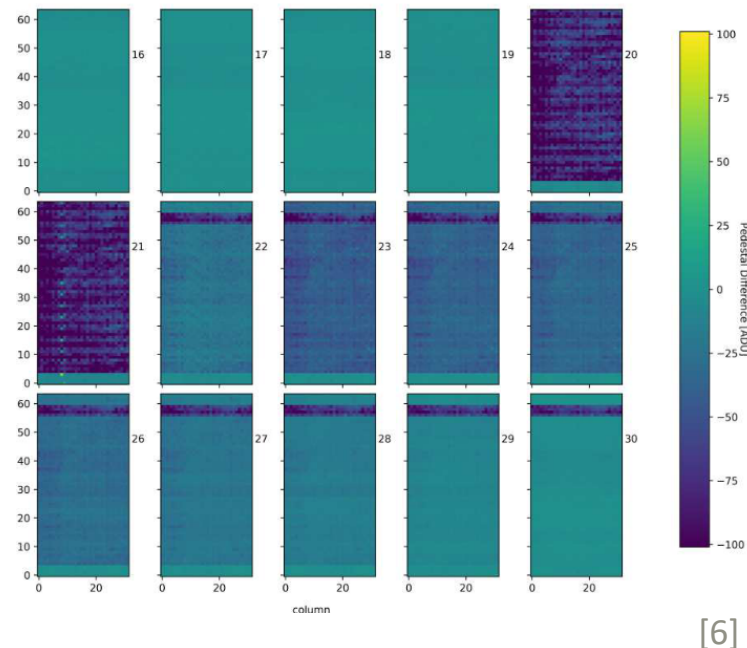
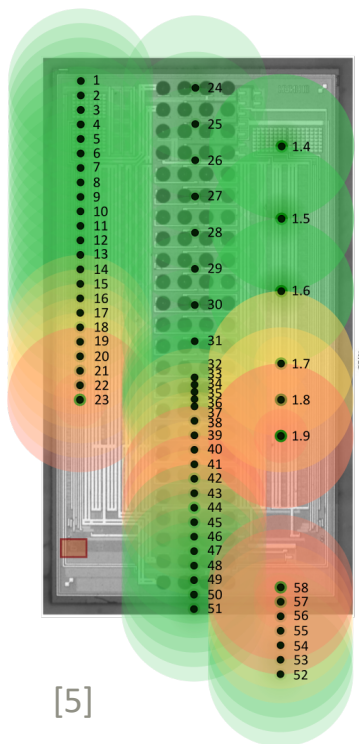


- PXD: two layers of DEPFET (Depleted Field Effect Transistor) modules at radii of 14 mm and 22 mm
- 50  $\mu\text{m}$  x 75  $\mu\text{m}$  pixels thinned to 75  $\mu\text{m}$
- Three types of Application Specific Integrated Circuits (ASICs) are responsible for readout:
  - DCD, DHP, **Switchers**



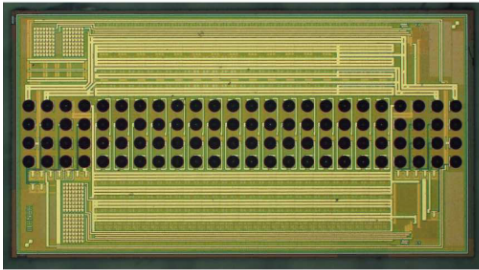
# CONFIRMATION OF RESULTS

- Irradiation with electron beam
- Fine scan of ASIC area
  - July 2020 with H5029
  - Colour coded measurement points
  - red => permanent damage
- Raw data difference of 15 raw frames during injection
  - Second to last Switcher channel is damaged permanently
- Switcher only vulnerable when turned on

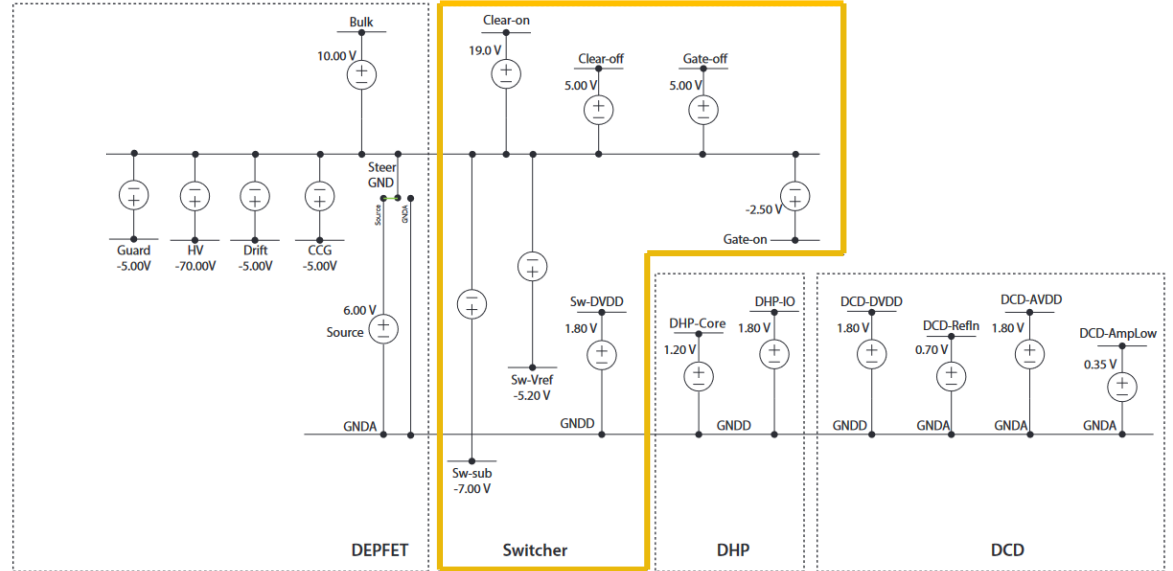


# POWERING SCHEME

- Dedicated power-up and power-down sequence
- Range between +19V and -7V
- Switcher switches between high voltages



[7]



[8]

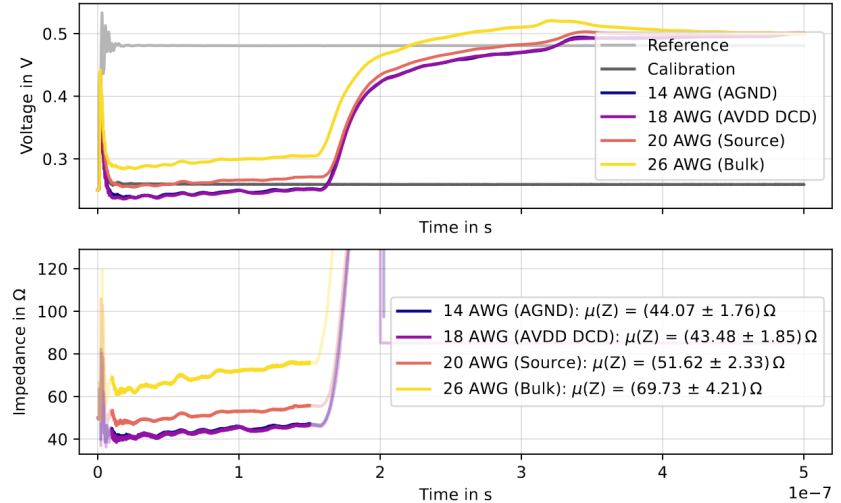
# DELAY TIME AND IMPEDANCE

- Needed for Simple Line model (HyperLynx)
- **Impedance profile:** view cable as cascade of cable segments
  - Reflection at cable connection
  - Average over cable length
  - Rise in impedance due to DC-resistance
- **Delay time:**  $\tau_l = (75.5 \pm 0.5) \text{ ns}$

## Simple Line

→ HyperLynx

- Impedance
- Delay time
- DC-Resistance

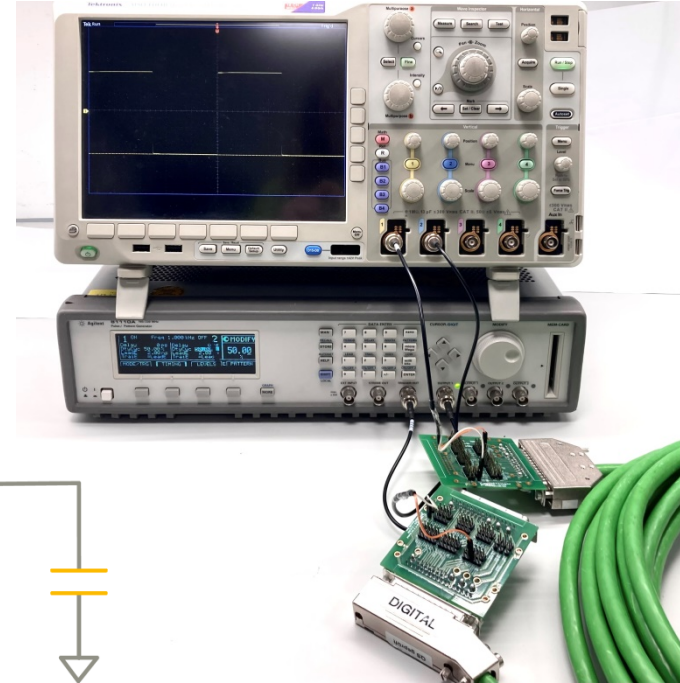
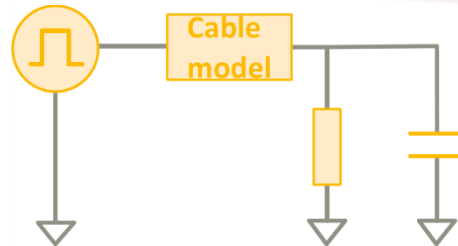


$2 \cdot \tau_l$



# REFERENCE MEASUREMENT

- **Measurement** to compare against simulation
  - **Falling edge** of a squared pulse
  - View transmitted signal on oscilloscope
- Verify each cable segment **individually**
- For quantification:
  - Compute **difference in voltage** between simulation and measurement data



# SHUTDOWN PROCEDURE

## PASSIVE SHUTDOWN

- Passive shutdown → **separate** force line from power supply
- Simulate by **time dependent resistor** which switches from  $0\ \Omega$  to  $100\ \text{G}\Omega$
- Time constant in simulation too big

