DEPFET X-RAY IRRADIATION STUDIES

Belle II Germany Meeting
Bonn
09.09.2025

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UNIVERSITÄT BONN

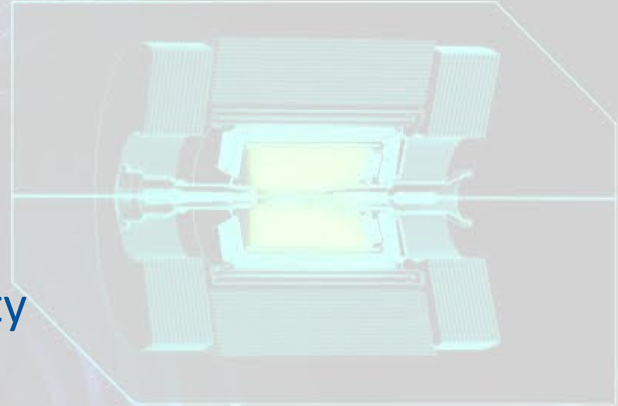
FTD

SI LAB Silizium Labor Bonn

bmb+f - Förderschwerpunkt Elementarteilchenphysik Großgeräte der physikalischen Grundlagenforschung

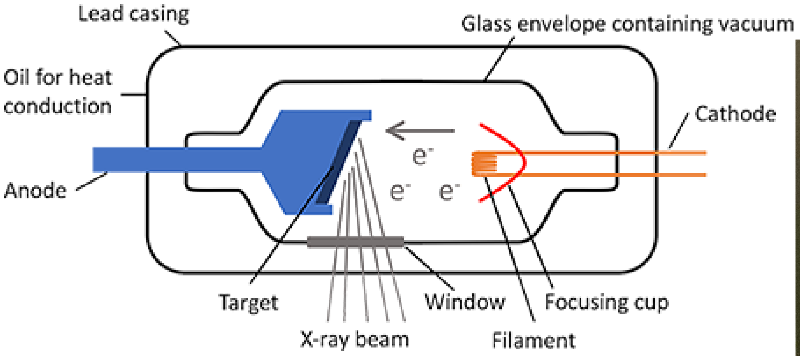
JENNIFER2 EU grant n.822070

OVERVIEW

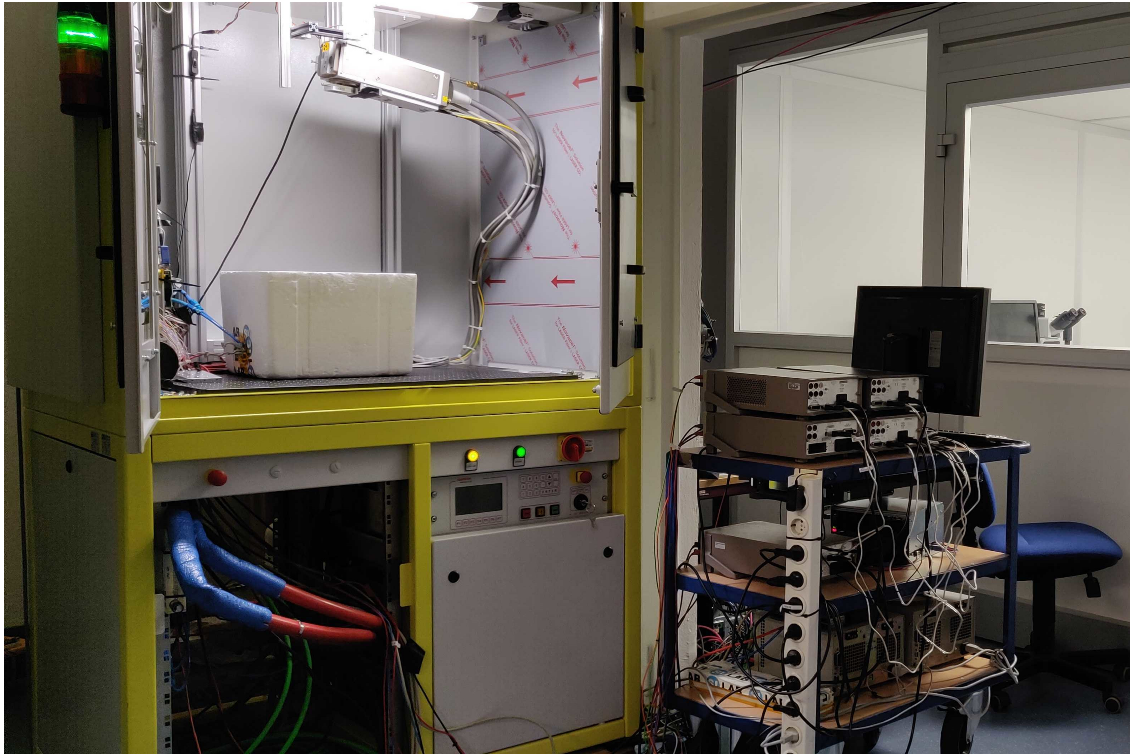


- Introduction
  - Bonn X-ray Irradiation Facility
  - X-ray Dosimetry
- X-ray Irradiation Damage in DePFET
  - Front side
  - Backside
- Measurements and Results
- Summary and Outlook

BONN X-RAY IRRADIATION FACILITY

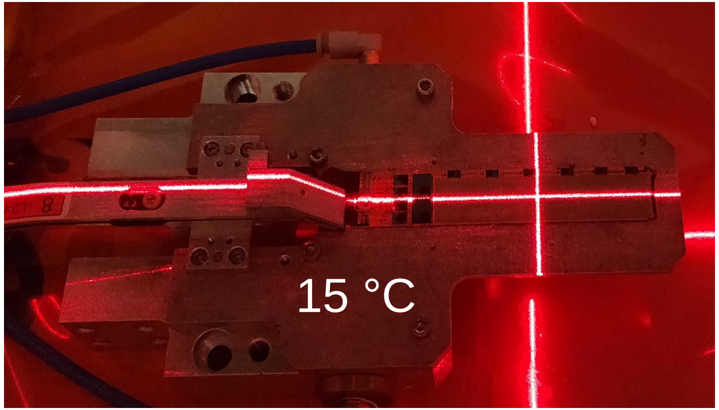


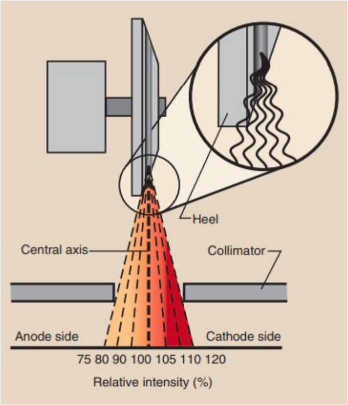
- X-ray setup in Bonn
- X-ray tube settings:
  - V_{tube} = 40 kV
  - I_{anode} = 50 mA
- Characteristics:
  - Tungsten target
  - Al filter (150 µm)
- Water-cooled

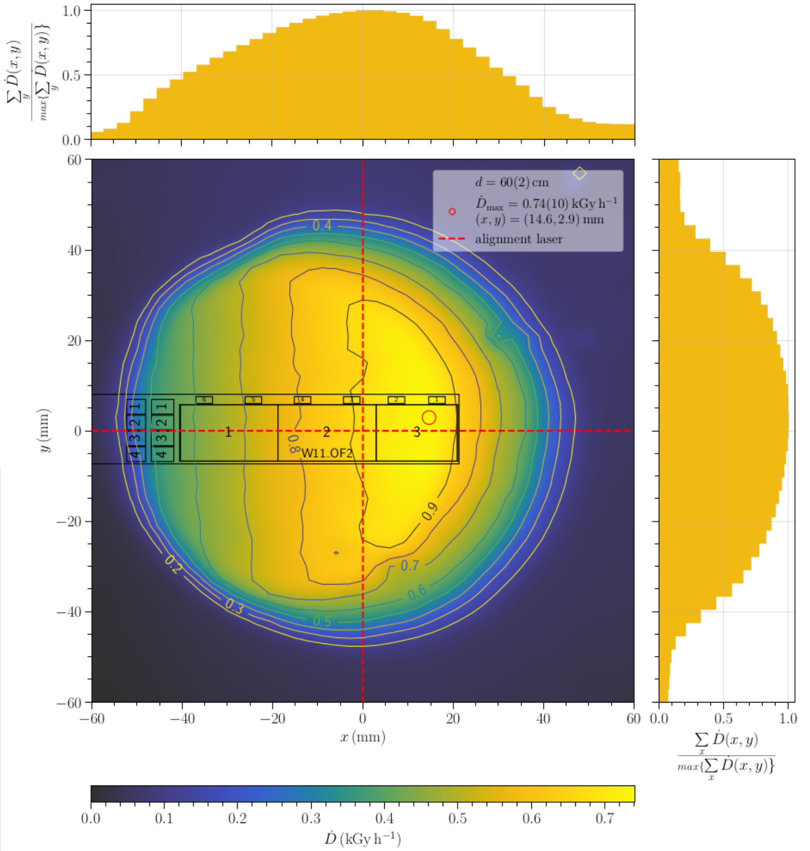


X-RAY DOSIMETRY

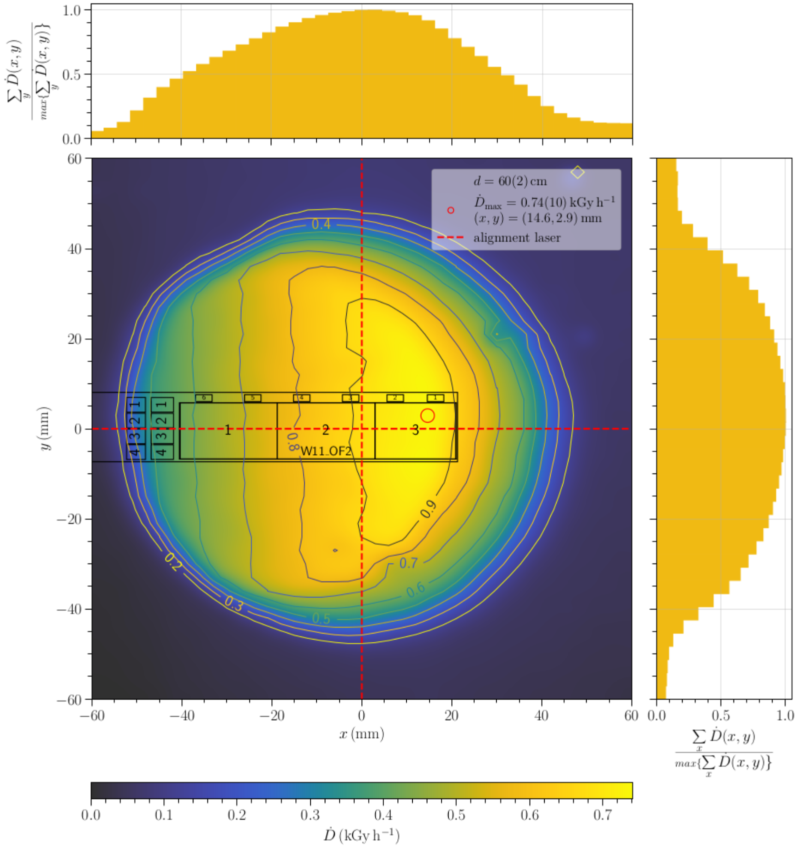
- Beam profile measured with a photodiode
- Anode heel effect → Inhomogeneous beam profile
  - Different dose for different module area → Different ΔV_{th}
- Independent V_G and V_{CCG} steering in three regions
- Total Ionizing Dose (TID) up to **~18 Mrad** in the DEPFET SiO_2
  - **Expected lifetime (10 years) exposure of the PXD is ~20 Mrad**

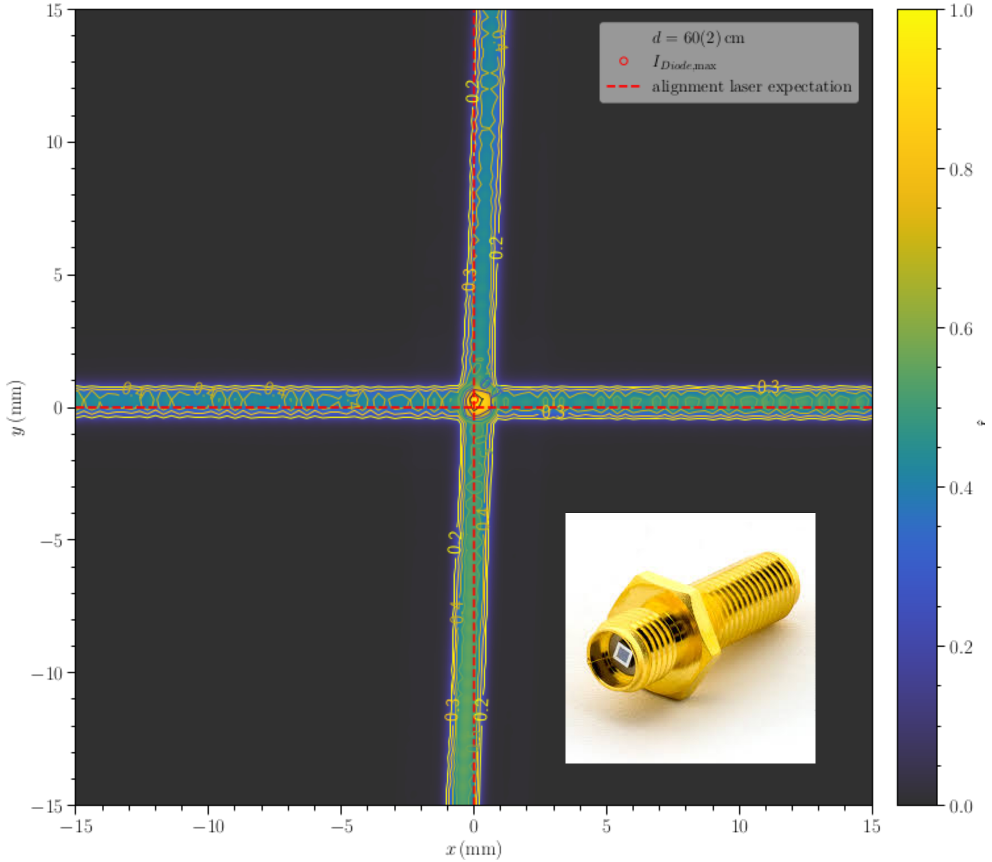






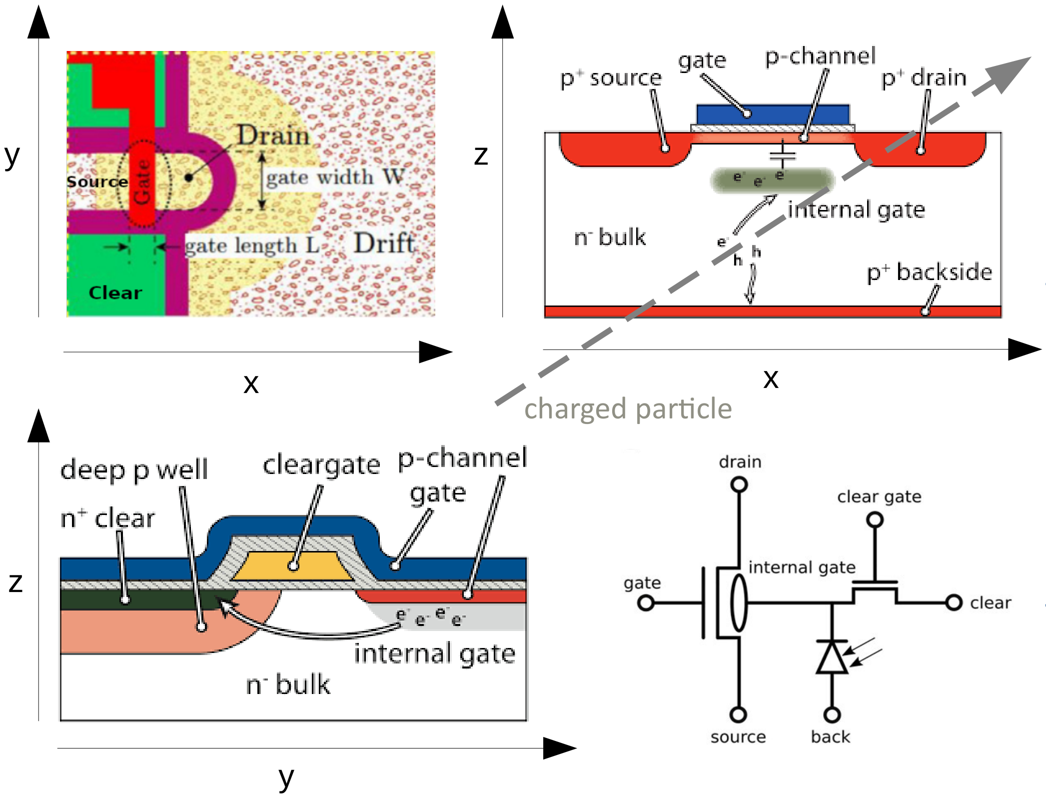
PHOTODIODE ALIGNMENT WRT THE LASERS





THE DEPFET STRUCTURE AND WORKING PRINCIPLE

Depleted P-channel Field Effect Transistor (DePFET)

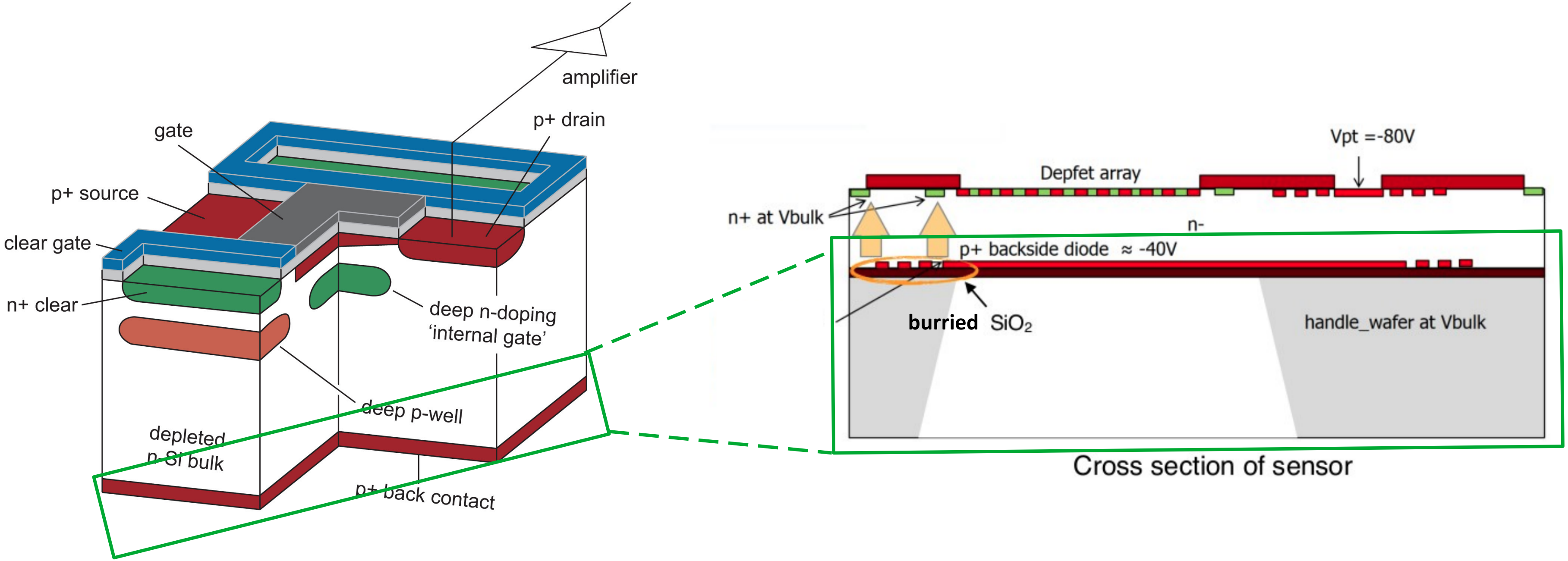


1. p-channel MOSFET operated in saturation
   - $V_{GS} > V_{th}$ and $V_{DS} \geq V_{GS} - V_{th}$
   - V_{GS} modulates I_{DS}

V_{GS}: gate voltage
V_{th}: threshold voltage
V_{DS}: drain-source voltage
I_{DS}: drain current

2. Internal gate
   - Fast charge collection (*O*(ns))
   - Additional I_{DS} modulation → Signal
   - $g_q = \frac{\partial I_D}{\partial q} \approx 750 \frac{pA}{e^-}$
3. Additional FET for clear mechanism
   - Directly connected to internal gate
   - Large positive voltage applied to clear → empties internal gate

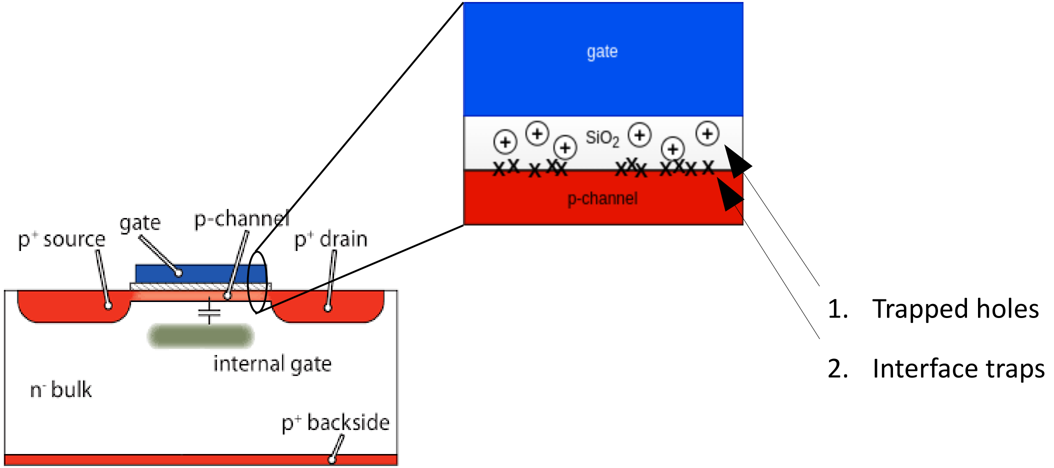
DEPFET BACKSIDE



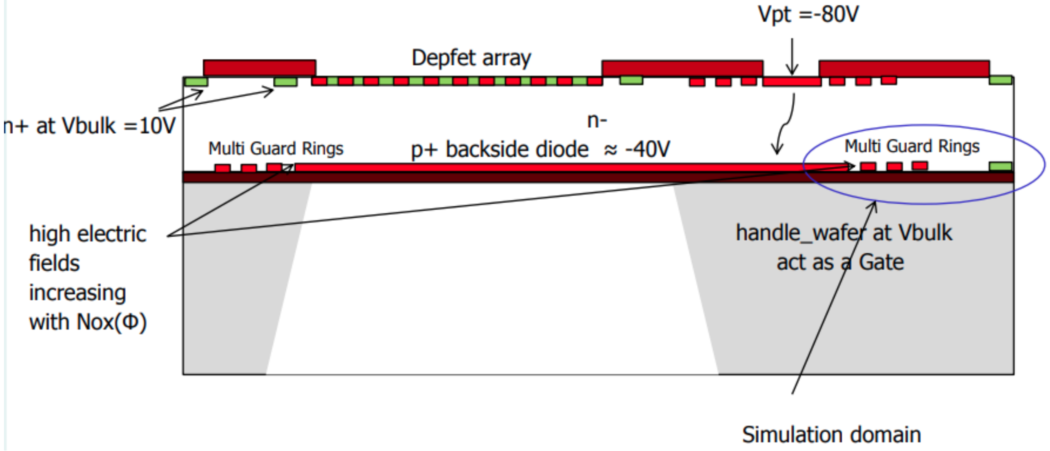
- Sensor depletion via Punch-through (PT or HV) contact
- Guard-ring structure surrounding the backside implant
- Guard-ring structure floating to ensure smooth electric field reduction towards the edge of the sensor

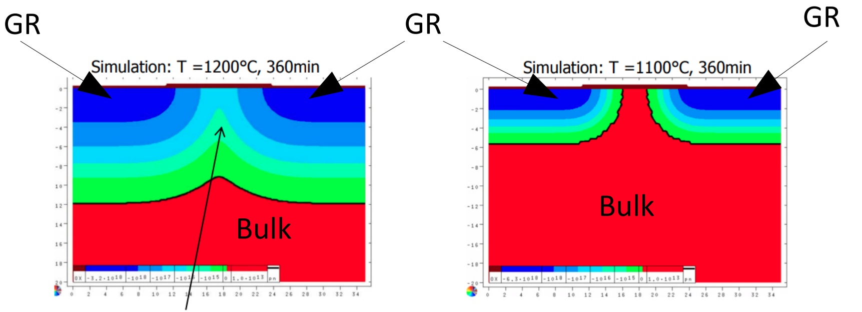
SURFACE RADIATION DAMAGE IN DEPFET

- X-ray irradiation → e-h pairs → Oxide damage
  1. **Trapped holes** in the SiO_2 bulk due to their low mobility
  2. **Interface traps** at Si/SiO_2 interface
- **Internal E-field** creation due to charge build-up in the SiO_2 layer and Si/SiO_2 interface
- Interfaces affected:
  - Front side SiO_2 layers
    - External gate oxide
    - Clear gate oxide
  - Burried SiO_2 under the p^+ backside



HIGH BACKSIDE CURRENTS WITH TID

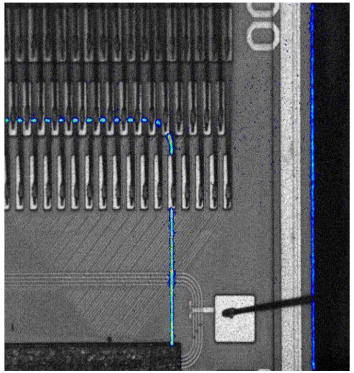




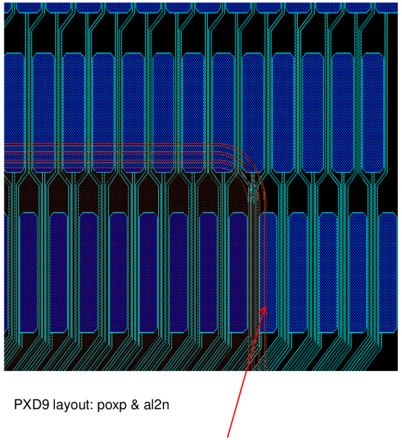
No n-doping, no space charge, no pot. barrier

some n-doping, some charge, weak pot. barrier

- *Secondary Ion Mass Spectroscopy (SIMS) + Simulation:* Extract dopant profile
- *Shorted guard rings*
- *Current understanding*: High electric fields at guard-ring structures → avalanche current multiplication → increased backside currents



Lens: x5
Camera: InGaAs



PXD9 layout: poxp & al2n

Break through at **outer most** guard ring!
(against all expectations)

Rainer Richter (2022), *DEPFET bulk currents in PXD*
24th International Workshop on DePFET Detectors and Applications

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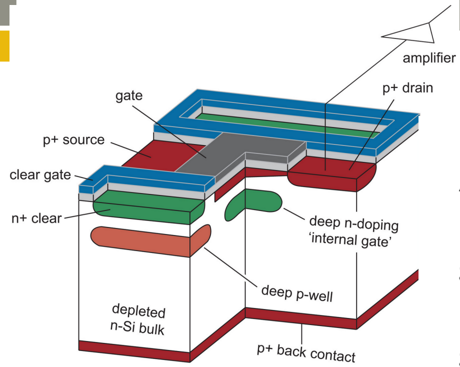
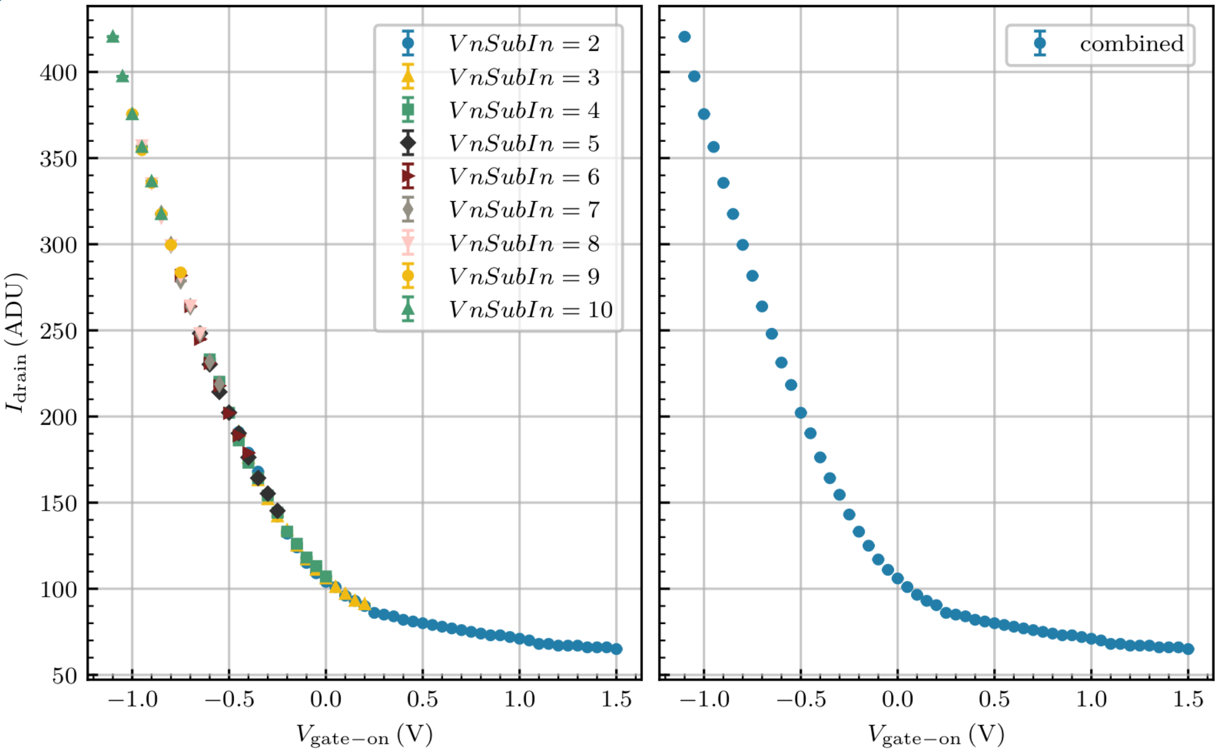
DEPFET GATE IV PER PIXEL

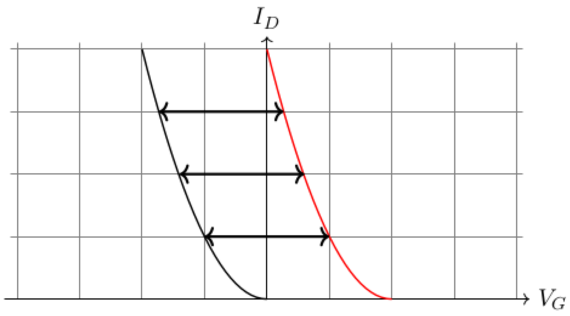


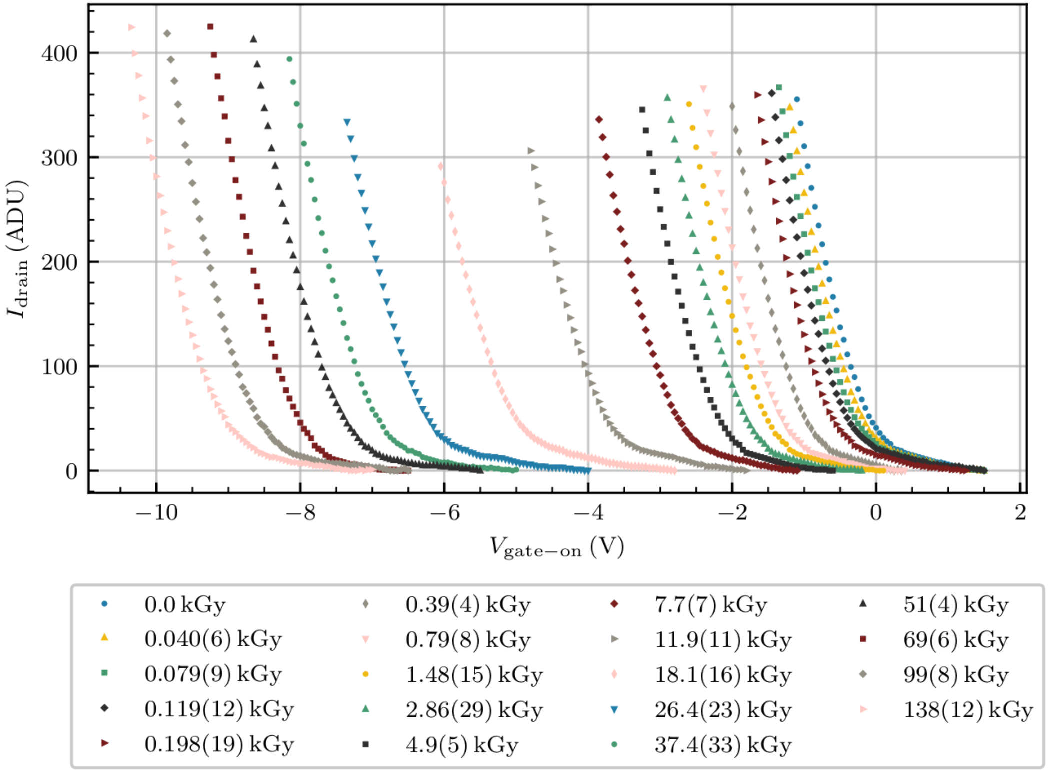
- Digitized drain current vs gate voltage
- DCD dynamic range not large enough to capture the entire IV
- Use a special DAC (VNSubIn) → Subtracts drain current before digitization
  - Capture of different IV part
- Stitch together all IV parts → final IV



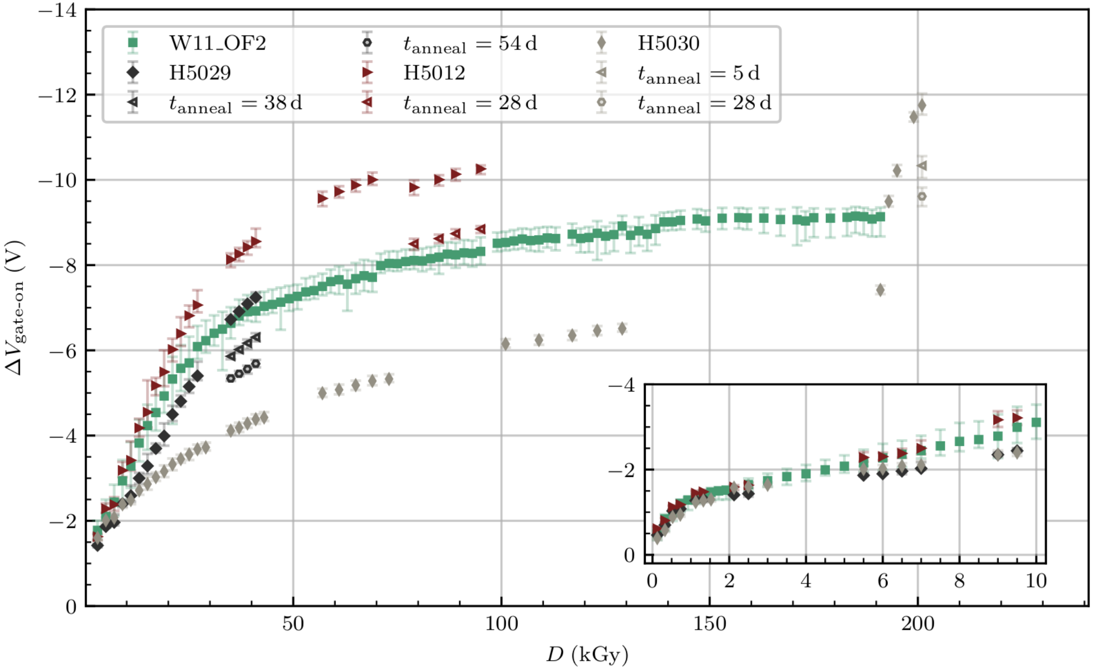
DEPFET GATE IV SHIFT WITH TID PER PIXEL

- IVs do not always have a nice shape, same baseline and clear threshold
  - Hard to find the exact gate threshold and then calculate threshold shift
- Instead compare the curves well after the threshold region



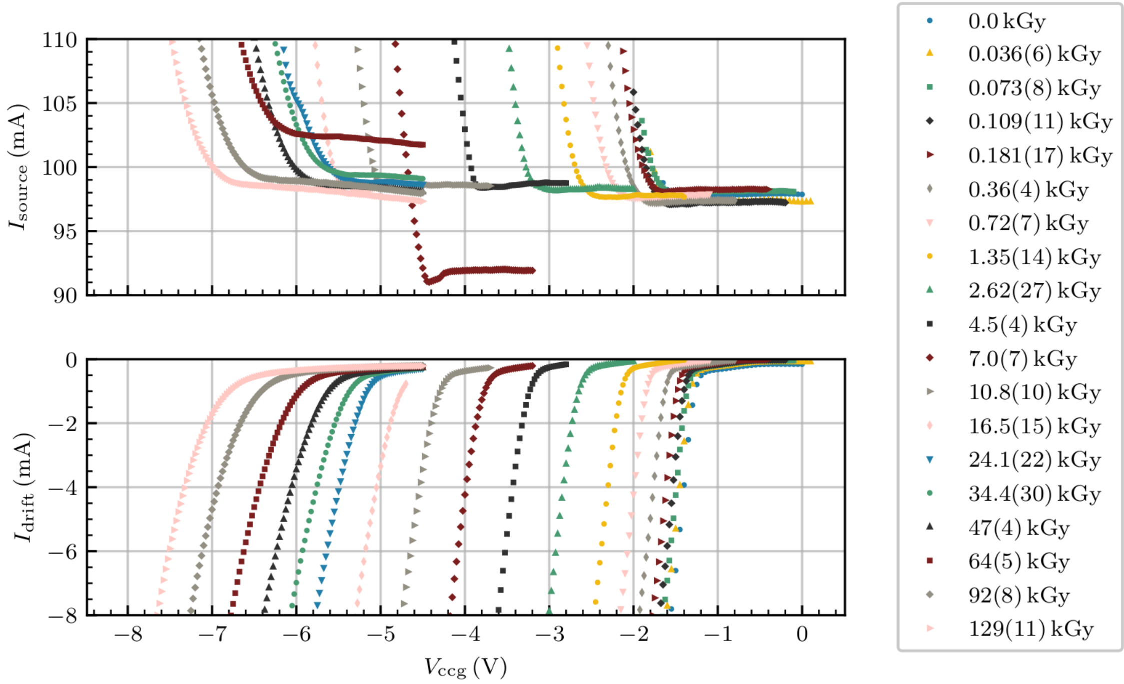


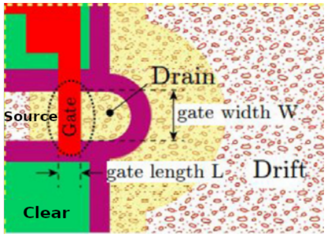
DEPFET GATE THRESHOLD SHIFT

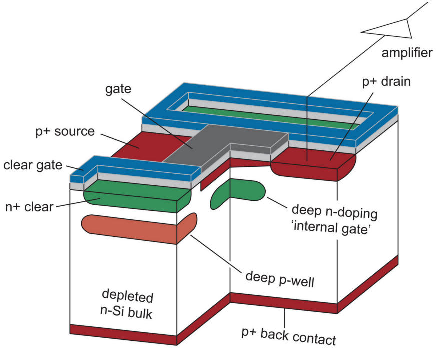


- W11-OF2 → full-scale module
- H50XY → prototype
- Every data point is the average of pixels with the same dose
- Dose rates:
  - W11-OF2: 0.42 kGy/h
  - H5012: 2.4 kGy/h (pre-irradiated with electrons)
  - H5029: 2.4 kGy/h
  - H5030: 2.4 kGy/h (irradiated in OFF)

CLEAR GATE IV SHIFTS PER AREA

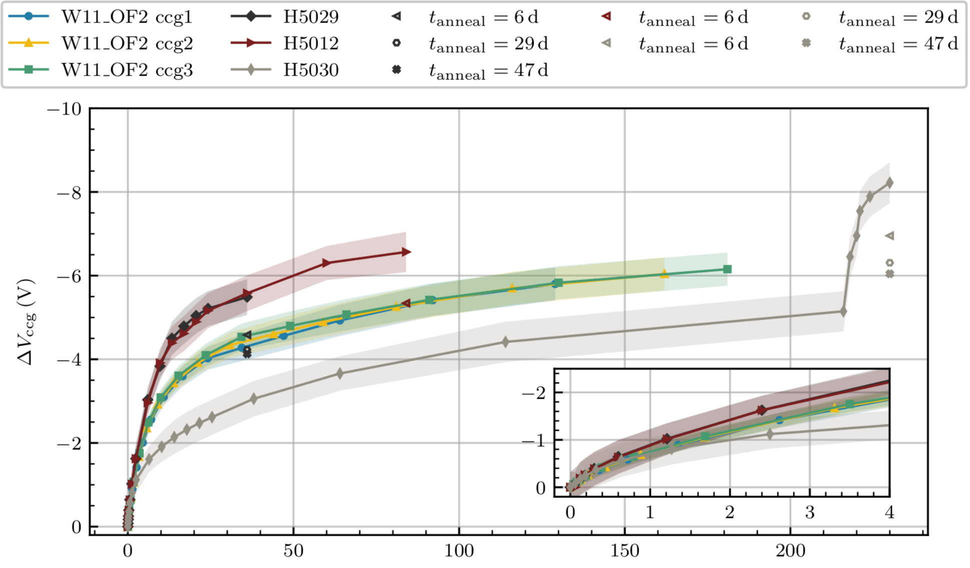


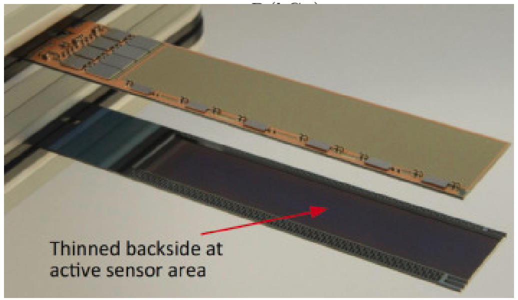




- For fresh DePFET module initial V_{ccg} = 0V
  - No current flowing to drift contact
- More negative V_{ccg} → Parasitic channels
- Same approach for shift calculation by looking at the drift IV shift

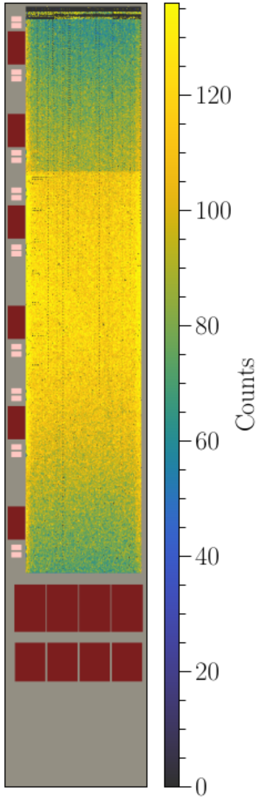
CLEAR GATE THRESHOLD SHIFT PER AREA

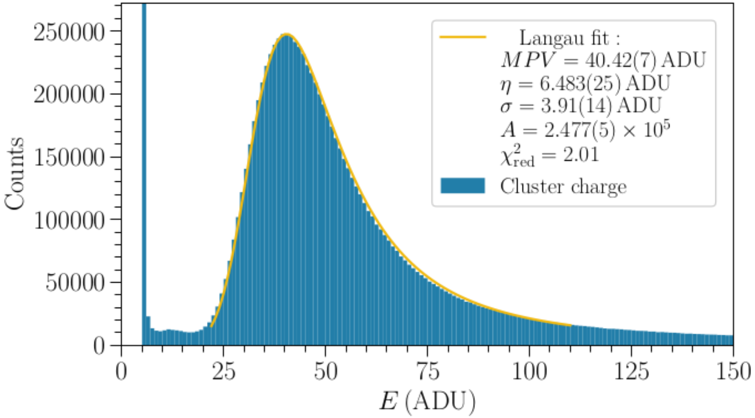


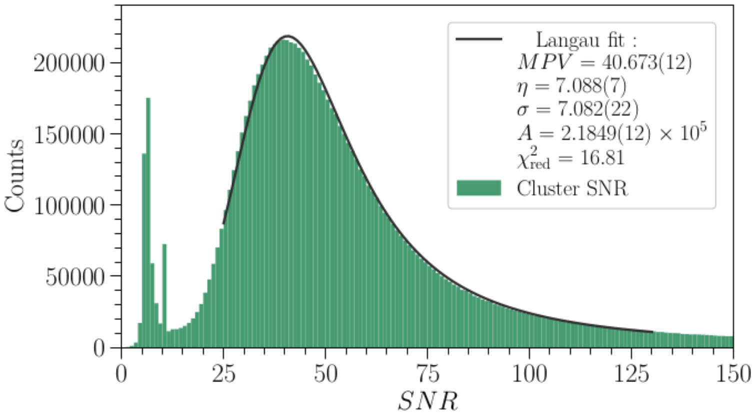


- W11-OF2 → full-scale module
- H50XY → prototype
- Every data point is the global IV shift of the matrix (prototype) or the voltage-controlled area (full-scale module)
- Dose rates:
  - W11-OF2: 0.42 kGy/h
  - H5012: 2.4 kGy/h (pre-irradiated with electrons)
  - H5029: 2.4 kGy/h
  - H5030: 2.4 kGy/h (irradiated in OFF)
- CCG threshold shift different from DePFET gate shift due to different oxide composition

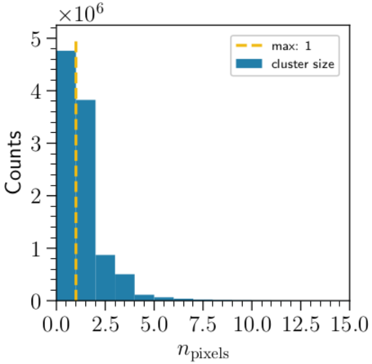
SOURCE SCAN SR90 ORIGINAL HV (-58V) UNIRRADIATED





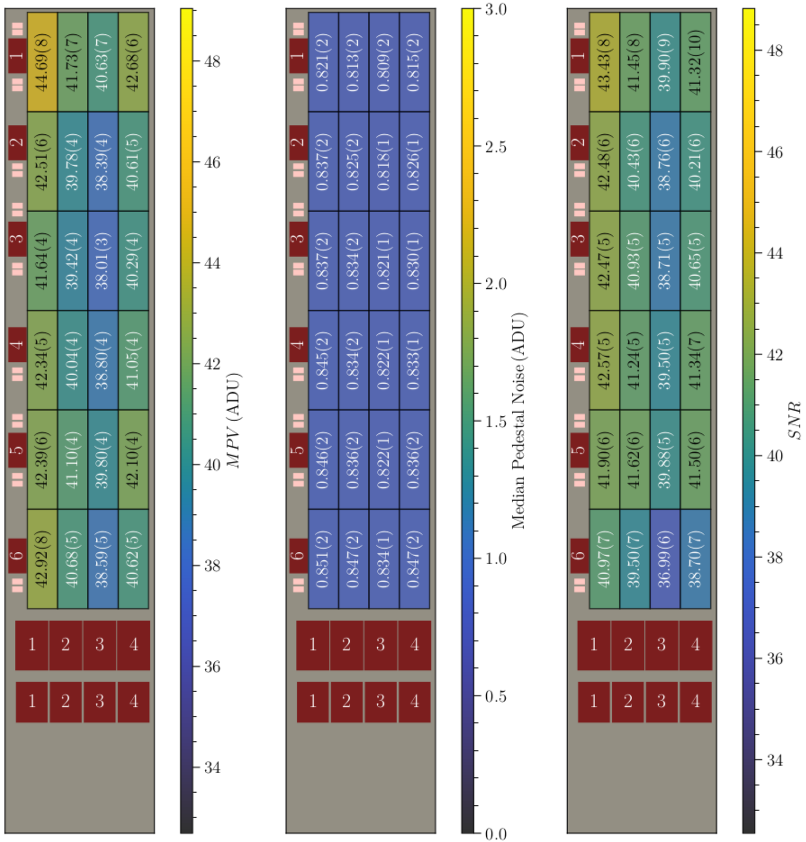


- Sr90 → MIP-like energy deposition along the sensor thickness
  - Close to what is expected in Belle II
- SNR calculated per pixel
- SNR can vary due to different system gain per module, which includes dcd gain, gm, gq



$$\mathrm{SNR}_{\mathrm{local}} = \frac{S}{\sqrt{d} \cdot n_{\mathrm{seed}}}$$

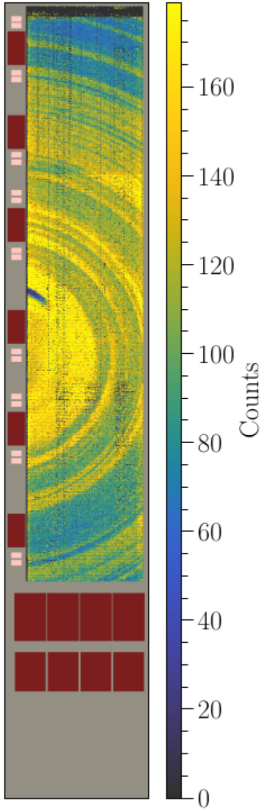
SIGNAL-TO-NOISE RATIO PER ASIC PAIR

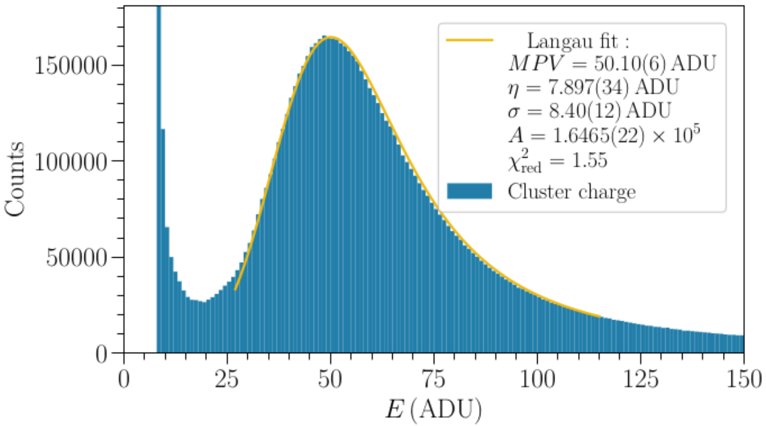


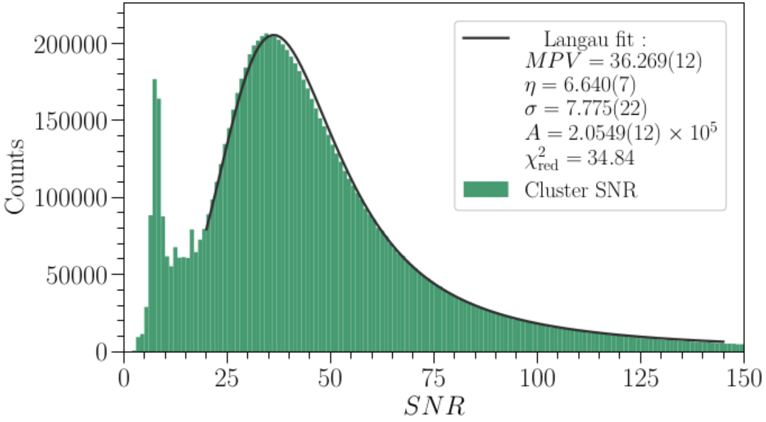
- SNR can also vary from area to area on a given module
  - Areas are controlled by different ASIC pairs
  - Different DCD gain
  - Different gm → different gq
- What happens to the cluster MPV and SNR with irradiation?

$$g_q = \frac{\partial I_D}{\partial q_i} = \frac{g_m}{C_{ox} W L}$$

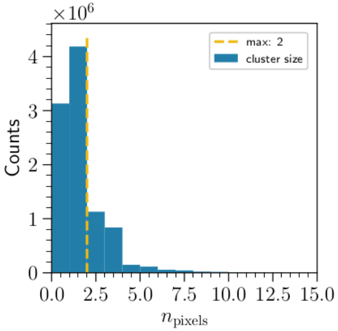
SOURCE SCAN SR90 ORIGINAL HV (-58V) IRRADIATED



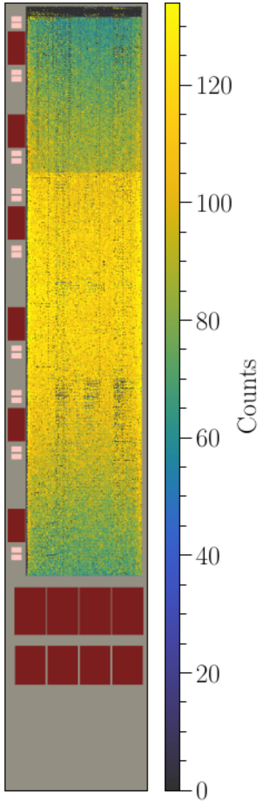


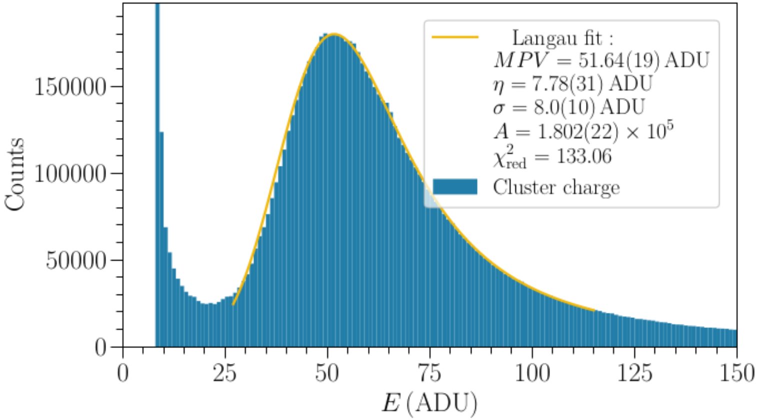


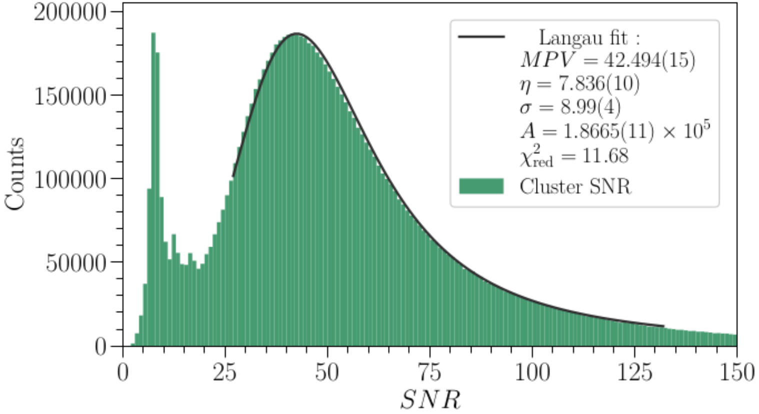
- Increased backside currents → Voltage drop through high resistivity bulk
  - HV needs adjustment
- Rings are concentric to the wafer
- Rings arise from the silicon ingot growth process
  - From center outwards
- Bulk doping variations
  - Darker areas → higher bulk doping → under-depleted
- Cluster SNR is heavily affected
  - More cluster size 2 events
  - Higher pedestal noise



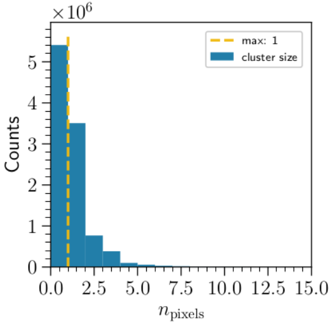
SOURCE SCAN SR90 NEW HV (-65V) IRRADIATED



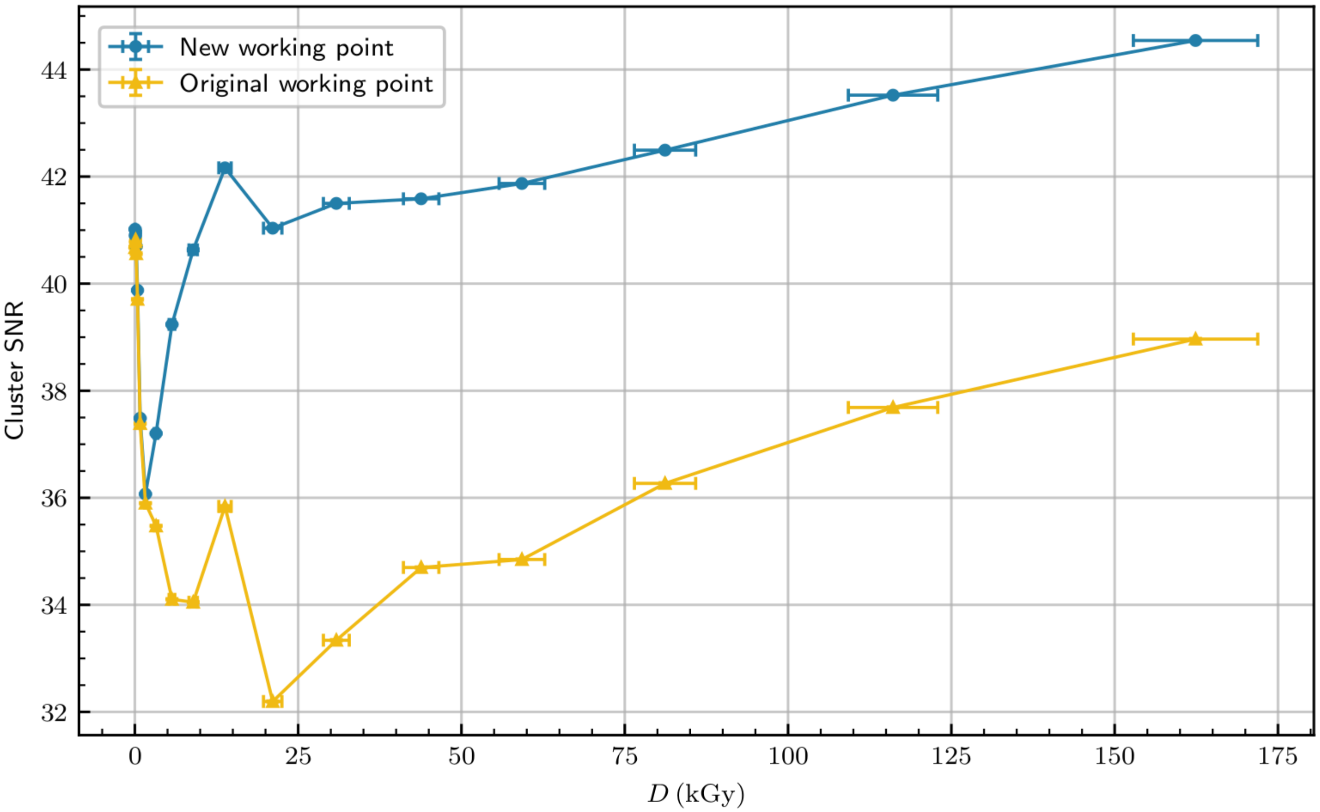




- Cluster SNR now much higher by just applying more negative HV
  - No under depleted areas
- Less cluster size 2 events as well
  - Charges drift faster to the internal gate
  - Less time for diffusion to neighbouring pixels



SIGNAL-TO-NOISE RATIO VS TID



- SNR is affected by **(20-30)%** due to high backside currents
- For TID < 10 kGy:
  - Backside currents increase
  - Higher voltage drop → lower SNR
- For TID > 10 kGy:
  - Backside currents slowly decrease
  - Lower voltage drop → SNR starts recovering
- Keep in mind:
  SNR(gm, gq, dcd gain)

SUMMARY

- Voltage threshold shifts are expected to be in a manageable range (> -13V)
  - Power supply limitations around -15 V
- System gain can be maintained at the same level during operation by adjusting the gate voltages accordingly and recalibrating the ASICs
- High backside currents heavily affect the sensor depletion voltage
  - SNR is affected by (20-30)%
- Radiation damage → f(T, RH, dD/dt, incident particle, biasing, ...)

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THANK YOU!

BACKUP

RING STRUCTURES WAFER LEVEL

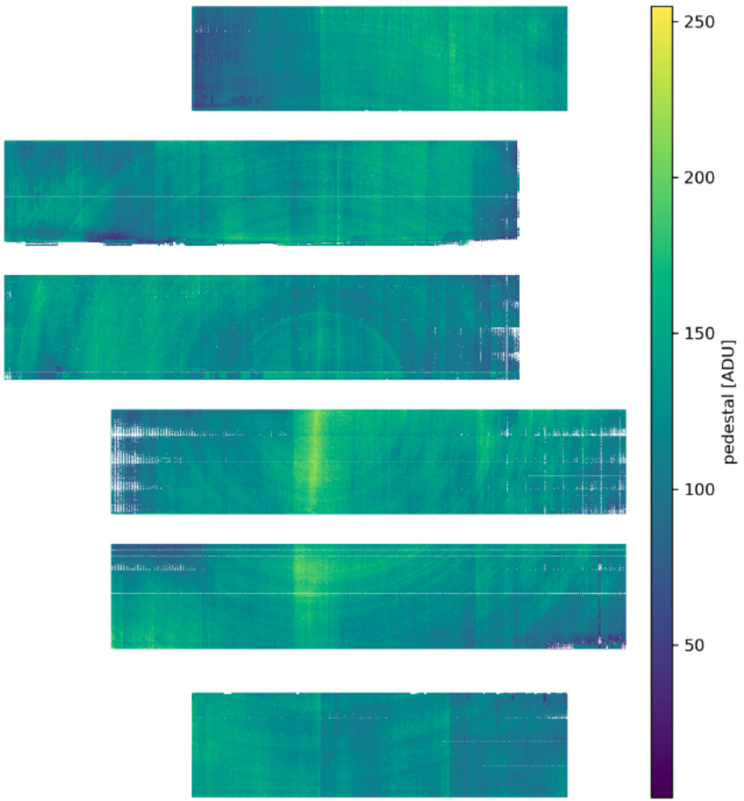
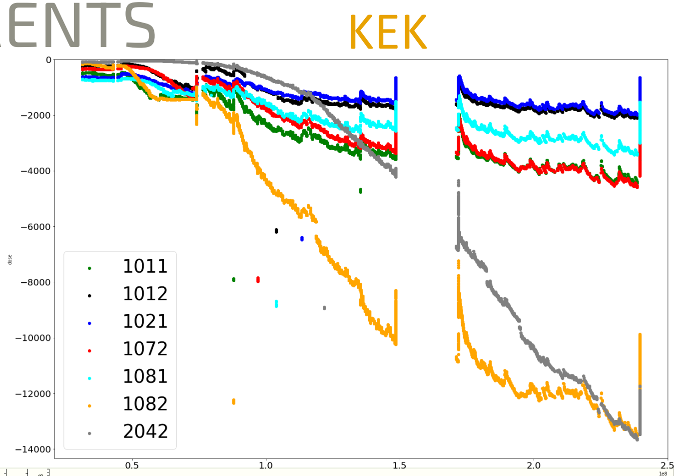
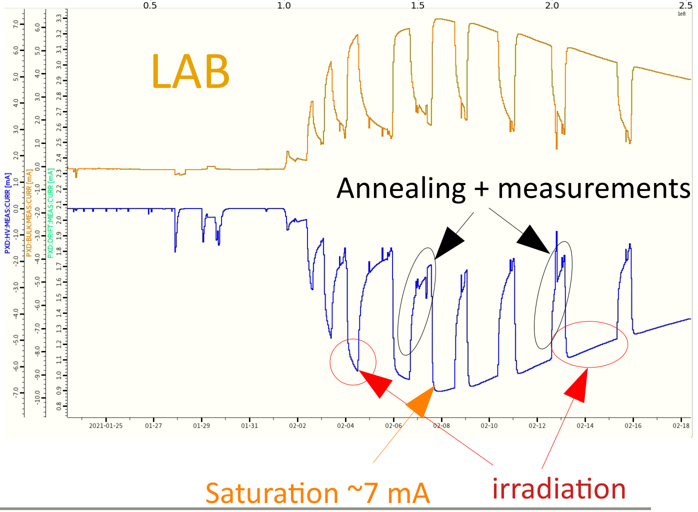


Figure 5.46: Pedestals of wafer 56 after all corrections.

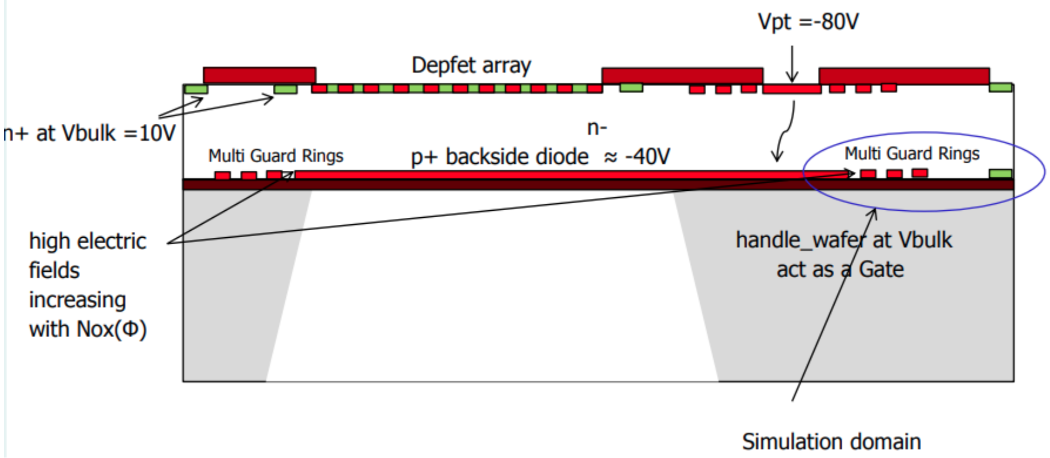
HIGH HV CURRENTS

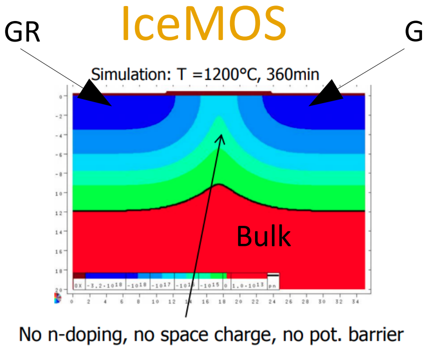


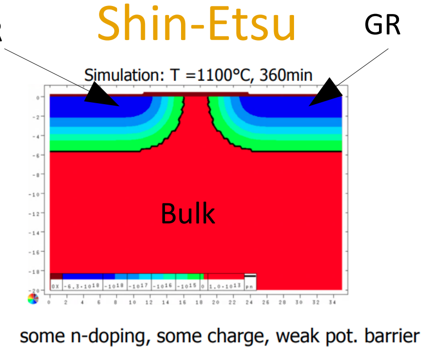


- High HV currents observed in PXD1 modules at KEK since spring 2020
- Verified by X-ray irradiation campaigns in the lab with full-scale and prototype modules
  - Saturation expected at approximately $\mathbf{D_{BOX}}$ **= 10 kGy** based on lab measurements
  - **IceMOS → saturation @ ~7 mA**
  - HV current in IceMOS is approximately **10x higher** than Shin-Etsu
- Dose of PXD1 modules **up to D = 6 kGy** , but currents went (far) beyond 7 mA
  - Radiation damage → f(T, RH, dD/dt, incident particle, biasing, ...)
- Mechanism?

HIGH HV CURRENT MECHANISM

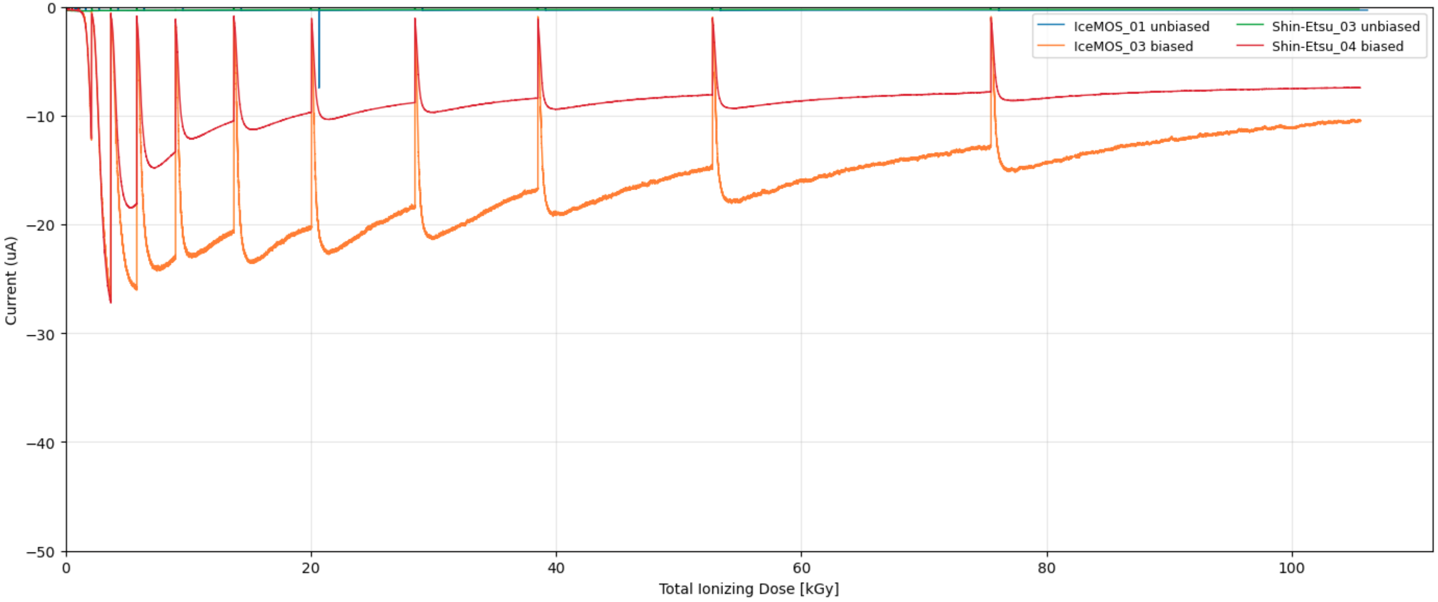






- *Secondary Ion Mass Spectroscopy (SIMS) + Simulation:* Extract dopant profile
- *Shorted guard rings*
  - The effect is worse in IceMOS than Shin-Etsu bonded wafers
- *Current understanding*: High electric fields at guard-ring structures → avalanche current multiplication → increased currents
- Structure to verify the mechanism?

BACKSIDE CURRENTS WITH TID



- IceMOS and Shin-Etsu **unbiased** during irradiation → little to no current
- IceMOS **biased** during irradiation
  - **Higher** current compared to Shin-Etsu
  - IceMOS has **shorted** guard rings → **higher** electric fields → **higher** currents