ÖAW AUSTRIAN ACADEMY OF SCIENCES

MARIETTA BLAU INSTITUTE FOR PARTICLE PHYSICS

=former “HEPHY Vienna”

The Belle II VTX Readout

presented at the
Belle II Trigger/DAQ Workshop 2025

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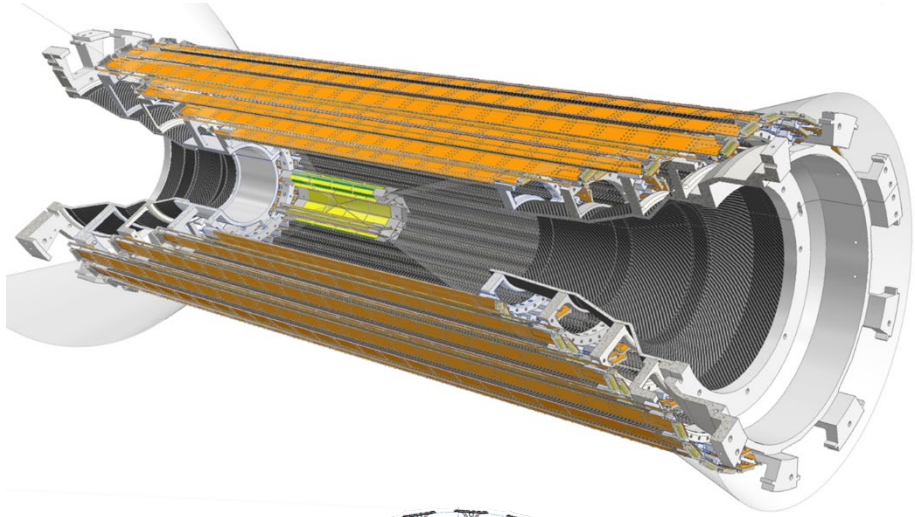
2025/10/23

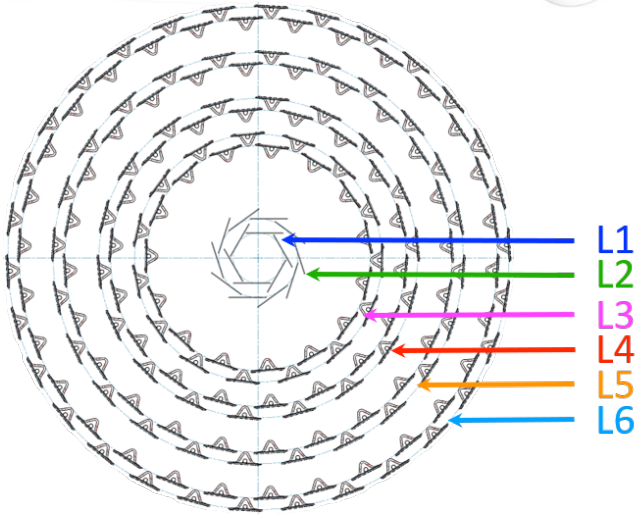
The VTX upgrade proposal

Planned for LS2 ~2032

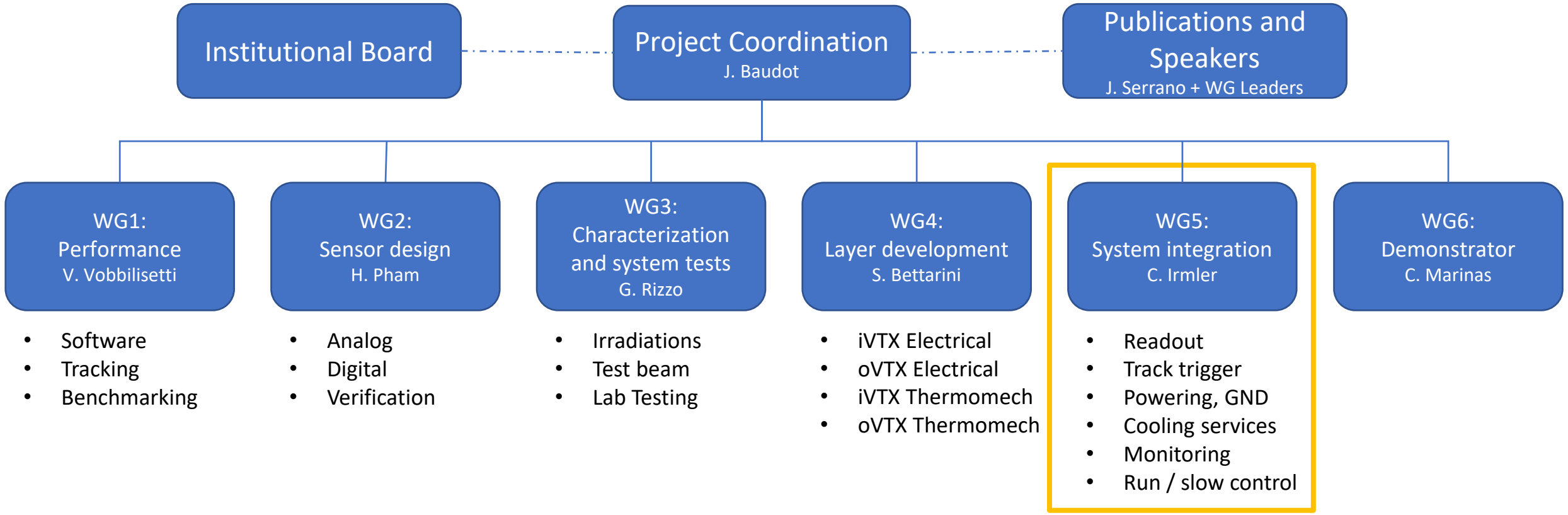
- **Baseline**: 6 straight layers using the same DMAPS sensor
- **O**ptimized **BEL**le II p**IX**el sensor (OBELIX)



- iVTX: L1, L2 → 0.3% X0
  - All silicon ladders, self-supported
  - Exploring different cooling options: air and passive cooling utilizing heat-drain material as well as liquid cooling with thin pipes
- oVTX: L3, L4, L5, L6 → 0.8% X0
  - Carbon fiber support frame
  - Cold plate with liquid cooling



VTX Organisation



MBI (Vienna)
IHEP (Beijing)
University of Jilin
CPPM (Marseille)
IJCLab (Orsay)
IPHC (Strasbourg)

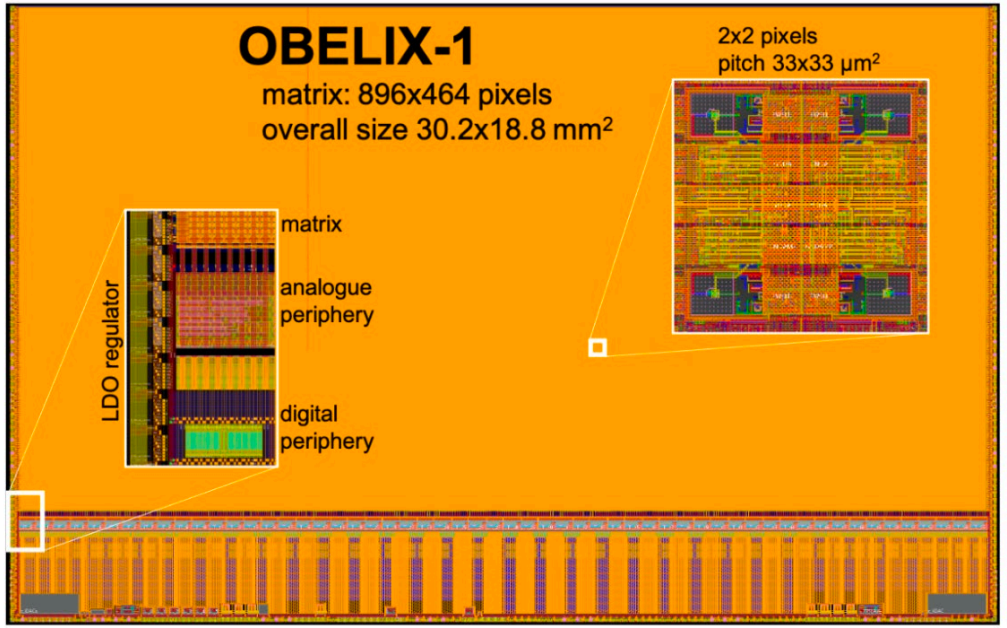
University of Bergamo
INFN Pavia
INFN & University of Pisa
University of Bonn
University of Dortmund
University of Goettingen

KEK (Tsukuba)
University of Tokyo
IPMU (Kashiwa)
IFCA (CSIC-UC, Santander)
IGFAE (Santiago de Compostella)
IFIC (CSIC-UV) (Valencia)

ITAINNOVA (Zaragoza)
Queen Mary University (London)
RAL (UK)

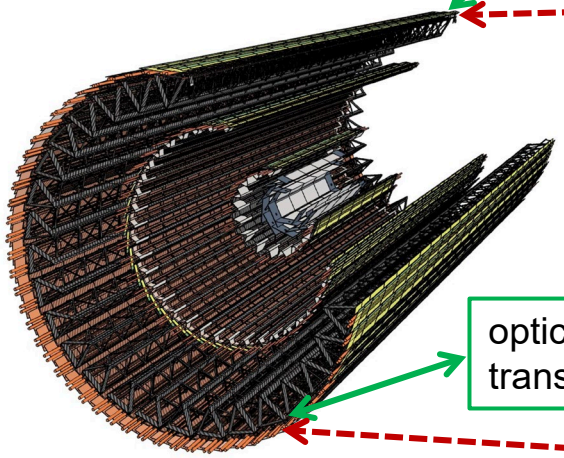
The OBELIX Chip

- Matrix inherited from TJ-Monopix2 developed for ATLAS
  - Tower 180 nm modified imaging technology
- Dimensions adjusted to VTX geometry
  - 464 rows and 896 columns,
  - 29.60×15.33 mm² active area
- Low dropout regulators (LDOs)
  - to allow input supply voltage range of 2 to 3V
- Completely revised digital periphery
  - Trigger unit with up to 10µs latency
  - Precision timing measurement
  - Low latency output for trigger contribution
- Submission planned by December 2025



- Clock frequencies:
  - Derived from SuperKEKB RF: 508.9 MHz
  - Main clock frequency 169.6 MHz
  - 2 LVDS data links operated at 339.2 MHz (169.6 MHz DDR) for hit and trigger data

VTX Readout Concept



optical transceiver

Dock Box

DC/DC converters

optical transceiver

Dock Box

DC/DC converters

optical transceiver

Back-end electronics

Belle II DAQ

Belle II trigger & clock (TTD)

L1 trigger

Run control

Slow control & config

Power supplies

power

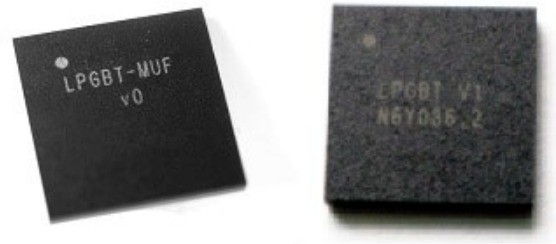
e-link: data, cfg, clock, trigger

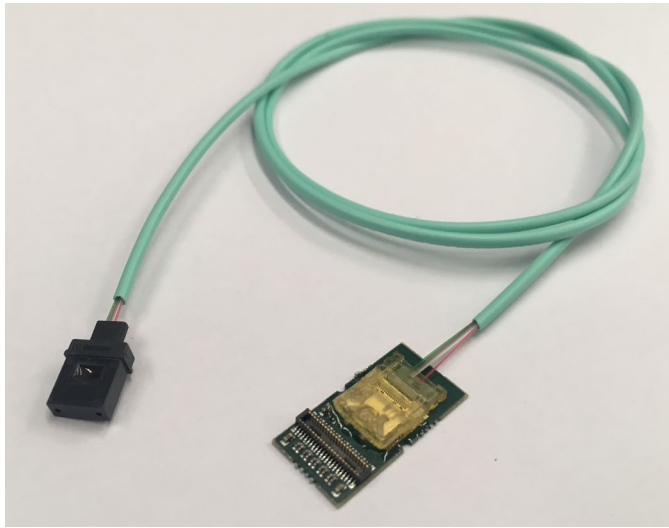
Optical transceivers placed as close to the modules as possible

radiation hard components ← → commercial components

Transceiver and optical transmitter

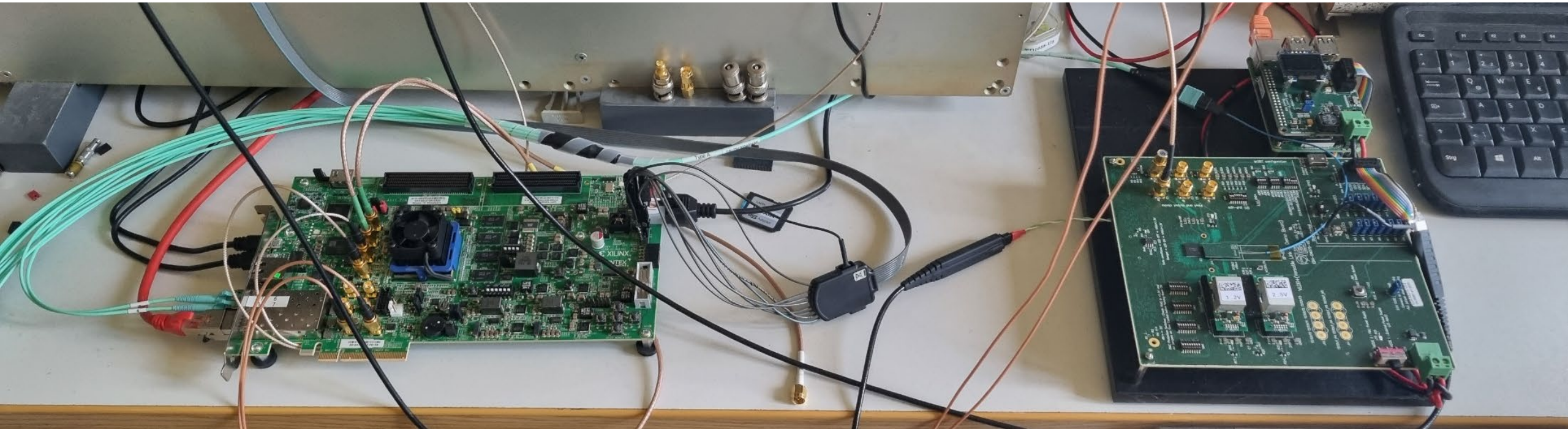
- Need fast and radiation hard transceiver and optical driver
- CERN developed a common solution for LHC upgrades
  - **lpGBT** (low power Gigabit Transceiver)
    - Collects/distributes data/clock from/to several electrical links and aggregates them on a single pair of serial high-speed data stream
    - *https://cern.ch/lpgbt*
  - **VTRx+**
    - Bi-directional optical link module
    - 1 Rx channel, 2.56 Gb/s
    - Up to 4 Tx channels, 10.24 Gb/s
    - *VTRx+ Application Note*
- Promising device, but we need to operate it out of specs
  - Specified system frequency range: 39 MHz – 41 MHz
  - For VTX we need RF/12 = 42.4 MHz





Tests at MBI Vienna

- Verification if chip can be operated with a clock frequency of 42.4 MHz
- So far ~60 chips from 8 different wafers tested in Vienna with lpGBT test kit
- Performed full loopback test with simulated OBELIX data frames



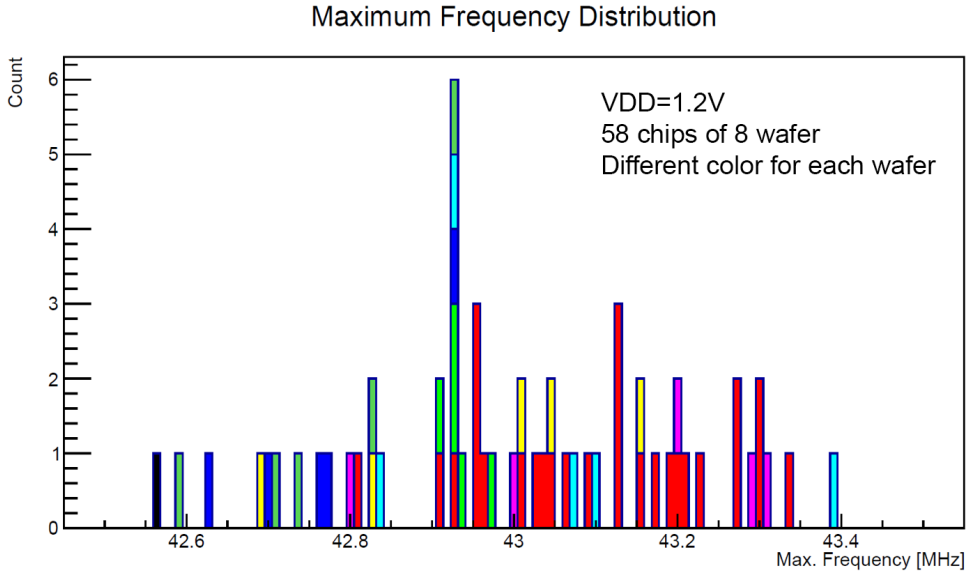
“Back-end” Optical Fiber “Front-end”

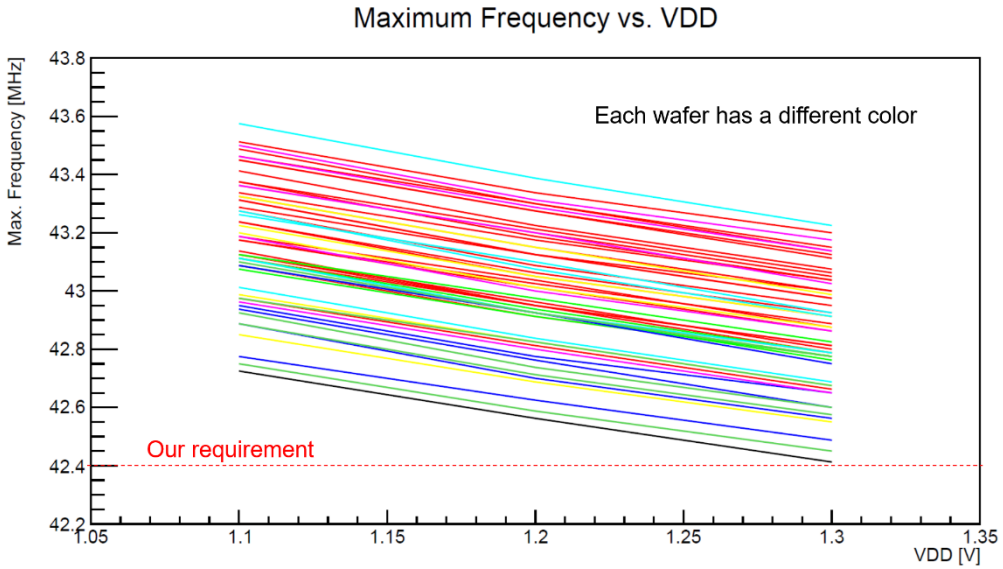
lpGBT Test results

- Tested 61 lpGBT chips from 8 different wafers.
- lpGBT operation frequency: 338MHz−350MHz
- Corresponds to a lpGBT base frequency range of 42.25MHz − 43.75MHz.
- VDD: 1.1 V, 1.2 V and 1.3 V

- Test results:
  - All chips achieved a maximum frequency of >42.55 MHz at nominal VDD, which is above the required value.
  - Three chips did not work properly at 1.1 V and/or 1.3 V, resulting in bit errors.
  - Maximum frequency improves with decreasing VDD

- So far only non-irradiated samples tested



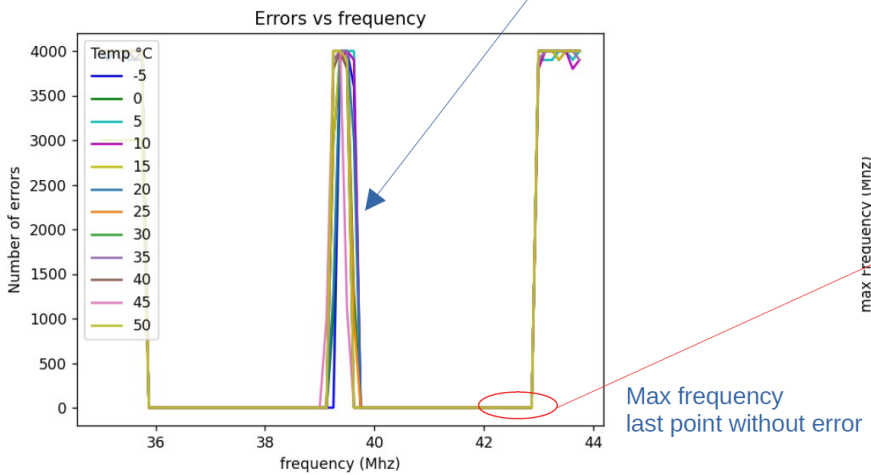


Temperature Tests at CPPM (Marseille)

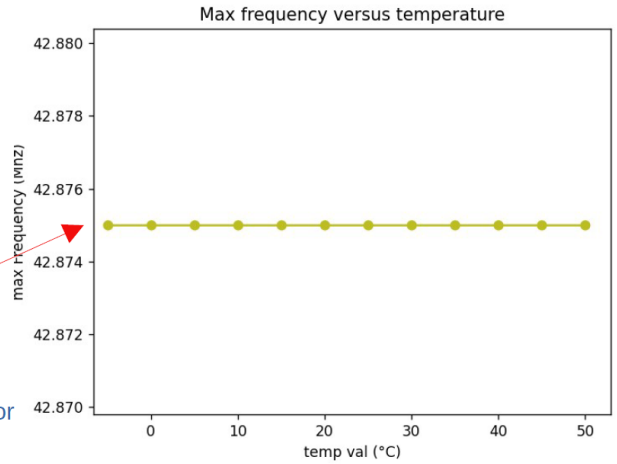
Patrick Breugnon (CPPM)
20 August 2025

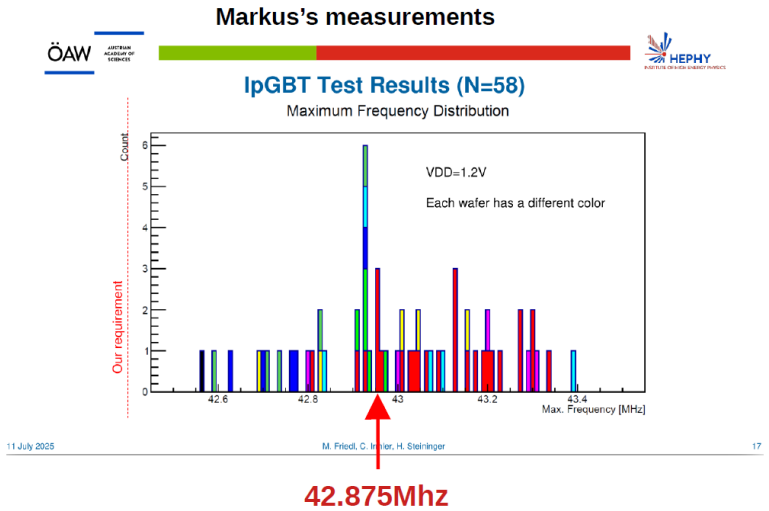
Generator from 280 to 350Mhz
Ref Clk from 35 to 44 Mhz

Phase not adjusted



Max frequency
last point without error





42.875Mhz

We want to operate at
RF / 12 = 508.887 MHz / 12 => RefClk = **42.40725 MHz**

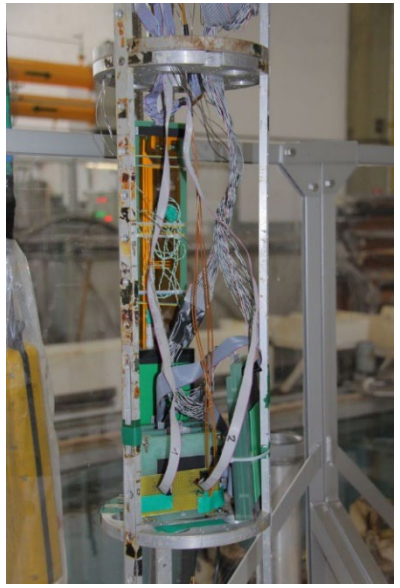
Max frequency of lpGBT, CPPM chip **42.875 Mhz**

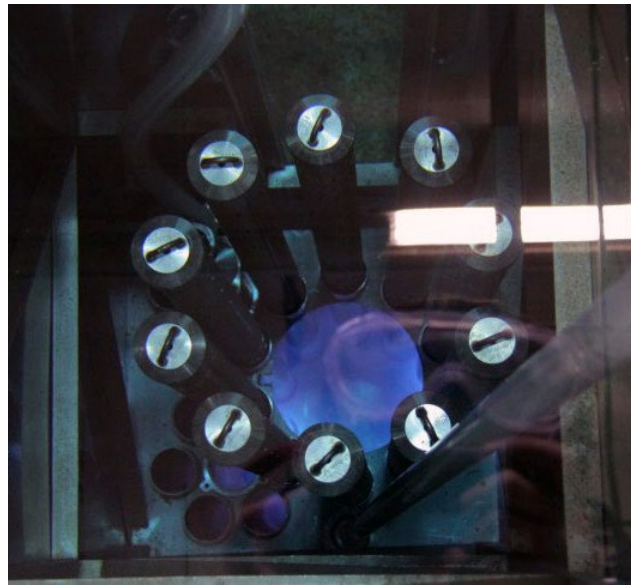
Temperature has no influence on the max frequency

We have at CPPM an operational lpGBT test setup

Irradiation @ SCK-CEN (Mol, Belgium)

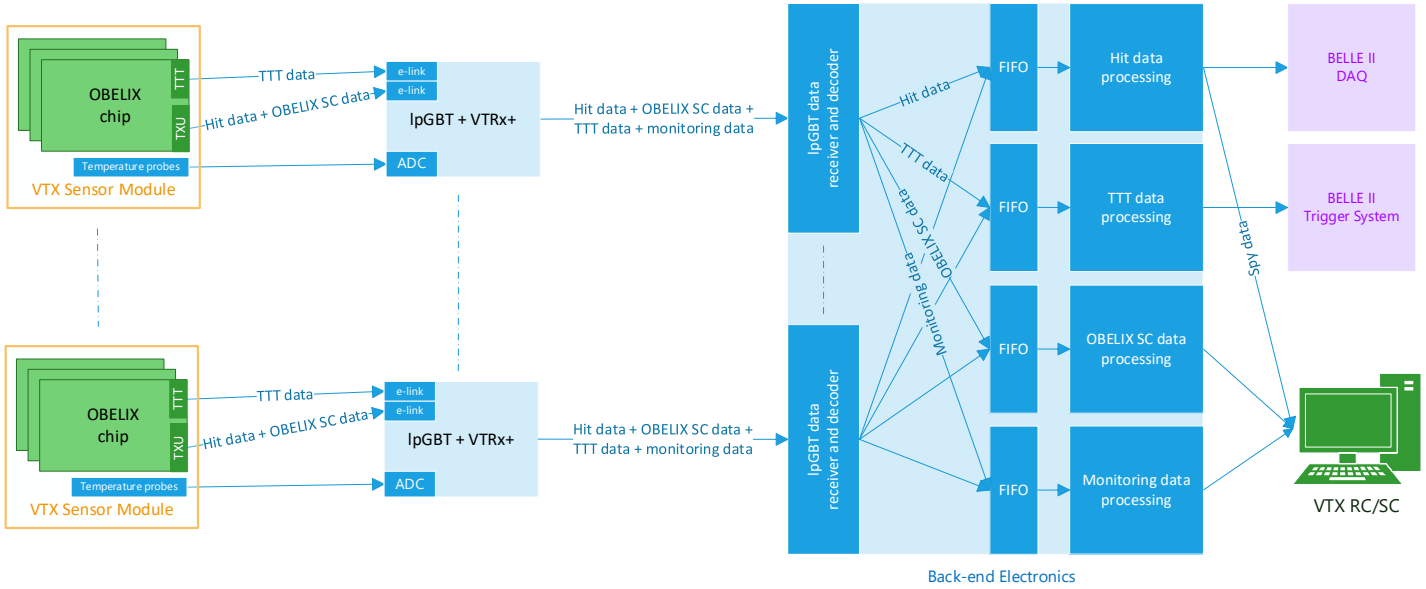
- Irradiation under bias; we aim for (up to) 100 Mrad
- Underwater Cobalt-60 source:
  - BRIGITTE with ~600 krad/h (1 week to 100 Mrad) – still under commissioning, more info soon
  - Irradiation planned for early 2026





Back-End Electronics - lpGBT data uplink

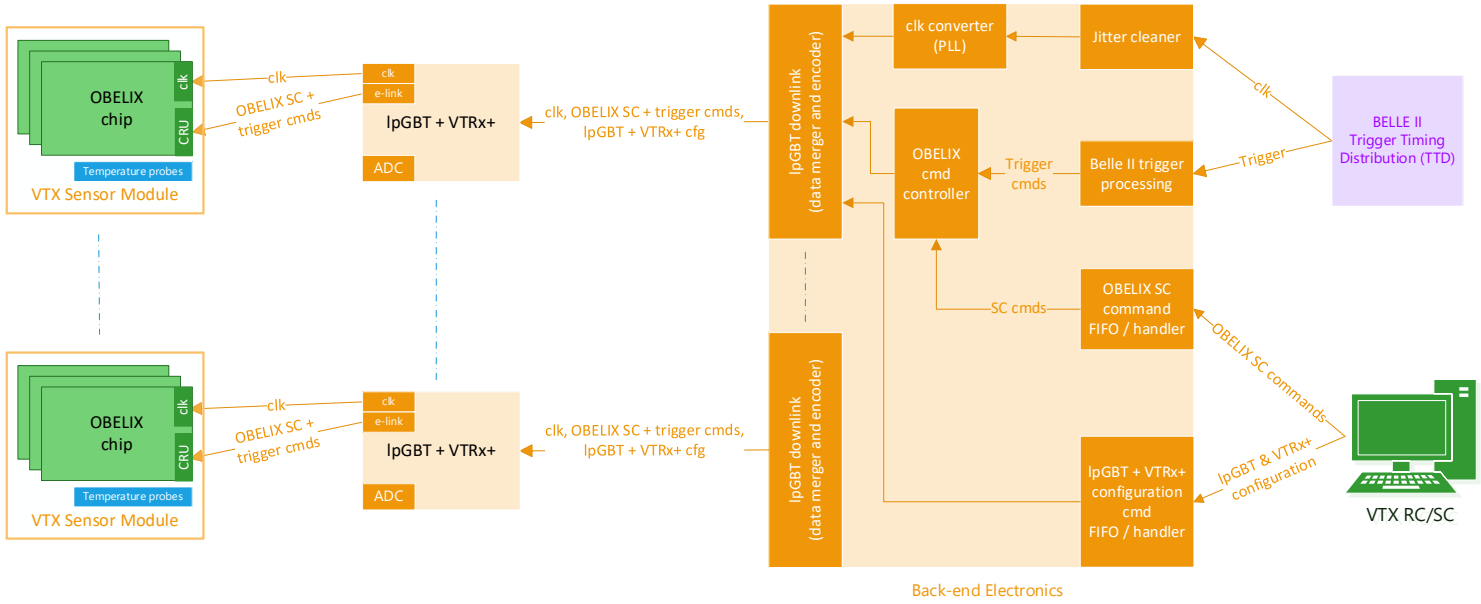
- lpGBT data frame contains 4 types of data:
  - **Hit data**: particle hits = physics data
  - **Trigger data from TTT**: input for L1 trigger, need low latency readout
  - **OBELIX register values**: read on demand and sent via hit data path
  - **Monitoring data** from lpGBT ADCs, e.g. temperature probes, voltages, etc.
- Back-end data handling
  - Unpack, decode and split lpGBT data into individual data streams
  - Discard OBELIX IDLE patterns
  - Forward data streams to
    - DAQ: hit data
    - Trigger system: TTT data with low latency
    - Slow control SW: monitoring data



OBELIX SC data = OBELIX slow control data: configuration read-back, temperature values, voltages, etc.

Back-End Electronics - lpGBT data downlink

- Data from several sources to be sent to lpGBT via optical downlink
  - From Belle II TTD
    - Clock
    - Trigger
  - From VTX run and slow control
    - OBELIX slow control commands:
      - Configuration
      - Reset and local run commands
      - Register read-back
    - lpGBT and VTRx+ configuration
  - Belle trigger need to be converted into OBELIX trigger commands (RD53 style)



OBELIX SC commands = OBELIX configuration, reset and local run commands, etc.

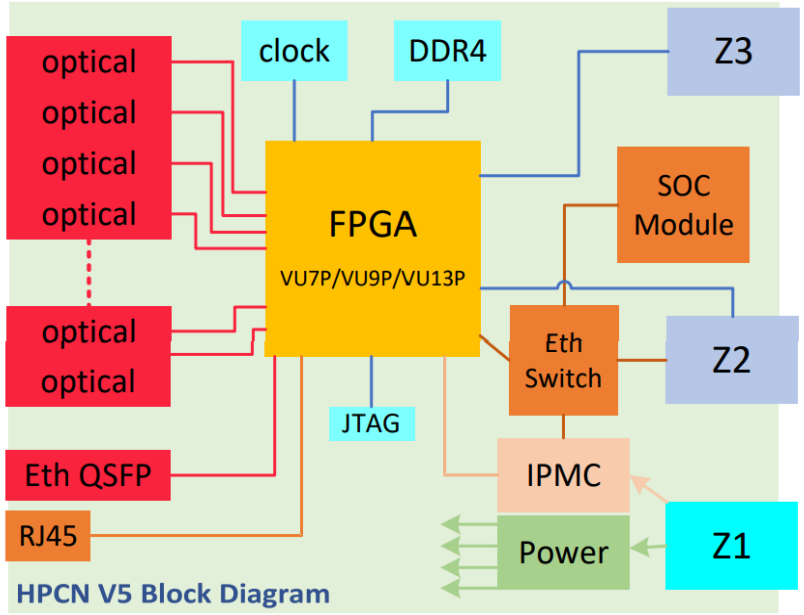
Back-End Electronics HW

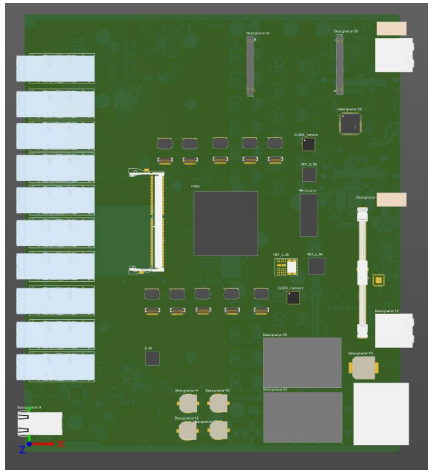
- Will be placed in e-hut → does not need to be radiation hard
- FPGA based system with sufficient amount of optical links
  - Current 6 layer VTX design requires up to 334 bi-directional optical links
  - Uplink: 10.2 Gb/s, downlink: 2.5 gb/s
- In the process of identifying appropriate boards and systems
  - Future-proof choice of FPGA: mid- and long-term availability, adequate performance, sufficient contingency, reasonable price
  - **PCIe40**: currently used in Belle II, uses Intel Aria 10, released 2013, need to verify if it fulfils our requirement regarding performance, moreover the FPGA might be outdated when VTX is installed
  - **PCIe400** under development: Intel Agilex 7, first boards expected 2026/2027, to be checked if we can use them for VTX
  - **CEPC TDAQ board** currently under development by IHEP China: based on ATCA, but ATCA might fade out soon…

TDAQ Board for CEPC: Details

(proposed by Jingzhou Zhao, IHEP China)

- Common Trigger board function list
  - ATCA standard
  - **Virtex Ultrascale Plus FPGA** (VU9P,VU13P pin compatible)
  - 44 channels for optical, 11 QSFP+
    - Optical channel: 10-25 Gbps/ch
    - 40 channels for links to FEE and Trigger
    - 4 channels for DAQ readout
    - Optical Ethernet or RDMA : 40-100GbE
    - RDMA IP core is under developing
  - DDR4 for mass data buffering:16GB
  - Front 1 GbE and Z2 GbE fabric port for parameter configuration and control
  - SoC module for board management
  - IPMC module for Power management
- Progress
  - Preliminary finished schematics, PCB layout is next step
  - First version is expected mid-2026

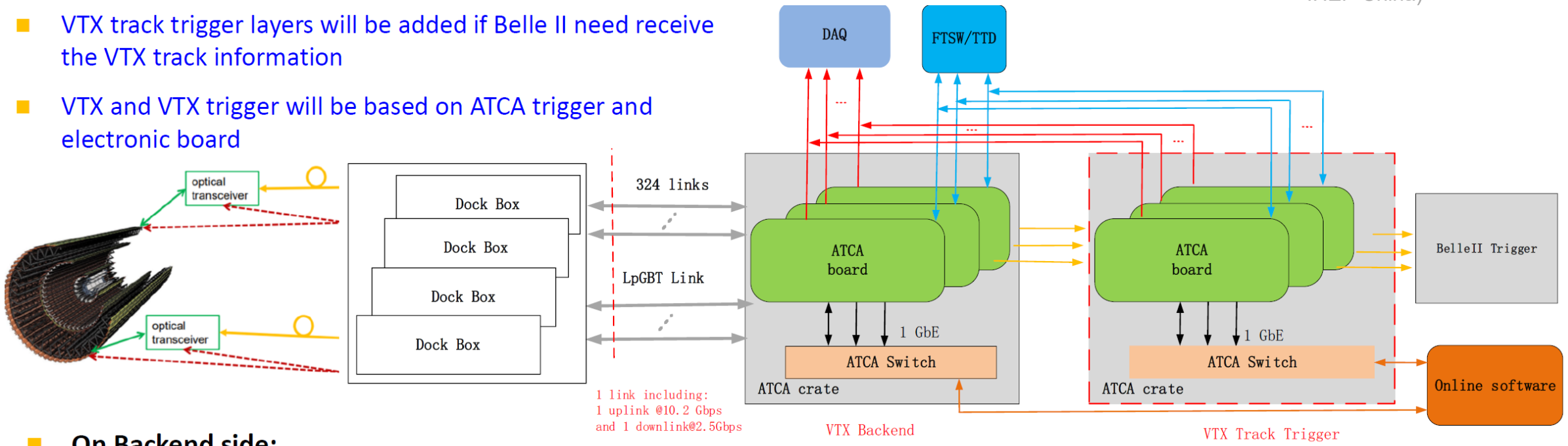




IHEP Proposal for VTX Backend (1)

(proposed by Jingzhou Zhao, IHEP China)

- VTX track trigger layers will be added if Belle II need receive the VTX track information
- VTX and VTX trigger will be based on ATCA trigger and electronic board



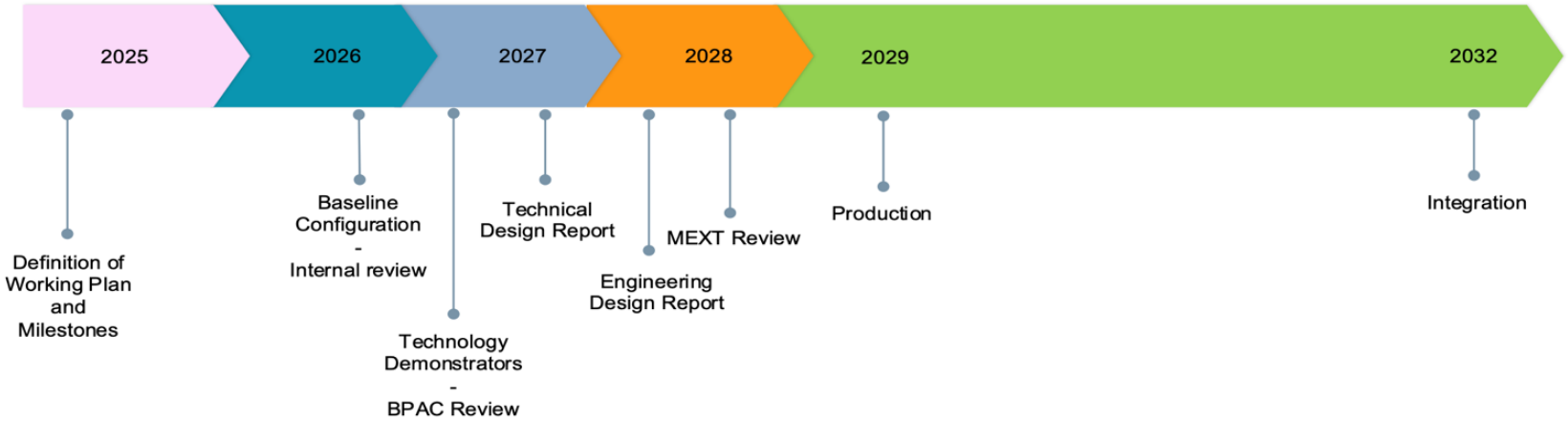
- **On Backend side:**
  - Receive and decode TTC signals from FTSW and feedback BUSY and Error signal to FTSW
  - Separate the hit data and trigger data;
  - Generate the cluster Trigger Primitive(TP)
  - Send TP data to VTX tracker in pipeline way
  - Package the hit data and TP data based on L1
  - Send data package to DAQ via TPC/RDMA
  - ATCA Switch board as a 1GbE Ethernet switch for Online connection with ATCA board for Slow control

- **On Track trigger side:**
  - Receive and decode TTC signals from FTSW and feedback BUSY and Error signal to FTSW
  - Receive Cluster TP data and do track finding in section;
  - Send track data to Belle II trigger based on BelleII trigger transmission Protocol
  - Package the TP data and Track data based on L1
  - Send data package to DAQ via TPC/RDMA
  - ATCA Switch board as a 1GbE Ethernet switch for Online connection with ATCA board for Slow control

IHEP Proposal for VTX Backend (2)

- Scale estimation:
  - Back-end: One ATCA board deals with 36 lpGBT links → 9 boards needed
  - VTX Track Finding: one ATCA board deals with 60 degrees or 120 degrees → 6 or 12 boards needed
- More information needed for further discussion
  - What does Belle-II trigger need from VTX?
  - What is the maximum latency allowed for VTX backend?
  - Data transmission protocol with Belle-II trigger?
- Need to verify and ensure long-term availability of ATCA platform

Roadmap Towards L2 (2032)



- Milestones
  - Technology decision 2026
  - TDR mid-2027
  - Prototype system for demonstrator and module testing ~2029
  - Production of final system 2030+

Outlook

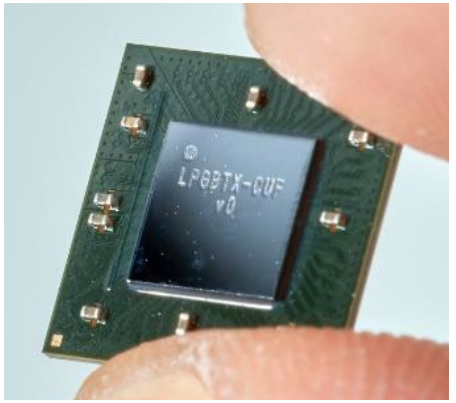
- Will continue evaluation of lpGBT
- Continue the search for possible HW solutions for the back-end electronics.
  - The proposal from IHEP is promising, but we are **open for suggestions**, especially from Belle II (T)DAQ groups, and new collaborators.
- Have to intensify discussion on
  - Powering (power supplies, DC/DC converters, etc.)
    - Currently preparing requirements
  - Monitoring (temperatures, humidity, etc.)
  - Run and slow control software: so far not started, which framework, etc.
- Have monthly WG5 meetings
  - Next meeting Nov. 30th partially combined with WG4
- New collaborators are always welcome

Summary

- The Belle II Upgrade proposal includes the replacement of the innermost detector by a fully pixelated vertex detector (VTX) made of DMAPS
- Evaluation lpGBT and VTRx+ for optical link ongoing
  - So far very promising results
  - Will conduct an irradiation campaign in early 2026
- Currently identifying appropriate platform for back-end electronics

BACKUP

Overview lpGBT



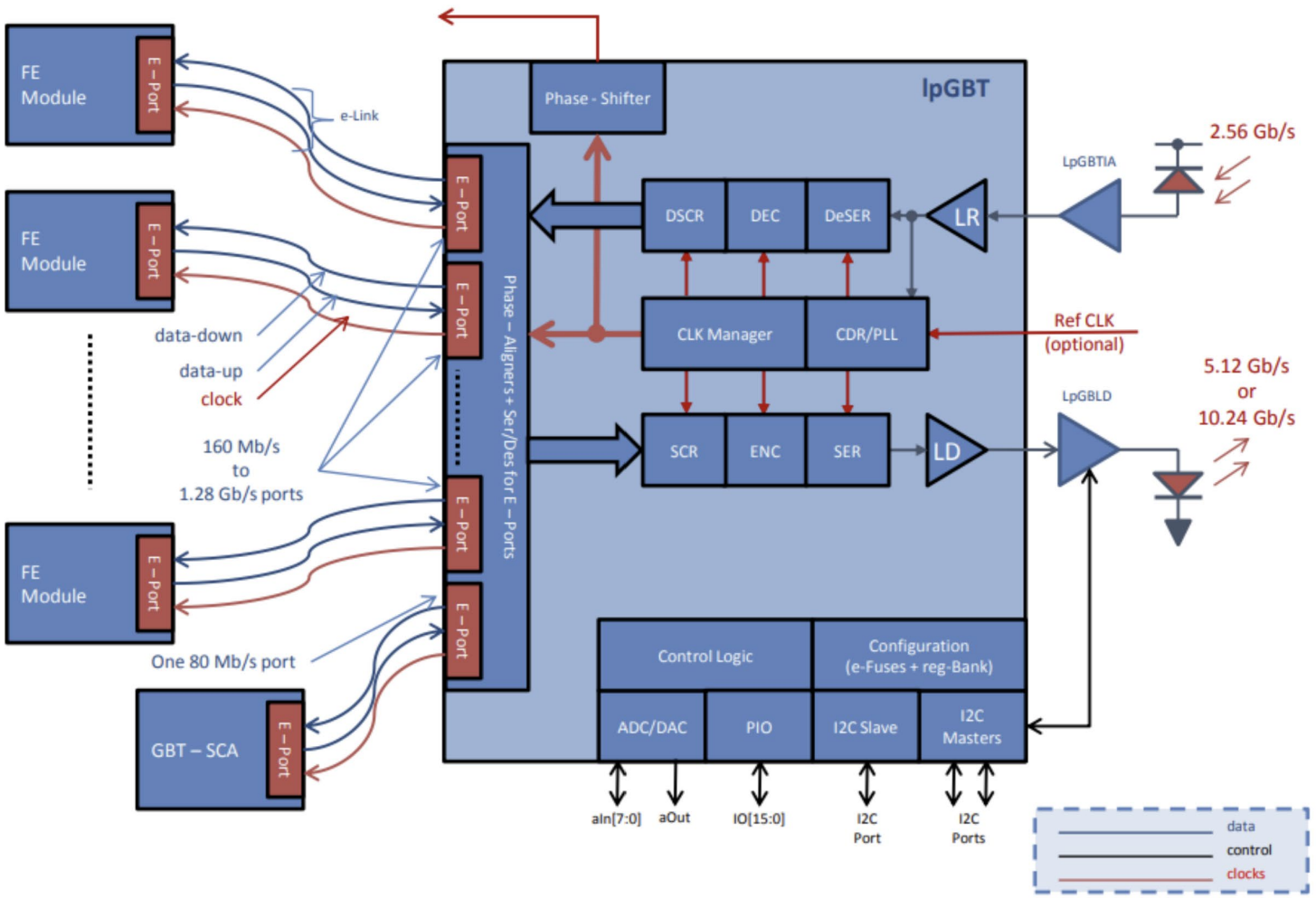
Low power Giga Bit Transeiver chip

- Uplink:
  - 5.12 Gbps: 128b@40MHz
  - 10.24 Gbps: 256b@40MHz
- Downlink: 2.56 Gbps: 64b@40MHz
- Up to 28 e-links
- Further features
  - 4 programmable clocks with 50 ps resolution
  - 3 x I2C masters
  - 16-bit GPIO, 10-bit ADC, 8-bit DACs
  - Programmable current sources for PT100/1000

- Design specifications
  - 65 nm CMOS technology
  - ~200 Mrad TID / SEU robust
  - 0.75W @ 10.24Gbps / 0.5W @ 5.12Gbps
- Link qualitymonitoring
  - Eye Opening Monitor
  - Bit Error Monitoring
- Small Footprint:
  - 9 mm x 9 mm with 0.5 mm pitch

General architecture of the lpGBT ASIC

Front-End



Back-End

LpGBTdata transmission

Uplink		e-link	
Speed	**Encoding**	**Bandwitdh [Mbps]**	**#**
5.12 Gbps	FEC5	160	28
		320	14
		640	7
	FEC12	160	24
		320	12
		640	6
10.24 Gbps	FEC5	320	28
		640	14
		1280	7
	FEC12	320	24
		640	12
		1280	6

- Different configuration possible
- Number of available e-links depends on BW of e-link as well as speed and mode of uplink.

Downplink		e-link	
Speed	**Encoding**	**Bandwitdh [Mbps]**	**#**
2.56 Gbps	FEC12	80	16
		160	8
		320	4