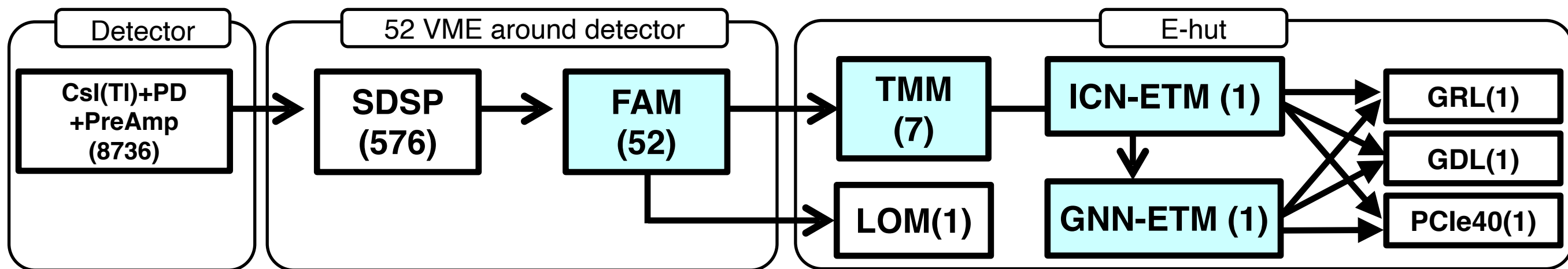


Status on ECL trigger

2025/10/22-24
TRG/DAQ workshop
Y.Unno

ECL trigger system



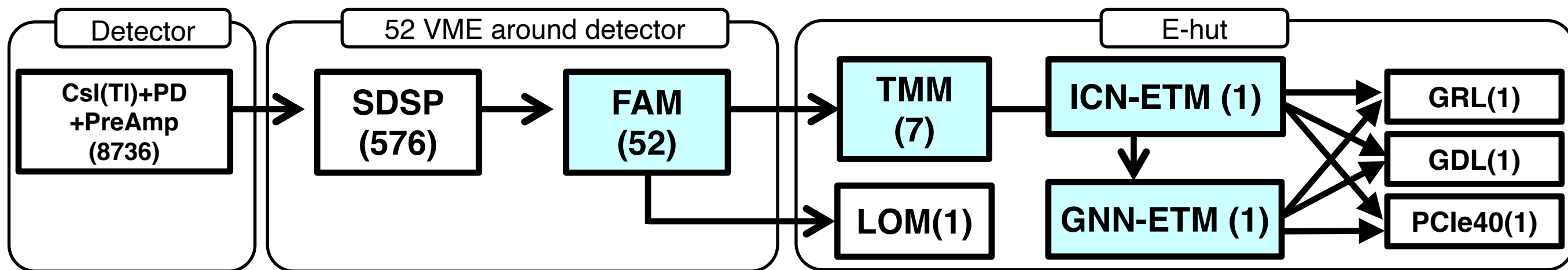
• FAM

- Receive 576 trigger cell(TC) analog data from ShaperDSP
 - 1TC consists of $4 \times 4 = 16$ crystal
- Digitization with FADC
- TC E&T rec. by WF analysis(χ^2 fit) with 8MHz on Kintex7
 - 100MeV energy threshold applied to each TC.
- Send 576 TC E&T to ETM through TMM by opt link with pipeline
- Send analog TC data of endcap to LOM(online luminosity monitor)

• TMM

- Play an role of merger on Kintex7

ECL trigger system

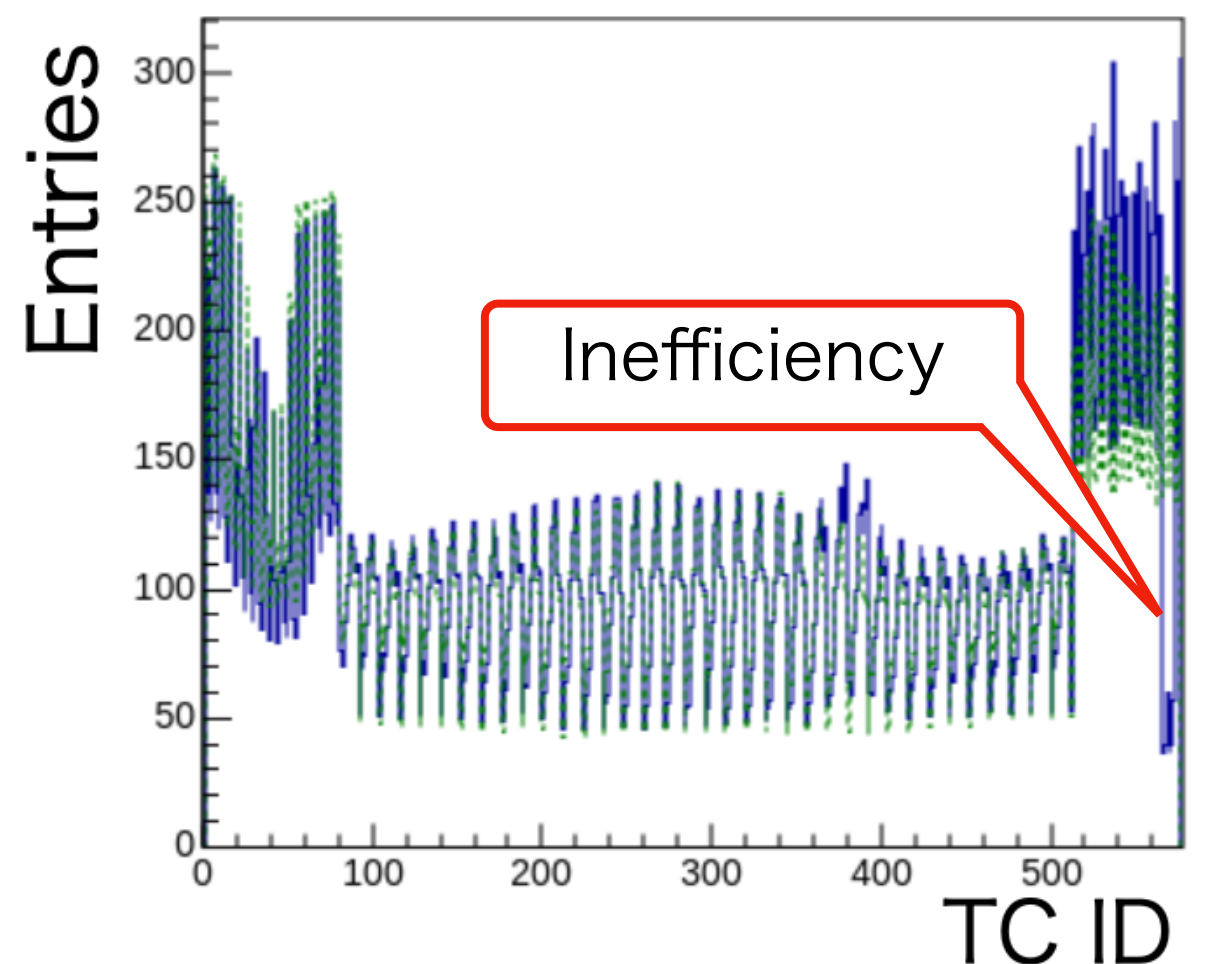
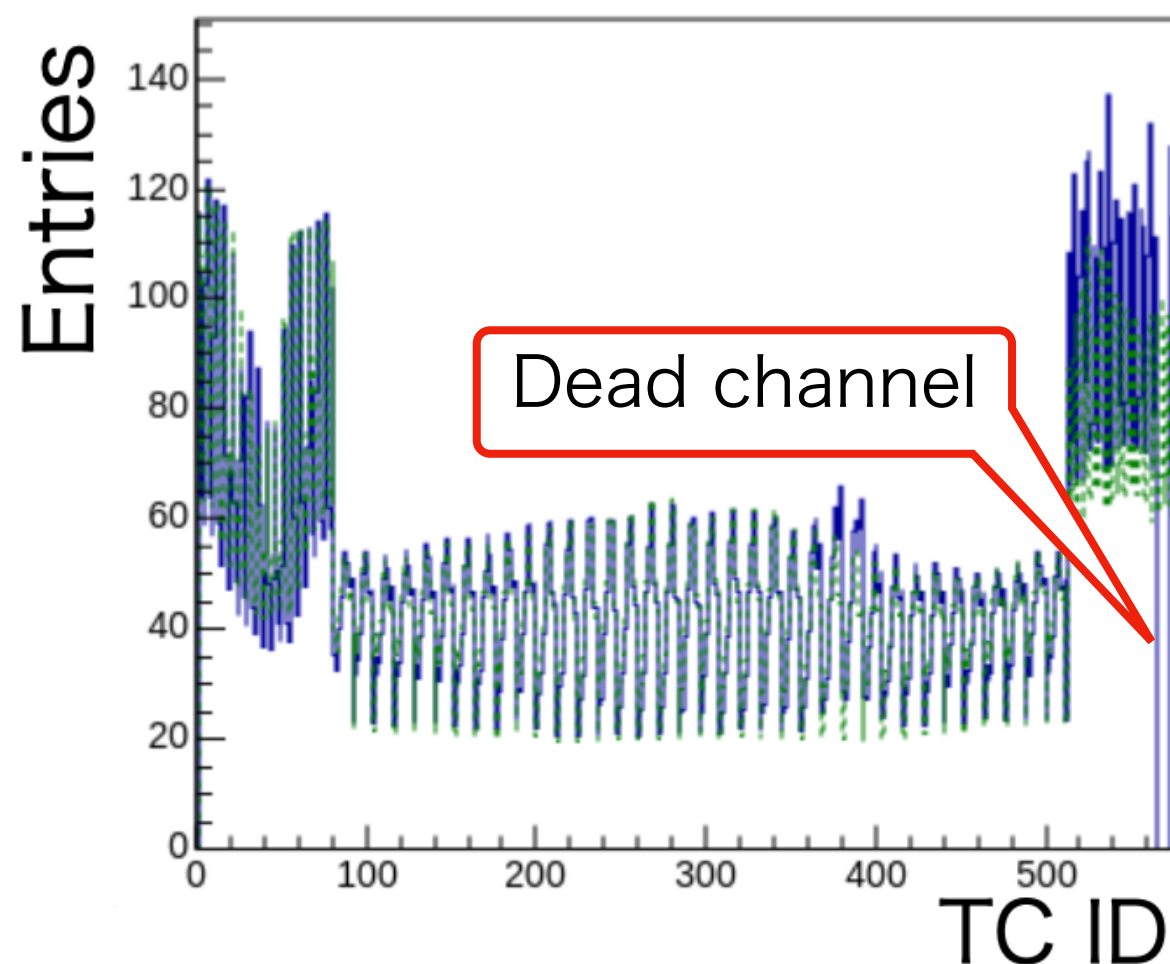


• ICN-ETM (UT4)

- ECL trigger summary by all TC E&T on VirtexUltrascale
 - Total energy sum and ICN(# of isolated cluster)
 - Clustering => 3D Bhabha veto, several low multi physics bits
 - Event timing based on timing of most energetic TC
- Send ECL trigger summary to GDL
- Send cluster data to GRL for track-cluster matching on GRL
- Send fired TC E&T and trigger summary to PCle40
- Send N(TC hit) to GDL for injection veto
- Real time bkg monitor : provide PV of N(TC hit) w/ and w/o local inj veto
- Provide PV of instantaneous luminosity based on 3DBhabha veto

Link instability of TMM to ICN-ETM

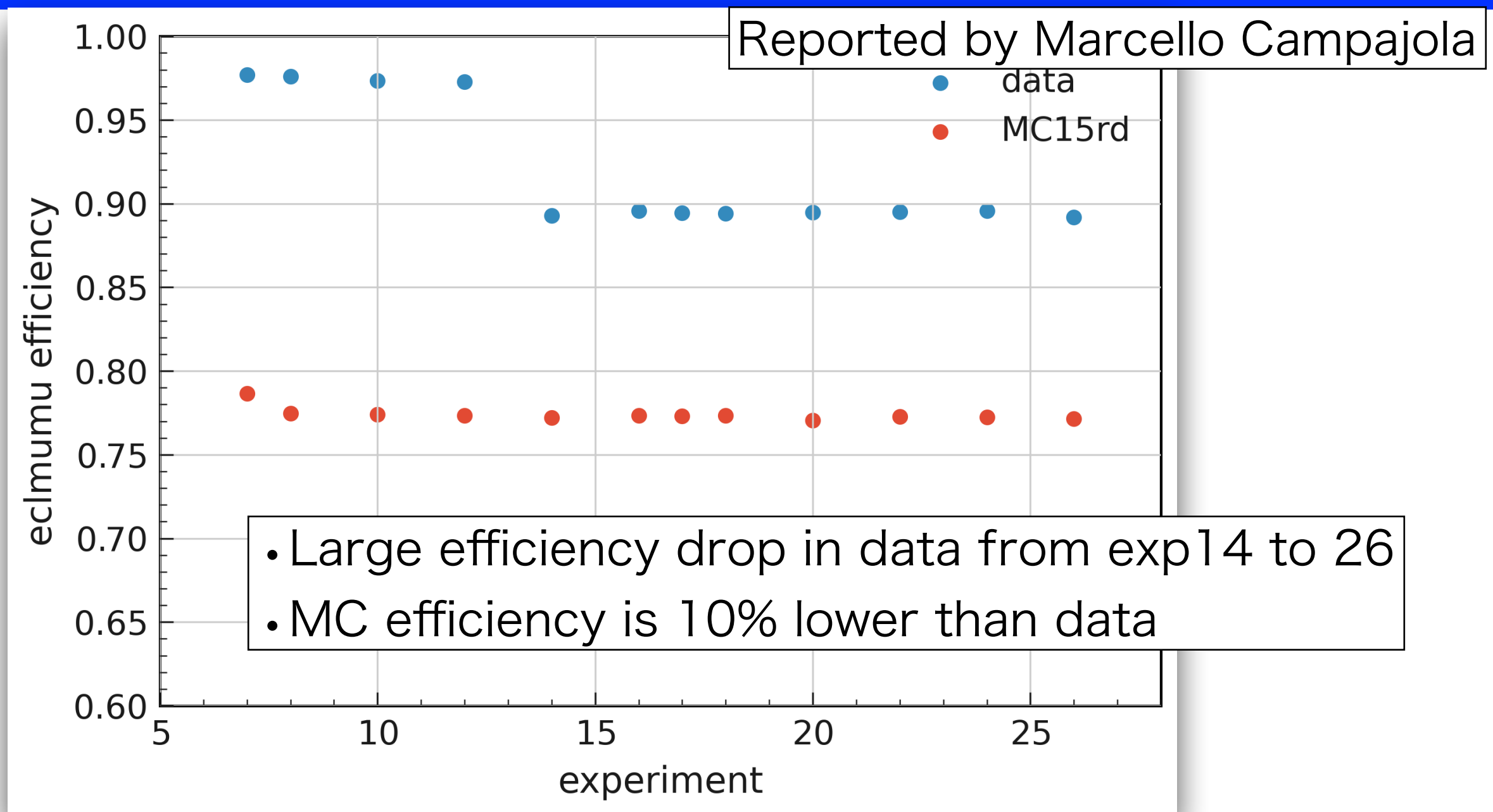
- link of TMM to ICN-ETM was stable when UT3 was used as ICN-ETM
 - 26 GTH lanes for 7TMMs to ICN-ETM
- After replaced UT3 with UT4, it became unstable just after reboot
 - (A) link is not correctly established
 - (B) repeat up and down with mild frequency
- Caused BAD runs (dead or inefficiency channels)



Link instability of TMM to ICN-ETM

- For dead channel detection
 - Logic to detect dead channel from DQM (Jing Yuan + T.Koga)
 - Logic to detect dead channel in SLC and stop global run
- For inefficiency channel detection
 - Found incomplete data alignment logic on ICN-ETM and fixed
 - Found incomplete logic to check link status on ICN-ETM FW
 - Updated ICN-ETM FW to detect unhealthy link
 - Modified SLC to stop run when unhealthy link is detected
- The reason why link is unstable after reboot is not identified yet.
 - Will tackle to identify the reason

Problem in eclmumu bit



- eclmumu bit, generated by ICN-ETM and prescale=1 at GDL

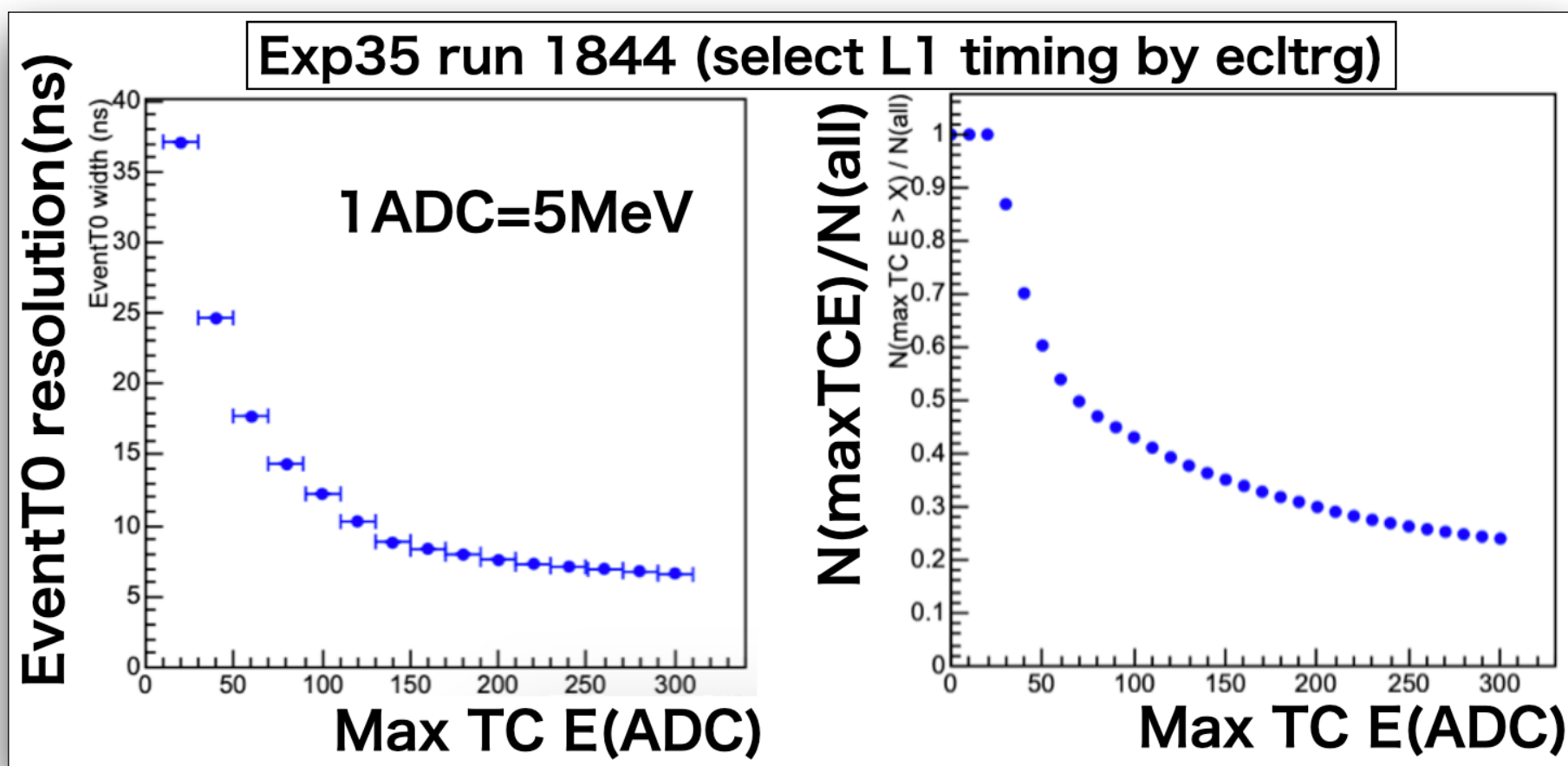
- $165^\circ < \Sigma\theta_{\text{CM}} < 190^\circ$, where $\Sigma\theta_{\text{CM}}$ is sum of polar angles of 2 clusters in CM
- $160^\circ < \Delta\phi_{\text{CM}} < 200^\circ$, where $\Delta\phi_{\text{CM}}$ is difference of phi angles of 2 clusters in CM
- $E(\text{CL1}) < 2 \text{ GeV} \ \&\& \ E(\text{CL2}) < 2 \text{ GeV}$
 - where $E(\text{CLX})$ is energy of cluster number X ($X=1,2$) in CM

Problem in eclmumu bit

- MC (tsim)
 - With help from Kang Chen and Yubo Li, the reason was identified.
 - Bug cause low efficiency in MC was fixed.
 - New conditionDB and tsim update for release10 were done.
- Data (ICN-ETM firmware),
 - Wrong parameter in ICN-ETM firmware was used in exp 12-26
 - The reason is not understood.
 - Updated SLC to compare parameters on FW and DB
 - If inconsistency is detected, SCL send error to stop global run.
- Countermeasures for MC and FW were done.

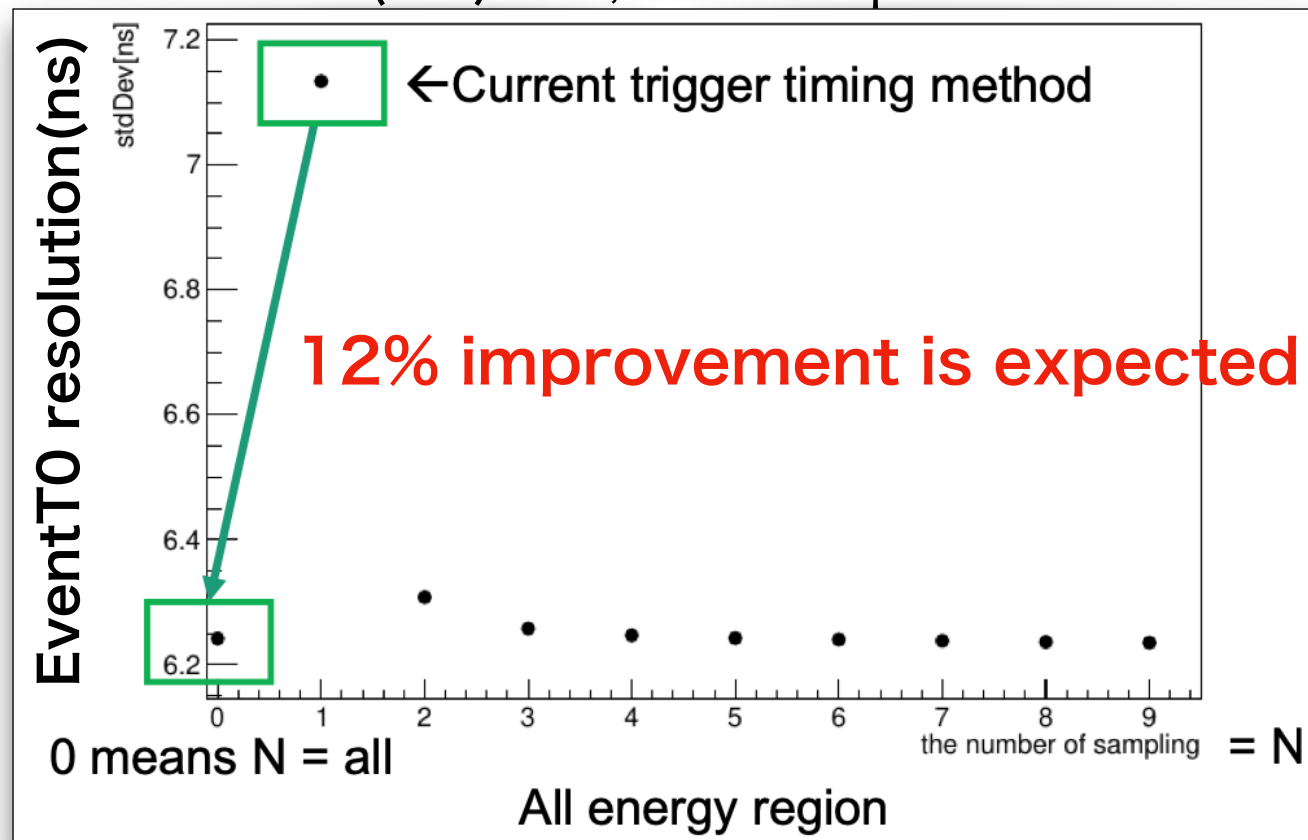
Event timing

- Currently L1 event timing is 90% based on ECL trigger
- ECL trigger event timing is determined by timing of most energetic TC in 256ns.
- SVD requires "good" resolution of L1 timing for 3 and 6 sampling mixed DAQ to reduce dead time in the future operation.
 - If the resolution is $< 10\text{ns}$ (?), apply 3 sampling, if not, 6 sampling
 - Larger fraction of event with $< 10\text{ns}$ is required (40%?)
- ECL trigger sends (course, fine, super-fine) flag to SVD.
- Event timing DQM is ready for performance check.



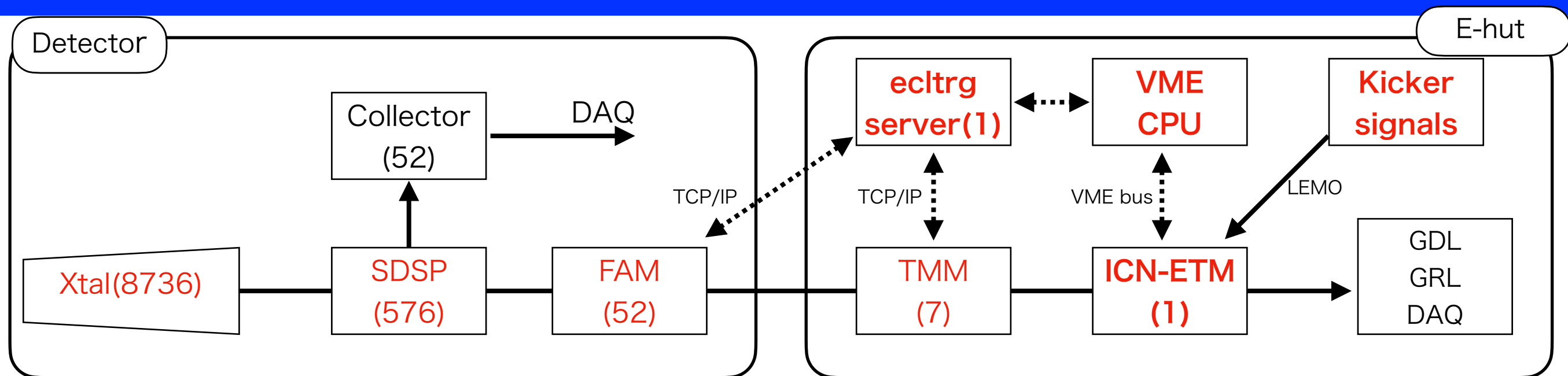
Event timing

- Investigate possible improvement by Hobin Lee and Myeongjae Lee
 - energy weighted TC timing with multiple TCs in 256ns
 - In case of $N(\text{TC}) \geq 2$, 12% improvement in resolution by offline data analysis.



- Core firmware logic is made without timing violation (36% DSP consumption)
- tsim is ready in local and the results are consistent with the expectations.
- Plan
 - check and modify FW and update software(unpacker, DQM), etc.
 - Take debug run with beam
 - Study of additional improvement by taking into account correlation with E and reso.

Real time ECL background monitor

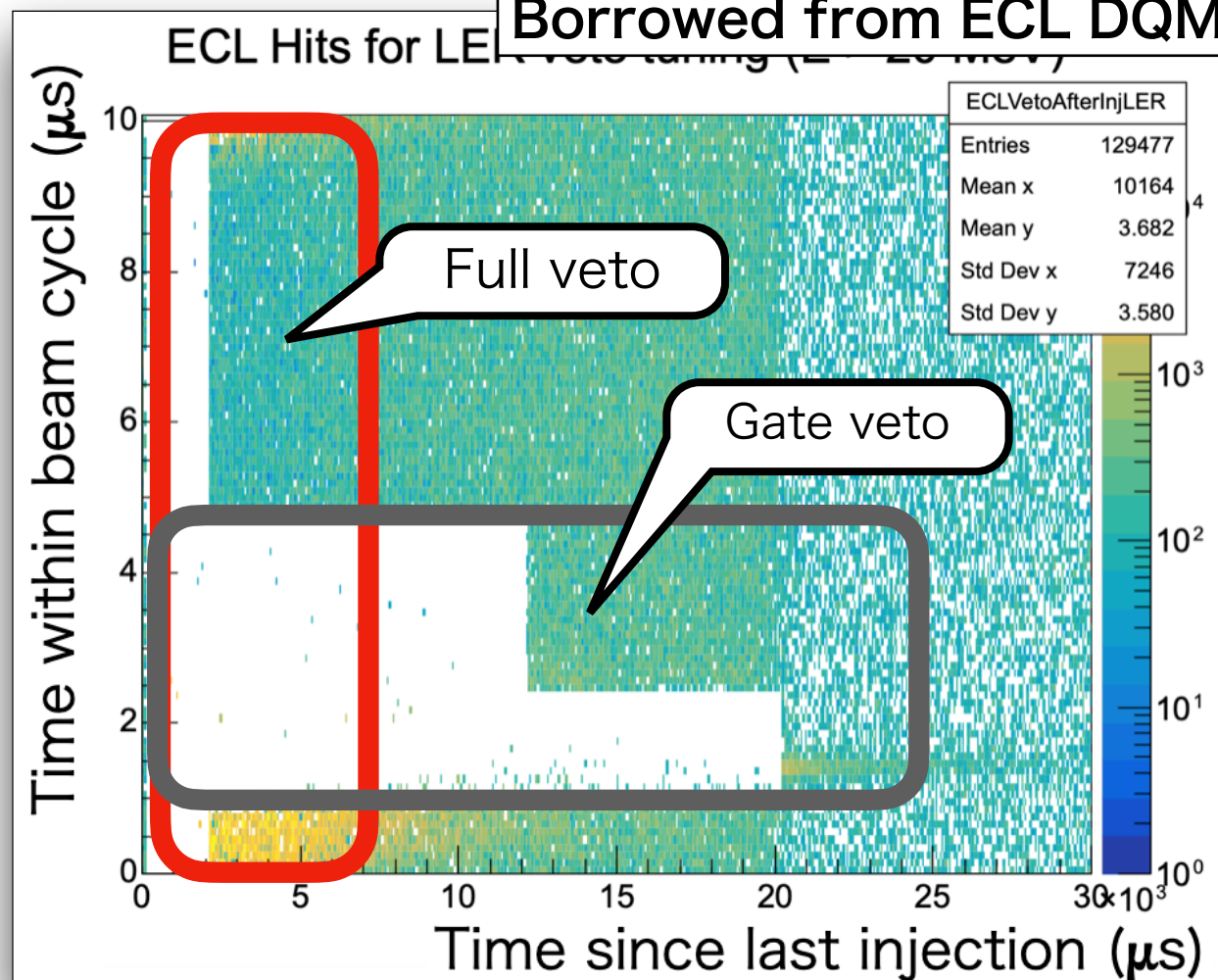


- ICN-ETM receives all 576 TC data from FAM through TMM
- ICN-ETM receives injection signals from NIM-BIN with LEMO cables
- ICN-ETM calculates TC hit rate w/ and w/o "local" injection veto
 - full veto and gate veto for LER and HER separately
- Read TC hit rates from ICN-ETM and generates the PVs

Real time ECL background monitor

- Simple GUI to control and monitor the system on beast2 server
 - Veto parameters are tunable from GUI
 - Any user can control veto parameters from beast2
- 1700PVs being archived
 - Update of PV on ICN-ETM and sampling rate of Archiver appliance are 1 Hz
 - Hit rate w/ and w/o injection veto, and veto parameters in PV list

Borrowed from ECL DQM



Control panel of ECL BKG monitor

	ALL	FW	BR	BW
(1) total hit rate w/o veto (Hz)	2475	318	1914	243
(2) total hit rate w/ veto (Hz)	1166	131	923	112
(3) calibrated total hit rate w/ veto (Hz)	2332	262	1846	224
Ratio ((2) / (1))	0.471	0.412	0.482	0.461
Ratio ((3) / (1))	0.942	0.824	0.964	0.922

	HER	LER
full veto (ms)	50.00	0.00
gate veto start in each revo cycle (us)	0.00	0.00
gate veto end in each revo cycle (us)	0.00	0.00
gate veto duration from last injection (ms)	0.00	0.00
total veto window per second (ms)	500.00	
kicker delay on ETM (ns)	0.0	0.0
Injection rate (Hz)	10.00	10.00

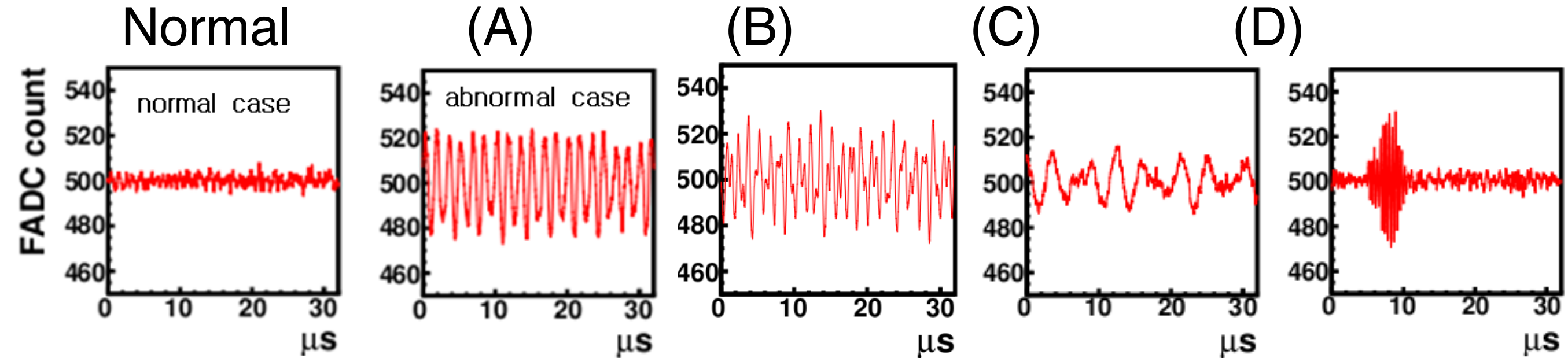
Load/Save full and gate veto parameters to DB

Load parameters

Save parameters

Noise

- 1 ADC $\sim$ 5MeV
- TC E Threshold=19 ADC



(A) ARICH FTSW => fixed at the end of 2017.

(B) TPC => TPC was gone at the end(?) of 2018.

(C) ECL

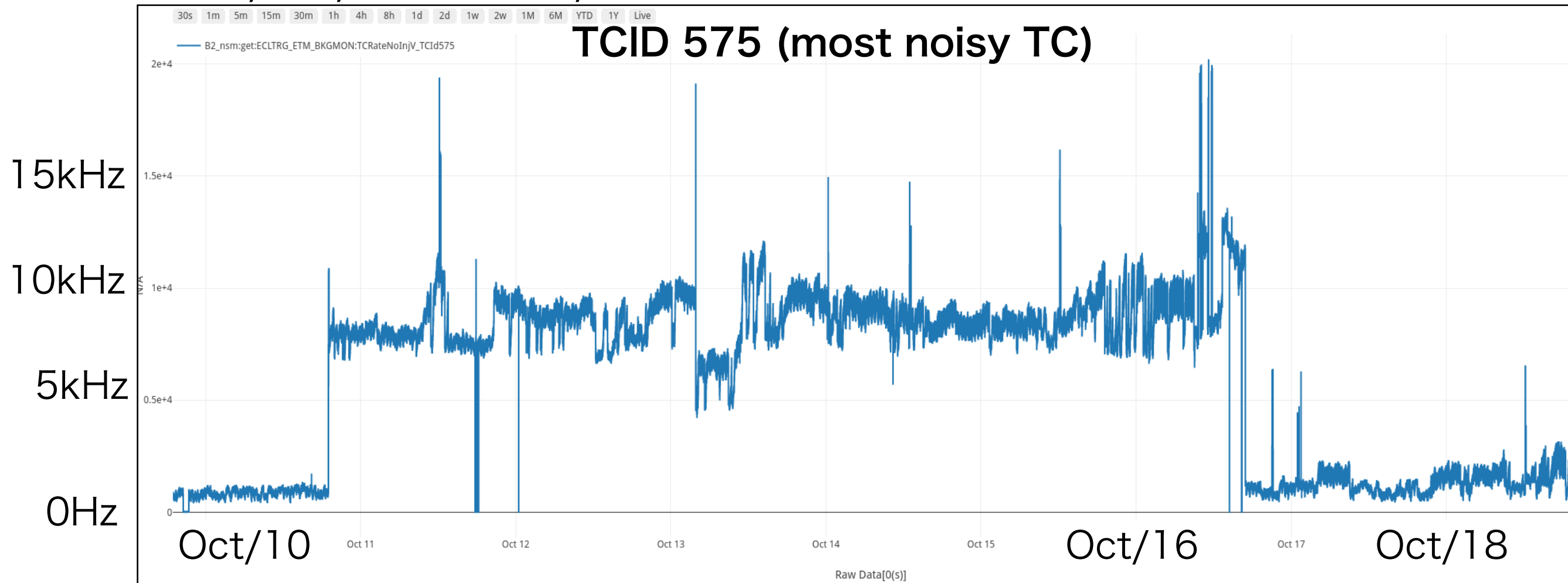
(D) Unknown source

For (C) and (D),

- Some TCs are fixed by
 - adjusting connections btw PD and PreAmp and new grounding
- Noise on some TCs remain
 - The number of noisy PCs vary (currently only 2 TCs)

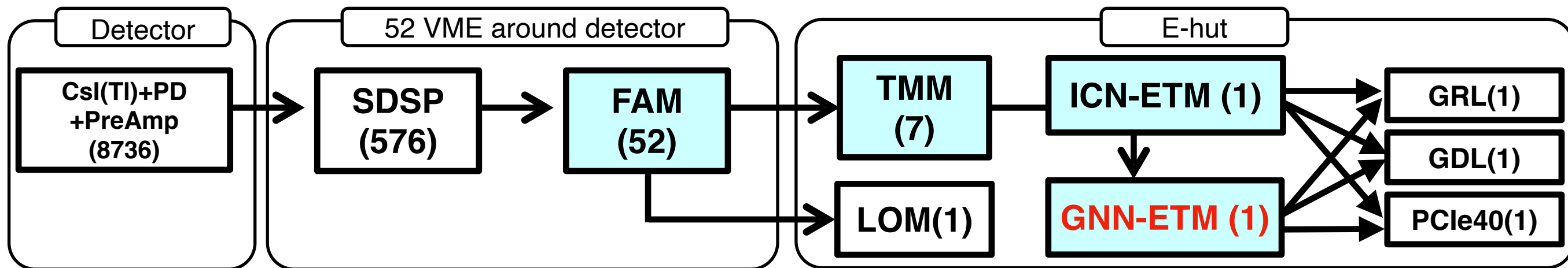
Noise

- There were VERY noisy 8 TCs in endcap just before exp35 started
- From 2024/Oct/10 to 2024/Oct16



- The reason is unknown, why appeared and disappeared.
- If noise level is too high, plan to apply higher TC energy threshold.
 - Plan to prepare conditionDB and update tsim for MC production

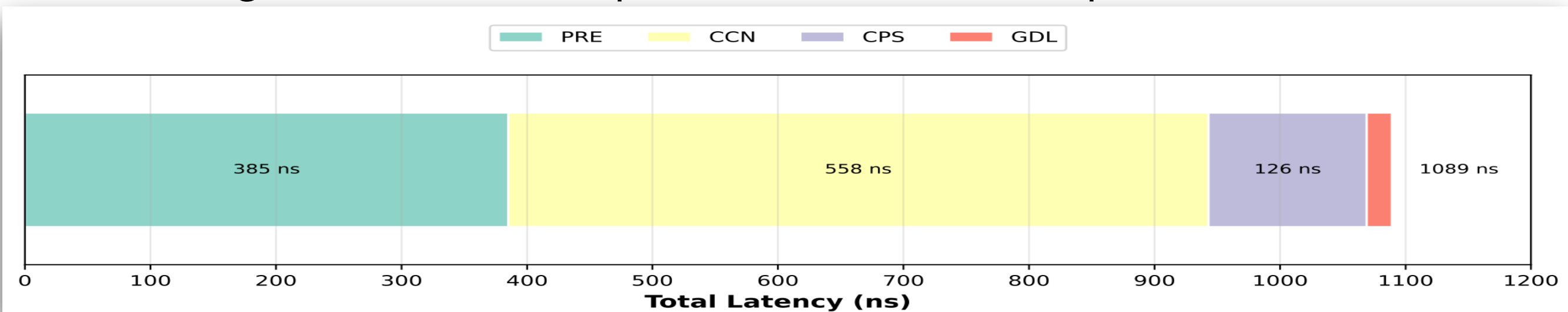
GNN-ETM



- Perform clustering based on Graph Neural Network
 - Aiming to have better resolutions of cluster energy and timing by KIT group (Torben, Isabel, Marc, Frank, Jurgen)
- Preliminary hardware configuration is done
 - Receive all TC E&T from ICN-ETM
 - Send trigger summary to GDL
 - Send cluster data to GRL
 - Send trigger summary and cluster data to DAQ
- FW preparation of link to GDL and GRL, and SLC are on-going.

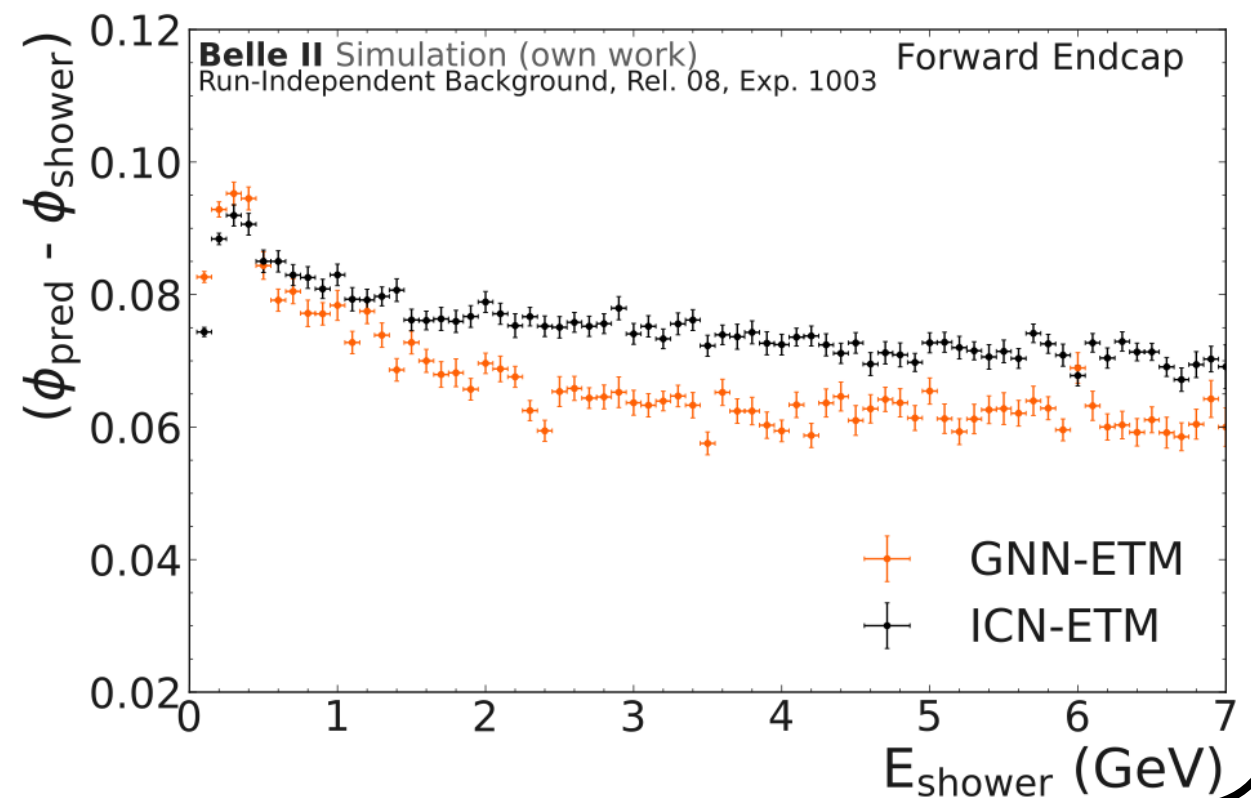
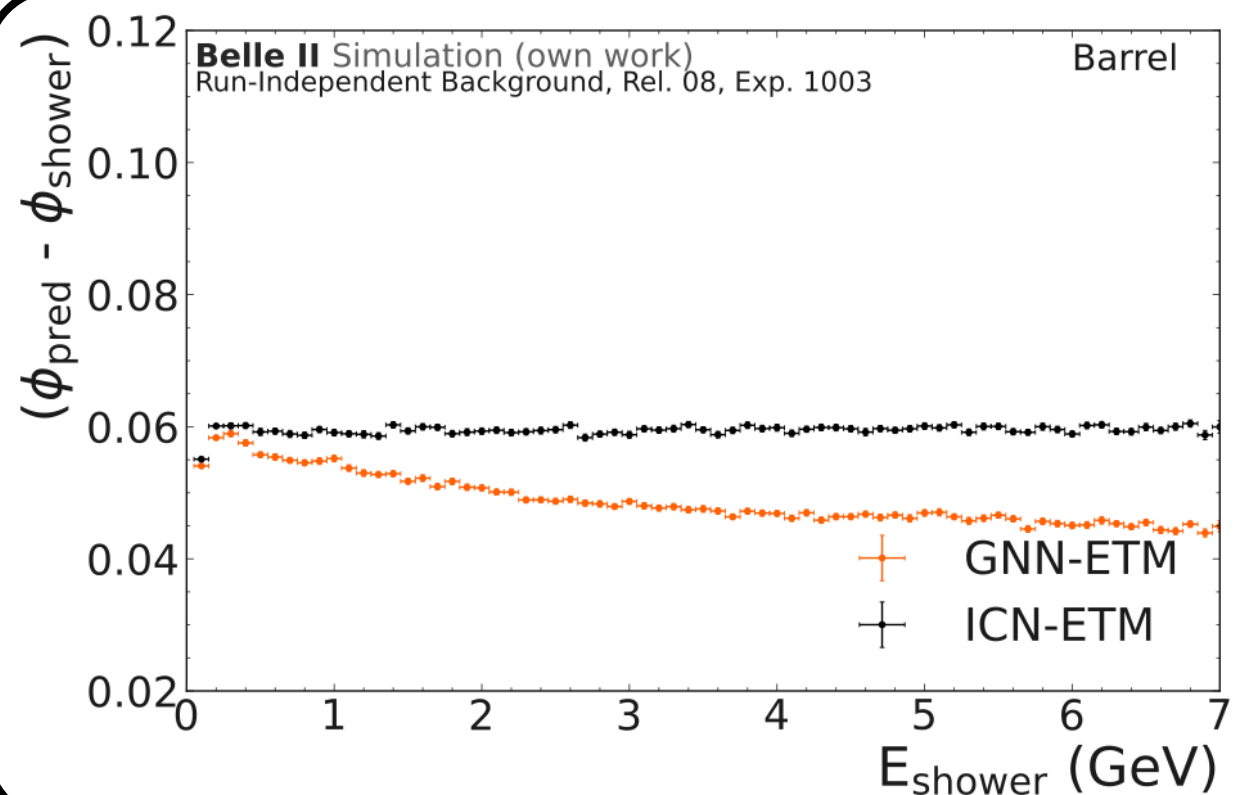
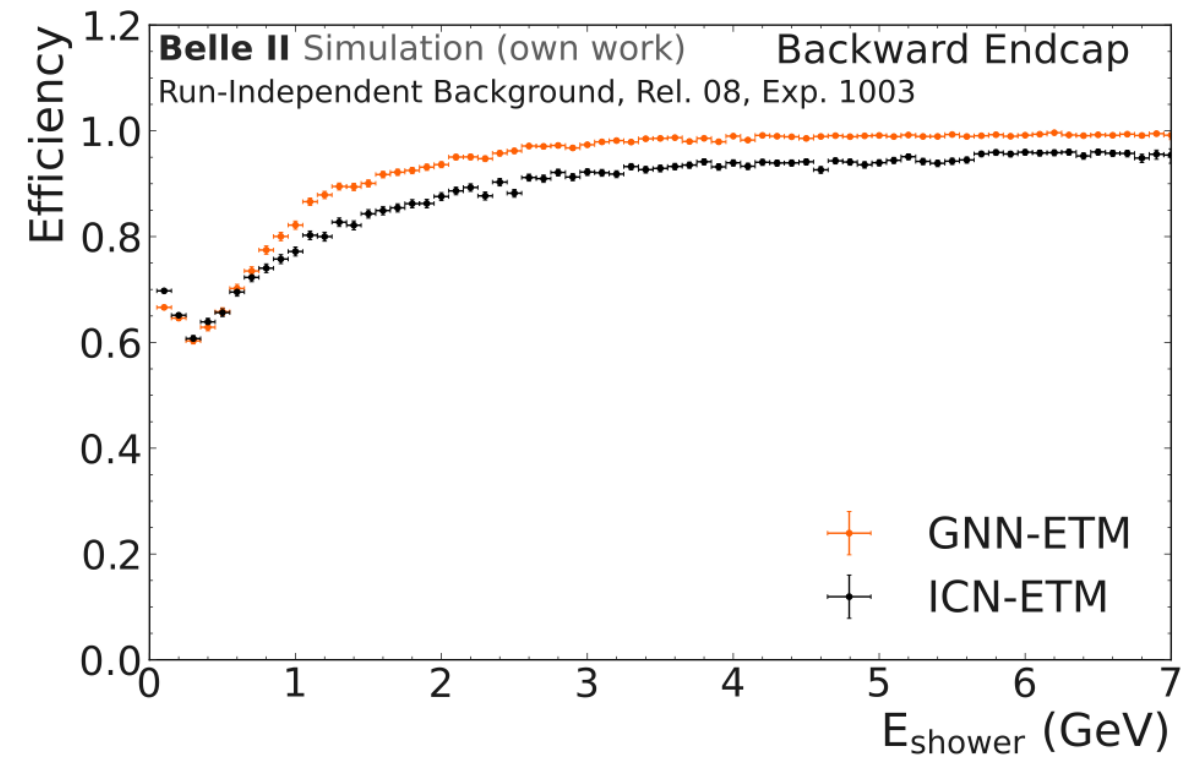
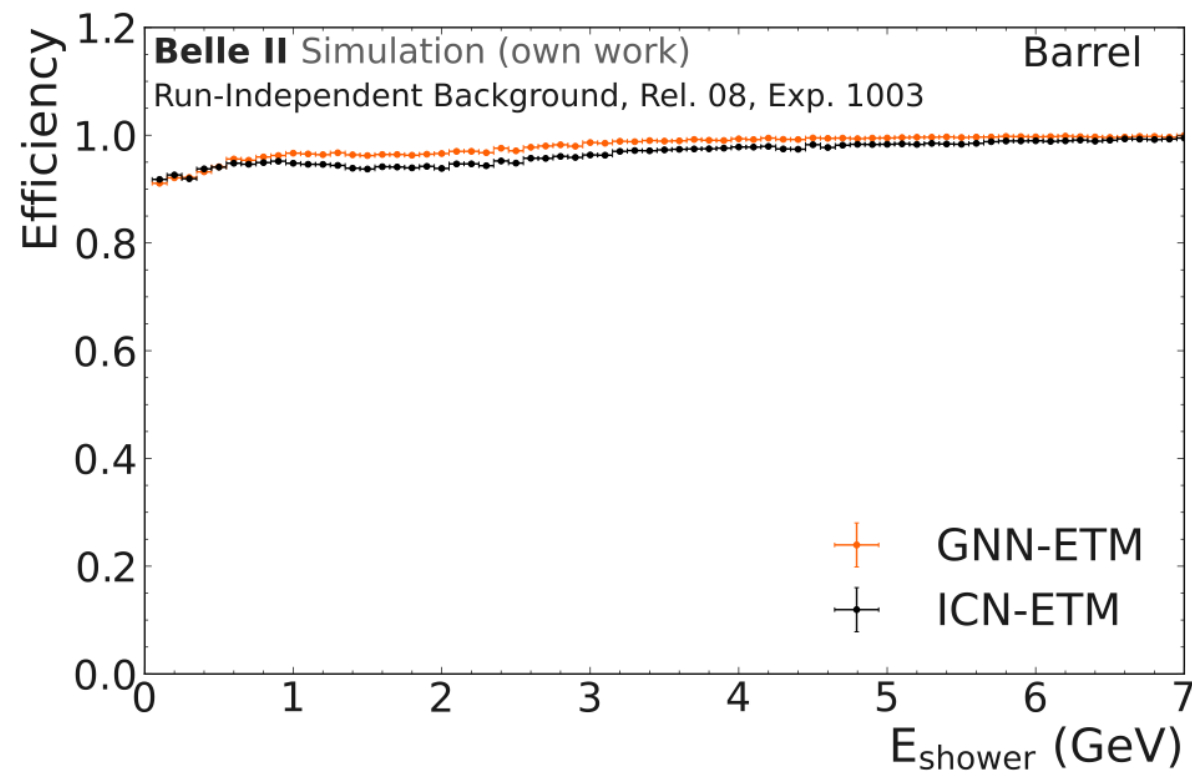
GNN-ETM

- 1st version firmware consumes **3us** latency
 - **~0.7us** latency is required with "current hardware configuration"
- Recently achieved **~1.1us** latency by long hard effort
 - smaller networks and higher clock speed(256MHz)
 - the degradation of the performance at acceptable level.



- **0.4us** latency reduction can be made by
 - 0.1us from spare latency budget for FAM
 - 0.3us by swapping ICN-ETM and GNN-ETM
 - => requires modification of both ETM FW and SLC and test.

GNN-ETM (preliminary MC results)



Others

- ttlost on one FAM happened once per month in average.
 - Fixed by replacing CAT7 with a spare
- ECL trigger servers and VME CPU board
 - Running with **SL6**(server) and **SL5(V7865)**
 - V7865 is no more in the market
 - no more support for SL6 and SL5
 - Replaced to **Rocky9**(server) and **Rocky9(Rosewood-II)**

Summary/plan

- Countermeasures for problems from link instability prepared
 - Plan to investigate and fix the source of the instability
- Bug-fixes for MC and countermeasure for firmware about eclmumu bit problems are completed
- Core logic of new event timing prepared
 - Plan to replace it with current logic next year
- Development of GNN-ETM is in progress
 - Plan to fully implement in L1 trigger line next year

Backup

Real time background monitor

- 1200 PV
 - PV list (<https://confluence.desy.de/display/BI/List+of+Archived+PVs>)
 - Hit rate w/ and w/o injection veto, and veto parameters
- Rates of PV update on ETM and sampling rate of Archiver appliance are 1 Hz

ECL trigger background monitor

#	PV name	Description	Unit	Comment
576	B2_nsm:get:ECLTRG_ETM_BKGMON:TCRateNoInjV_TCIIdXXX	• TC hit rate w/o "local injection veto"	Hz	• XXX=1-576 • "local injection veto" is generated on ETM, and is different from BelleII injection veto issued by GDL
576	B2_nsm:get:ECLTRG_ETM_BKGMON:TCRateInjV_TCIIdXXX	• TC hit rate with "local injection veto"	Hz	• XXX=1-576
4	B2_nsm:get:ECLTRG_ETM_BKGMON:TCRateNoInjV_XX	• Total TC hit rate in XX(all, FW,BR,BW) w/o "local injection veto"	Hz	• XX=AL,FW,BR,BW • AL=all TC, FW=forward TC, BR=barrel TC, BW=backward TC
4	B2_nsm:get:ECLTRG_ETM_BKGMON:TCRateInjV_XX	• Total TC hit rate in XX(all, FW,BR,BW) with "local injection veto"	Hz	• XX=AL,FW,BR,BW • AL=all TC, FW=forward TC, BR=barrel TC, BW=backward TC
4	B2_nsm:get:ECLTRG_ETM_BKGMON:TCRateInjVCorr_XX	• Total TC hit rates in XX(all, FW,BR,BW) with "local injection veto" and scaled with total veto window per second (B2_nsm:get:ECLTRG_ETM_BKGMON:InjVTime)	Hz	• XX=AL,FW,BR,BW • AL=all TC, FW=forward TC, BR=barrel TC, BW=backward TC
4	B2_nsm:get:ECLTRG_ETM_BKGMON:TCRateRatio_XX	• Ratio of TC hit rates of w/o and w/ "local injection veto" • B2_nsm:get:ECLTRG_ETM_BKGMON:TCRateInjV_TCIIdXXX / B2_nsm:get:ECLTRG_ETM_BKGMON:TCRateNoInjV_TCIIdXXX	---	• XX=AL,FW,BR,BW • AL=all TC, FW=forward TC, BR=barrel TC, BW=backward TC
4	B2_nsm:get:ECLTRG_ETM_BKGMON:TCRateRatioCorr_XX	• Ratio of TC hit rates of w/o and w/ "local injection veto" scaled with "total veto window per second" • B2_nsm:get:ECLTRG_ETM_BKGMON:TCRateInjV_TCIIdXXX / B2_nsm:get:ECLTRG_ETM_BKGMON:TCRateNoInjV_TCIIdXXX	---	• XX=AL,FW,BR,BW • AL=all TC, FW=forward TC, BR=barrel TC, BW=backward TC
1	B2_nsm:get:ECLTRG_ETM_BKGMON:InjVTime	• Total "local injection veto" window per second	ms	
2	B2_nsm:get:ECLTRG_ETM_BKGMON:InjVTime_XXX	• Total "local injection veto" window per second, associated to one of injection kicker signals (her or ler)	ms	• XXX=her or ler
2	B2_nsm:get:ECLTRG_ETM_BKGMON:InjRate_XXX	• Injection repetition rate monitored on ETM	Hz	• XXX=her or ler
2	B2_nsm:get:ECLTRG_ETM_BKGMON:fullveto_XXX	• full veto window of "local injection veto"	ms	• XXX=her or ler
4	B2_nsm:get:ECLTRG_ETM_BKGMON:gateveto_XXX_YYY	• gate veto start and finish timing in revo cycle for "local injection veto"	us	• XXX=her or ler • YYY=repeat_s or repeat_f
2	B2_nsm:get:ECLTRG_ETM_BKGMON:gateveto_XXX_duration	• gate veto duration of "local injection veto"	ms	• XXX=her or ler

Software status

- (Issue 11174)
 - Memory leak in TrgEclCluster.cc was reported by Carvalho Ana Luisa
 - Index for some array was out of range and it caused memory leak.
 - The bugfix was prepared and merged to main.
 - No change in the result of tsim.
- No progress on following items.

- (issue#10503) tsim does not reproduce same result with same random seed, pointed out by Isabel
 - Not started yet
- (issue#10711) improper TC position in tsim, reported by Isabel
 - Not started yet
- Update of tsim and dbobject for FAM
 - Not started yet

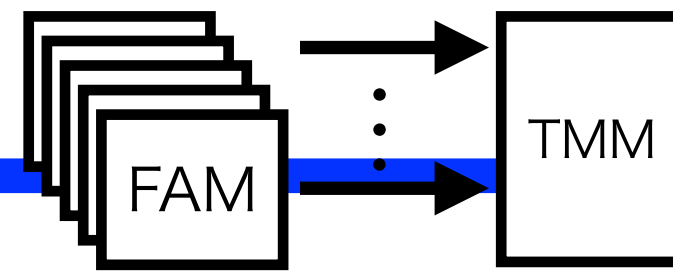
Summary/Plan

Plan shown at past B2GM

- Investigate the reason of TMM-ETM link instability
- Prepare logic to detect TMM-ETM link instability from data Done
- Update data alignment logic in TMM and ETM Done
- Update DQM
- Update ETM slow control to have parameter check logic Done
- OS update for btrgctr0/1 (together with all servers in B2) Done
- Investigation of FAM29 ttlost Done
- Investigation of noisy TC
- Update tsim to utilize condition database Done
- Update CSS (TRG and ECL) In progress
- Improve timing logic (Hobin Lee(SNU)) Core logic ready

- Preparation to replace ICN-ETM and GNN-ETM configuration
 - FAM → TMM → INC-ETM → GDL
 - ↳ GNN-ETM (→ GDL)

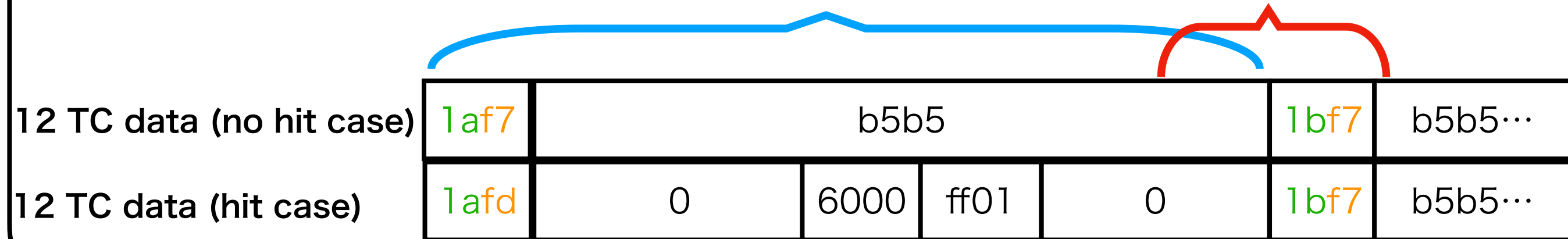
Data alignment



- We had alignment problem in past operations

$$16\text{clk}(128\text{ns}) = 1\text{clk}(\text{header}) + 15\text{clk}(12\text{TC data})$$

Use for alignment



- Current logic:

- (1) Find header by looking at "B5B5" for a few clks and fixed 8bit header "f7" and
- (2) perform alignment using header positions
- => at (1), sometimes header position is incorrectly identified.

- New logic:

- (1-1) Send control symbol (CHARISK) associated to a header from TX
- (1-2) Detect control symbol at RX and utilize it as a signal of header position.
- (2) perform alignment using header positions
- => logically same problem with old logic will never happen (if link is stable)
- New logic was implemented on both TMM and ETM
 - Monitoring firmware logic was prepared too (SLC update has yet to be done).

Update of monitoring logic

- Data flow problems in exp35
 - run 738-740(25min) (categorized as BAD run)
 - run 2870-2888 (not categorized as BAD run)
- Essential cause of the problem is link instability
 - But not fixed yet and will be tackled
- Needs monitoring firmware logic at both TMM and ETM to detect the problem w/o looking at DQM
- New monitoring firmware logic was implemented on TMM and ETM
 - Continuously check signal of control symbol associated to header and data
 - Signal of control symbol is '1' at every 16 clock cycle
 - if "B5B5" in 15 clocks or not when header is "F7" (<- no TC hit)
- Plan to update SLC to issue error signal on "ready_signal" to stop global run.

