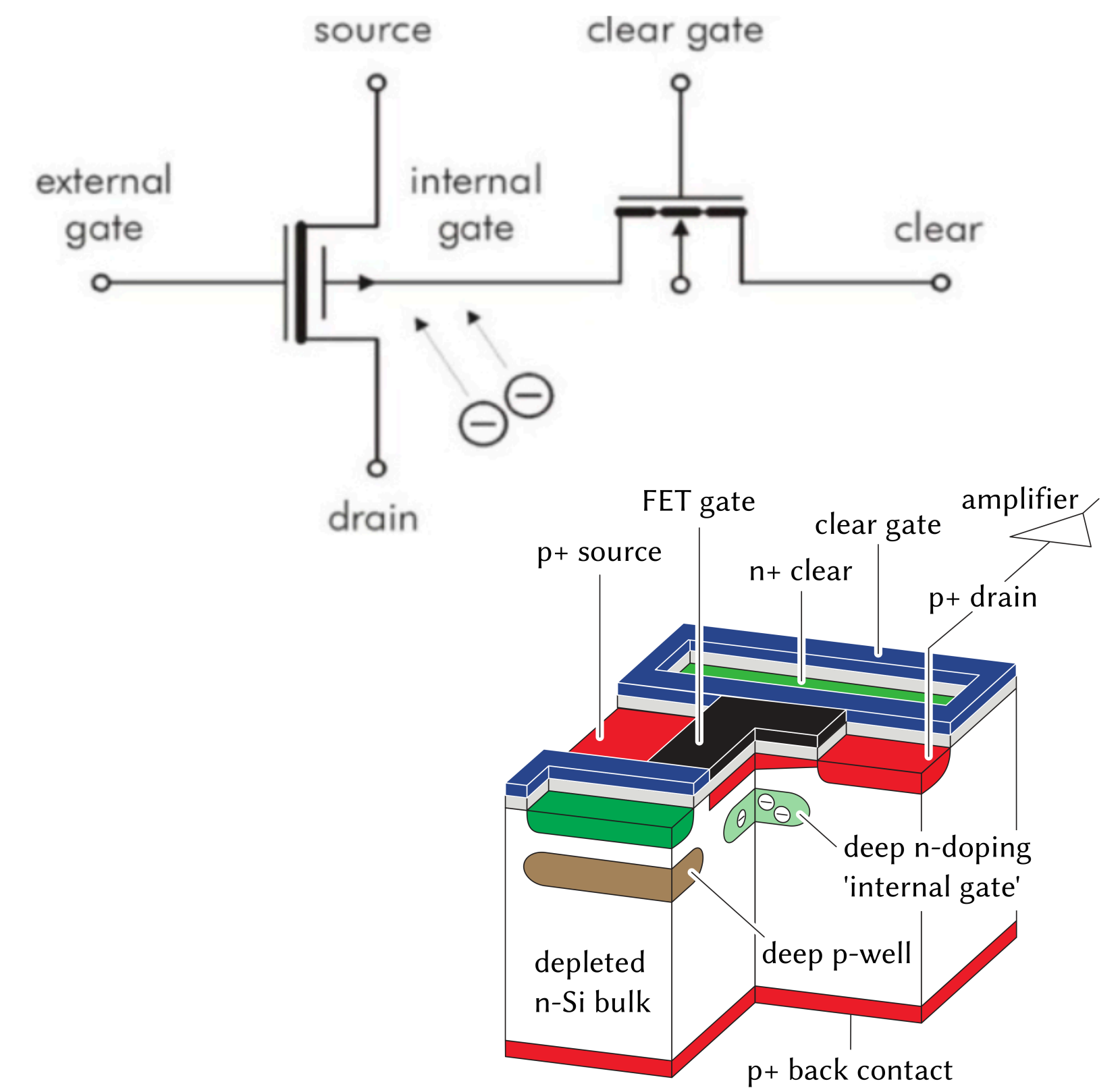


PXD

Status and Readiness

Detector Concept

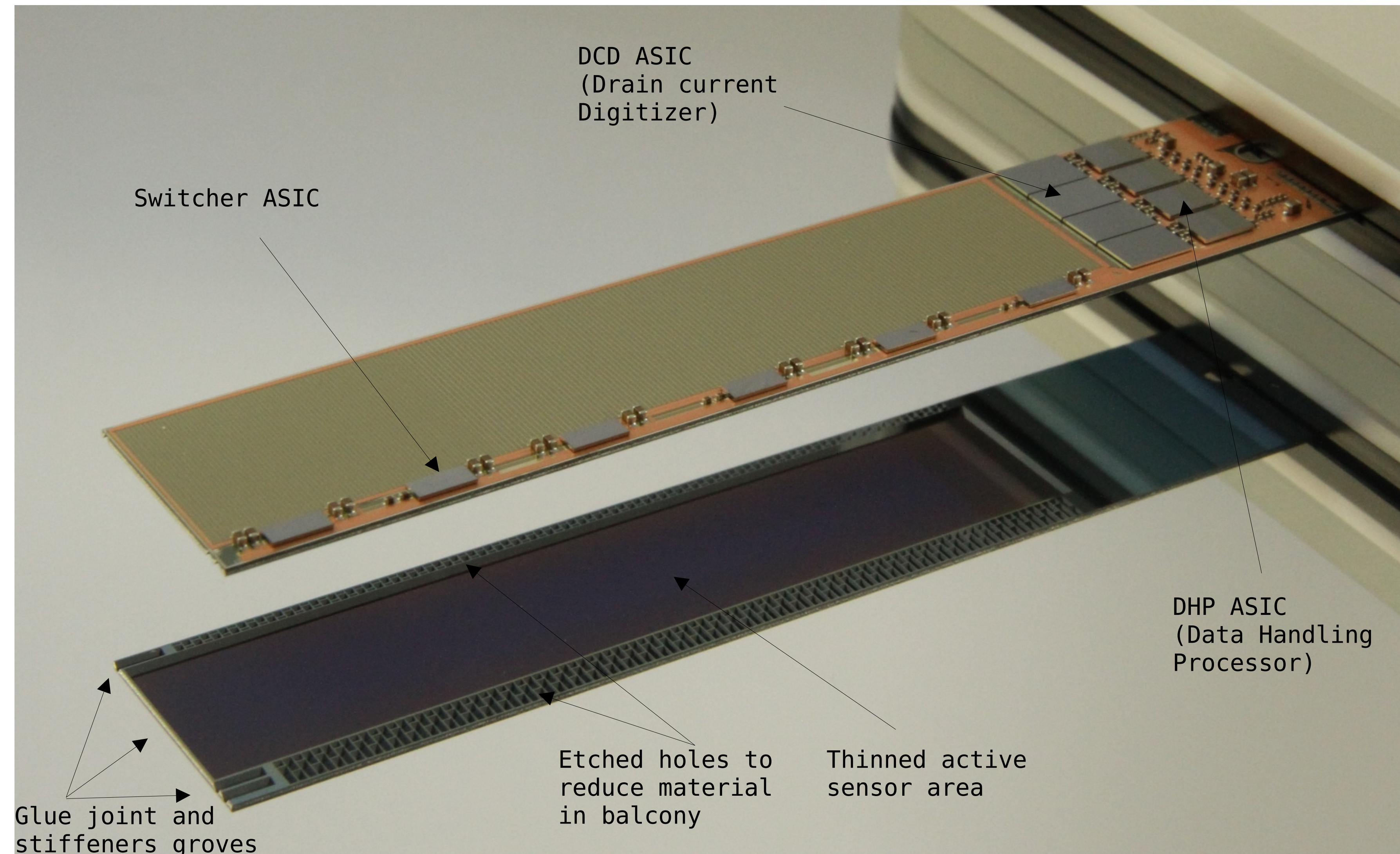
- Depleted P-channel Field-Effect Transistor (DEPFET) pixels on fully depleted silicon bulk
- Fast charge collection ($\sim$ ns) into internal gate; modulating readout current until cleared manually



PXD Module

- Mechanically self-supporting 75 μ m thin module
- 250x768 pixels with sizes down to 50x55 μ m²
- 40 modules placed in two layers around support cooling block in windmill structure
- Always two modules glued together allowing connectivity from forward and backward side
- Readout performed by 4 DHPs, 4 DCDs and 6 Switchers in rolling shutter mode within 20 μ s

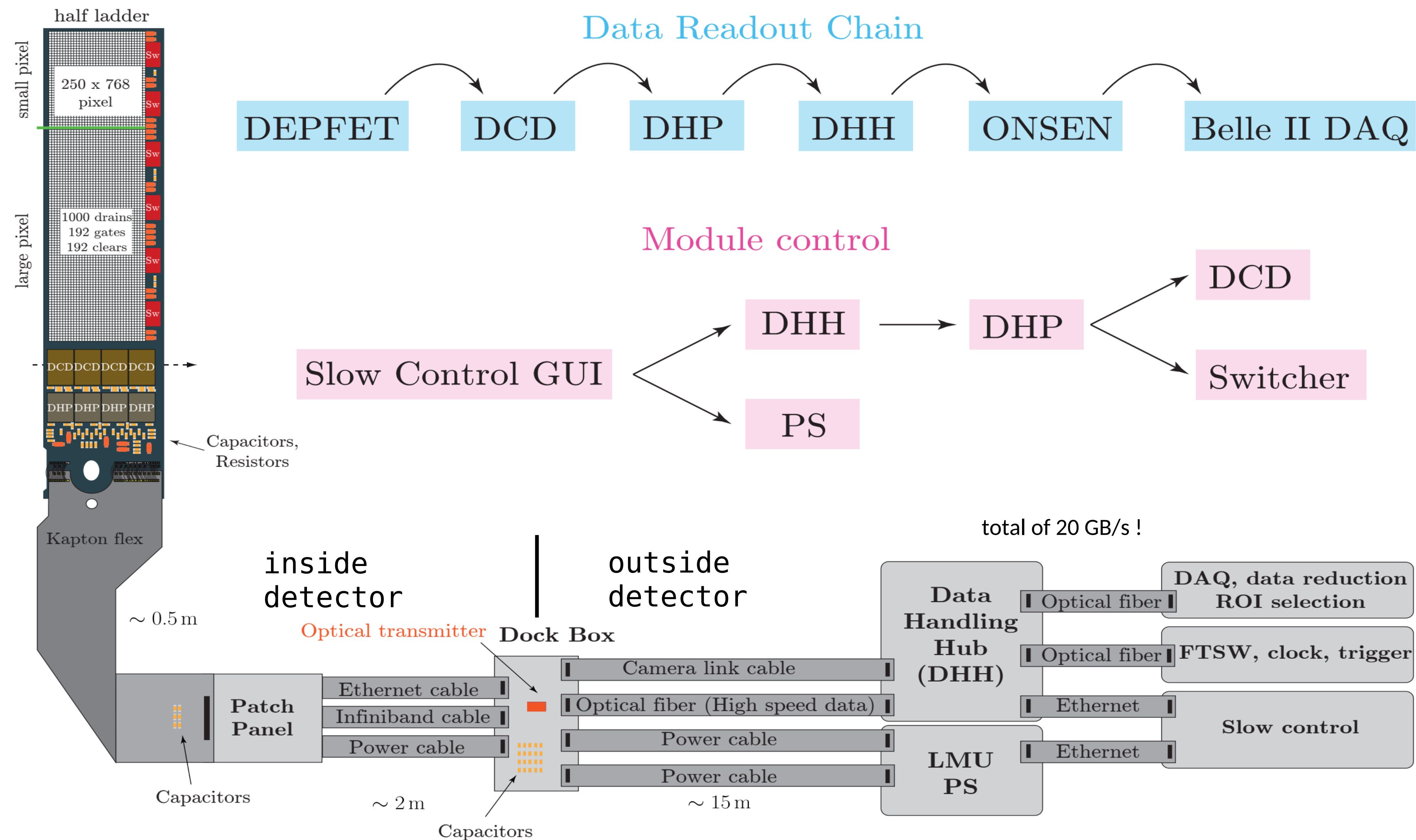
PXD Module



DAQ Scheme

- DHP ASICs perform zero-suppression to eliminate dark current and noise
- PXD data rates are expected to be 10x that of other Belle II detectors
 - 1–1.5% occupancy in layer 1, DAQ designed to cope up to 3%
- Most data originates from background requiring online data reduction
- Data Reduction based on reconstruction of interesting events and interpolation of tracks from outer detectors to PXD
- PXD data has to be buffered and HLT decision arrives

Control and Readout Chain



DAQ Scheme

- 40 DHEs receives data of 4 DHPs each
- Concentrator DHC builds events of 5 DHEs and forwards data to 4 ONSEN nodes each
- 32 ONSEN nodes (48 GB RAM total) buffer data for ~ up to 5 seconds
 - HLT information is mandatory for each event to clear buffers
 - Two-part reduction possible
 - (a) discard full event (~ 2/3 of events)
 - (b) discard data points far away from extrapolated areas (ROI) (~ 90% of data)

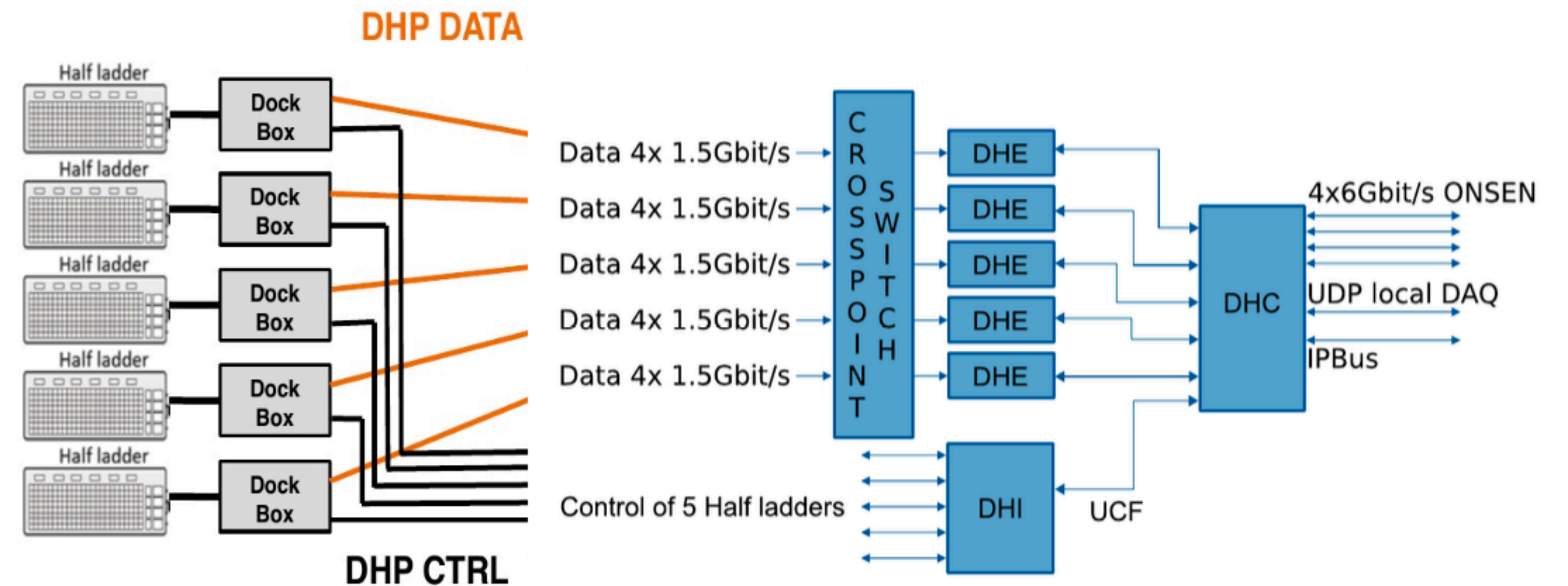
Total Reduction Factor: 30

- Final PXD data is merged afterwards by Event Builder 2

ROI calculation on HLT is always on
but filtering is currently turned off as
data rates are still low

DAQ Setup

- Different boards involved
 - DHI – module control (JTAG, TRG)
 - DHE – data readout, trigger matching
 - DHC – data concentration
 - ONSEN – buffering and data reduction
- Optimization
 - Load balancing with 2 inner and 3 outer modules done to reduce mean DHC data rate
 - DHC data distributed to 4 ONSEN in round robin scheme (must be applied on EB2 side as well)

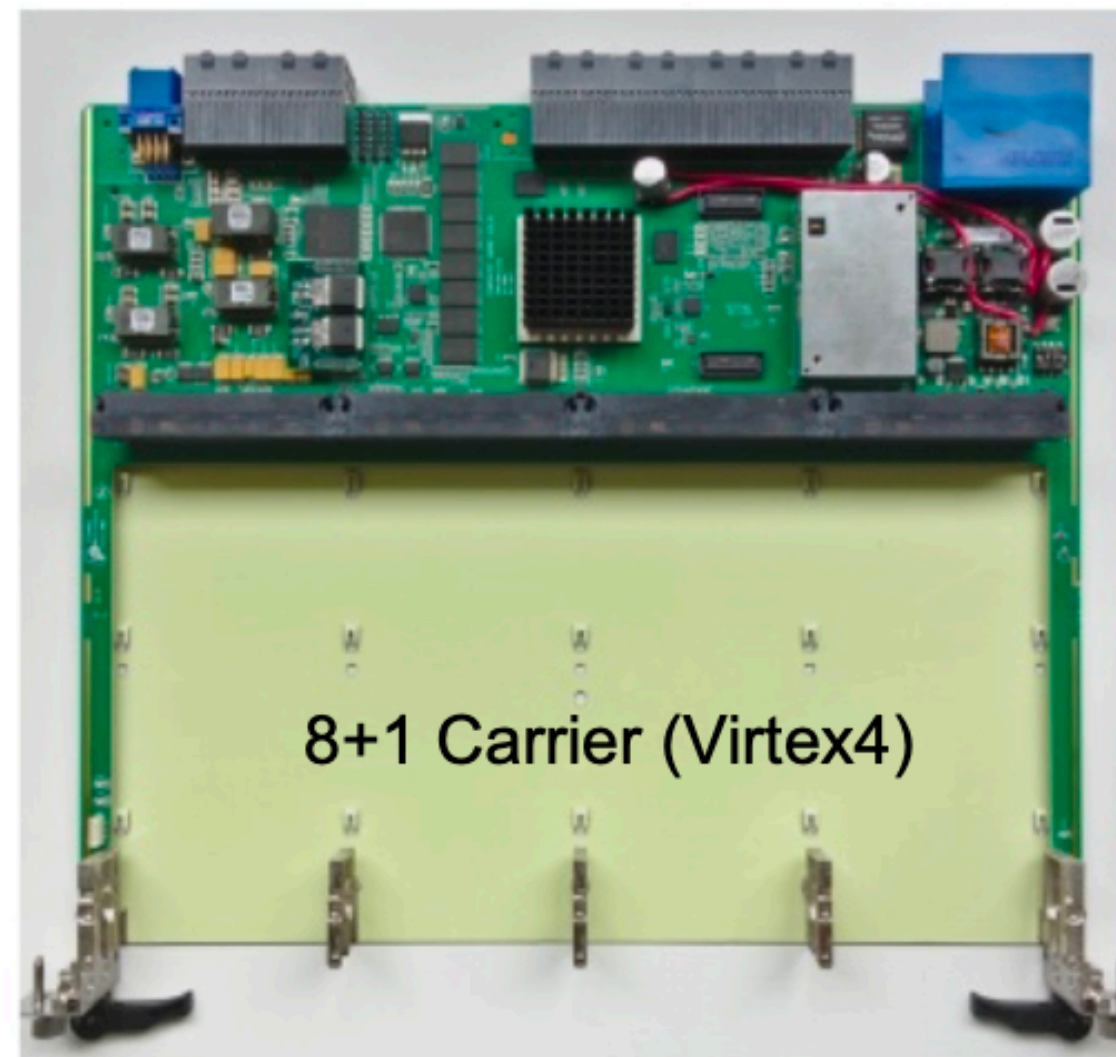


DAQ Hardware

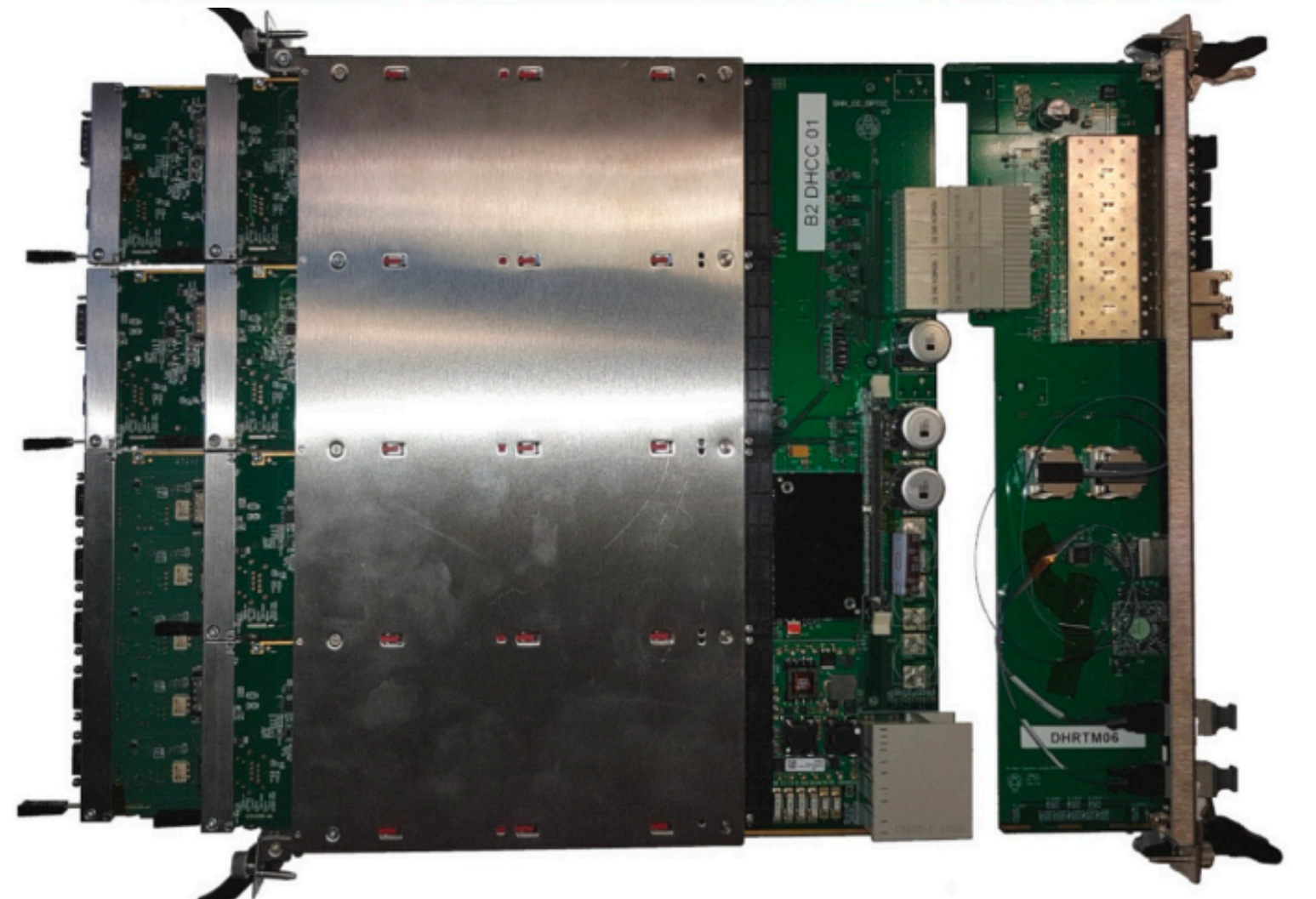
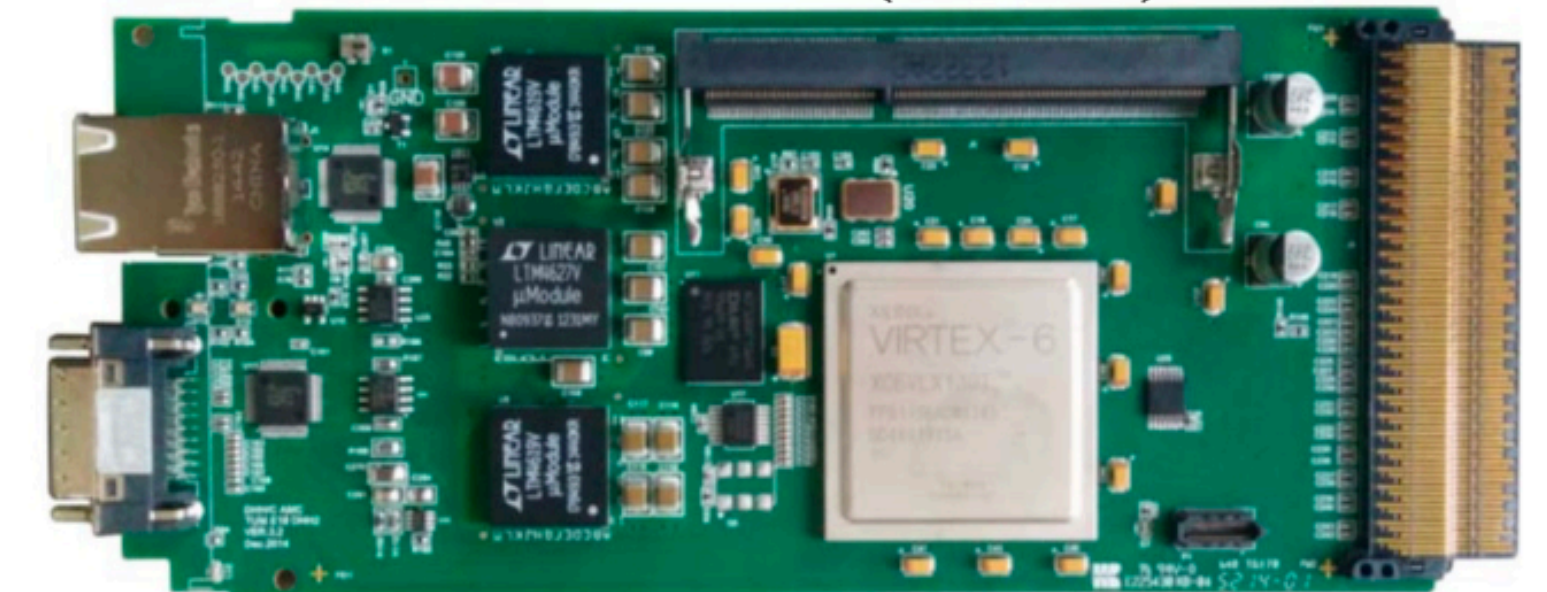
32 ONSEN AMC cards (Virtex5)



- Based on ATCA standard
- ONSEN and DHH use self-developed ATCA carrier boards with Advanced Mezzanine Cards (AMC)
- Follow IPMI standard allowing remote power monitoring and controlling



40+8 AMC (Virtex 6)



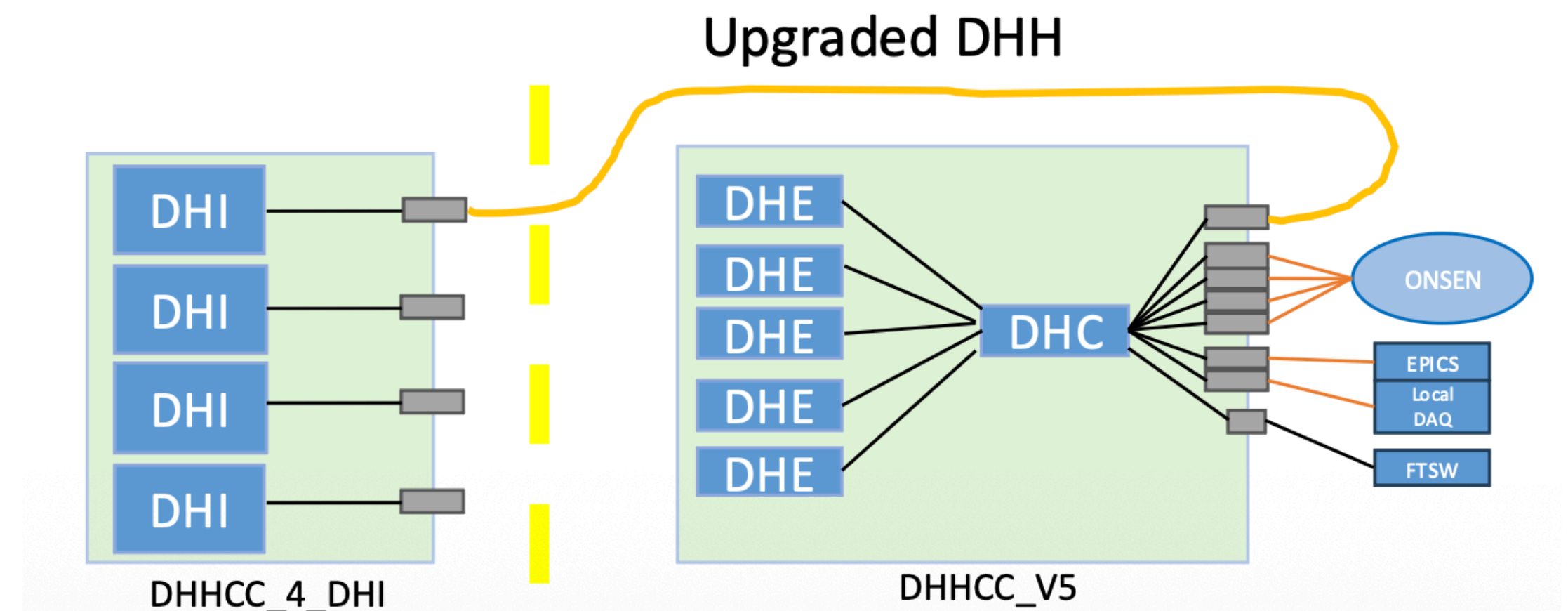
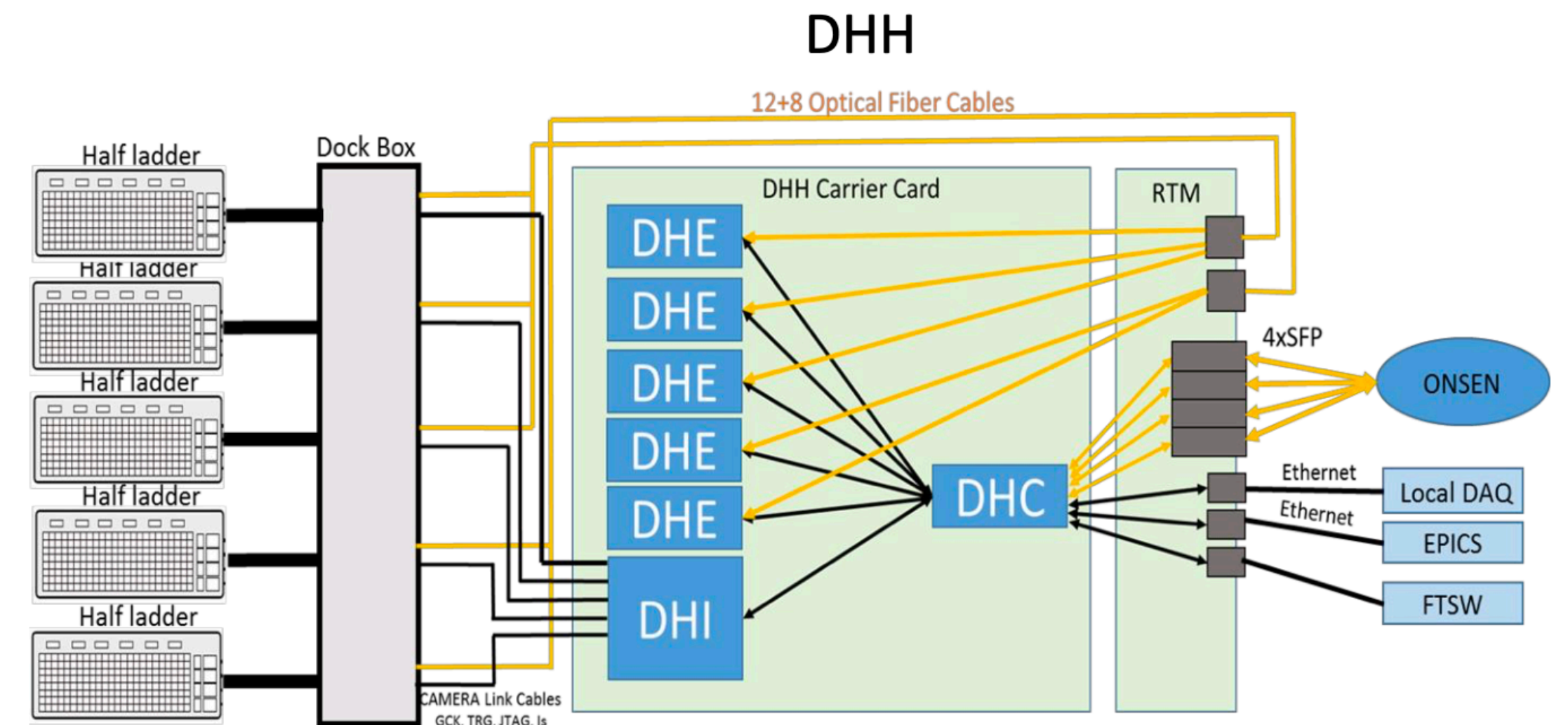
DAQ Stability

- Several long down times and emergency access to replace components
- Instability of clock recovered from Belle2 trigger link (mainly in one DHH unit)
- Boards inaccessible by slow control
- Some DHP links to DHE are unstable: errors and link drops
 - Difference to PXD1 unclear. Pre-emphasis adjusted, but for some ASICs there seem to be no optimal setting

DHH Upgrade 2025

- New DHH Carrier Card Design
- Allows designed bandwidth between DHC and DHE (500MB/s)
- Allows relocation of DHC/DHE outside of radiation controller area for faster access
- Place connectors of Rear Transition Module (RTM) directly on carrier to improve link quality to ONSEN at 6Gbps

Link Speed was reduced to 3Gbps to reduce link errors in 2023



Slow Control and Monitoring

- PXD Slow Control uses EPICS
- Configuration stored in our PXD ConfigDB
 - Sophisticated sequences for powering the modules (ASICs), interchange of power up and configuration of ASICs
- PXD EPICS Archiver
 - > 20,000 PVs (voltages, currents, data rates, ... —> > 200 GB/y)
- Logging: DB with Elasticsearch, Elog, Mattermost
- GUI application Phoebus in production now
 - Includes alarm system, logging interface

Slow Control and Monitoring

- >40 EPICS IOCs providing >100,000 PVs
 - Module and DAQ Configuration
 - Fast DQM on PXD Local DAQ
 - Calibration Tools
 - Shifting Tools (Elog entries, Login)
- All are handled by systemd and restarting automatically to reduce possible downtimes
- Since 2025 most PVs are not writable permanently, instead shifter have to enable access first to prevent unintentional changes to the system

DAQ for PXD2

- DAQ components increased from 4 to 8 DHH to read out 40 modules
- Full ONSEN shelf powered and EB2 configuration updated
 - High Rate Tests already performed before PXD1
- New start scripts for Slow Control to expand module count
- Everything else already designed earlier for full system
 - > no surprises

Summary

- Introducing PXD DAQ and data reduction concept
- PXD Slow Control and DAQ stable
- No fundamental changes planned in neither DAQ nor SC/Monitoring for next years
 - Focus on failover and future proof setup