CDC

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Belle II Trigger/DAQ Workshop 2025 @Umeda, Osaka

Many thanks to the TRG, DAQ, KLM, and ECL experts for supporting our CDC studies during this shutdown period. 👷

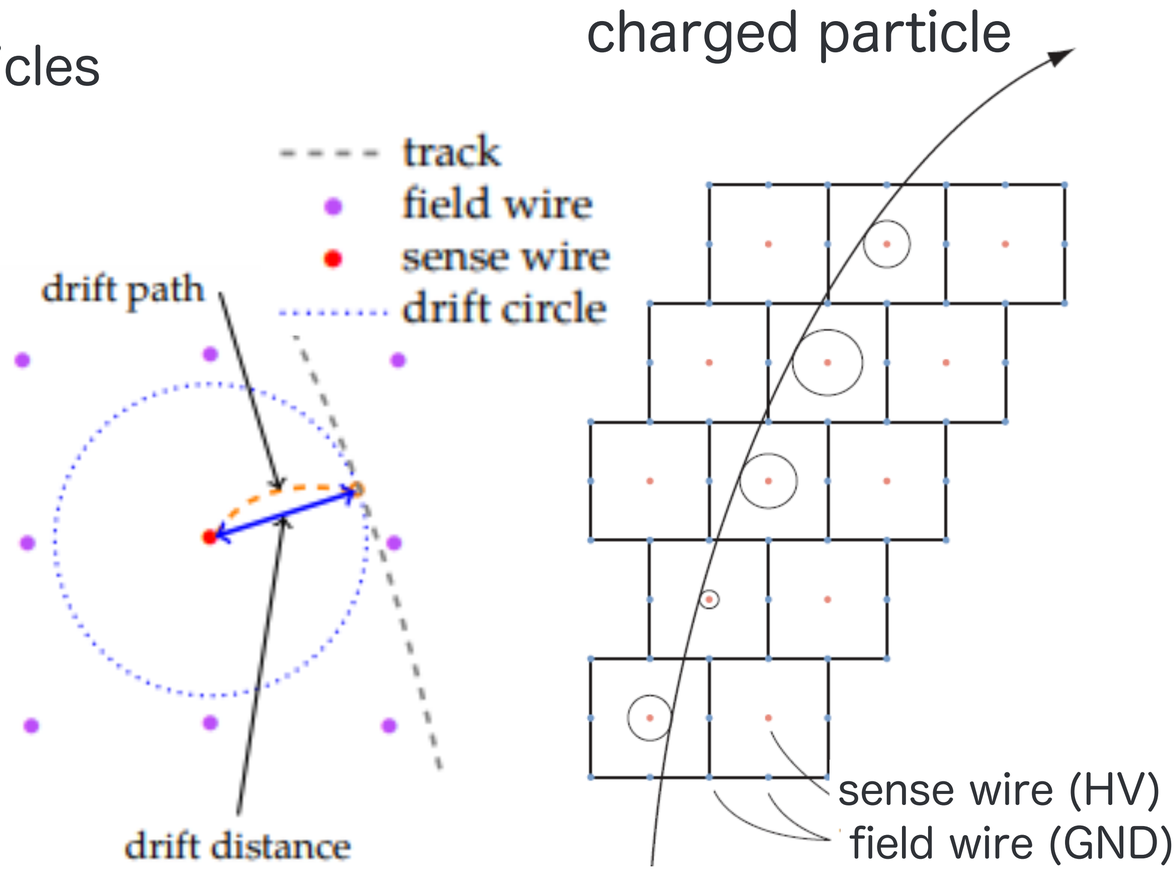
Central Drift Chamber; CDC

Role: Measuring charged particles

- From track reconstruction: particle multiplicity, charge, momentum, and production point
- Particle ID from energy loss (dE/dx)
- Low material budget to minimize impact on particles

Drift chamber w/ gas avalanche

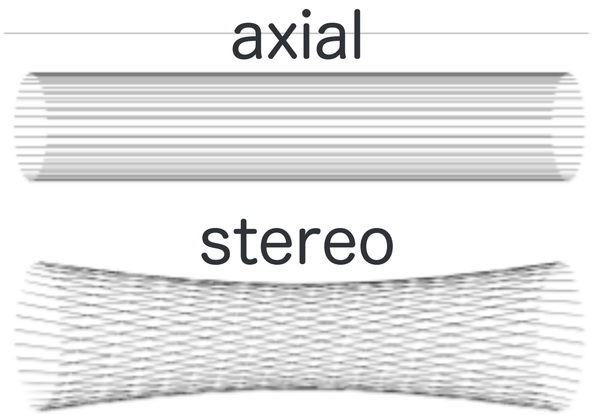
- A charged particle ionizes the gas molecules
- Electrons drift towards the anode
- Near the anode, drifting electrons cause the gas avalanche
- Measure the induced charge from ion motion
  - Position from the drift time
  - Energy loss from the signal amplitude

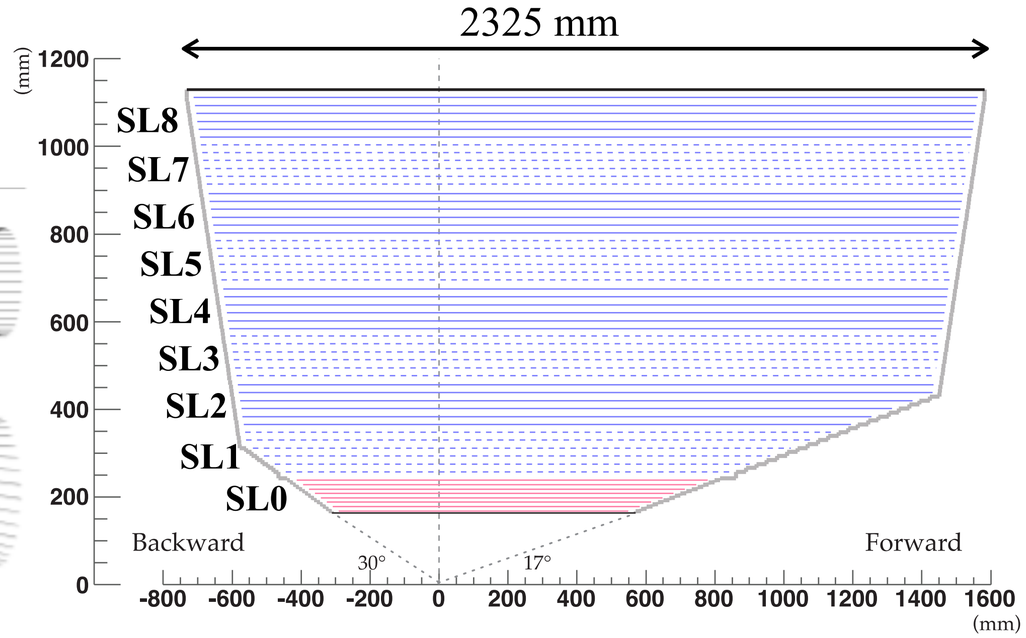


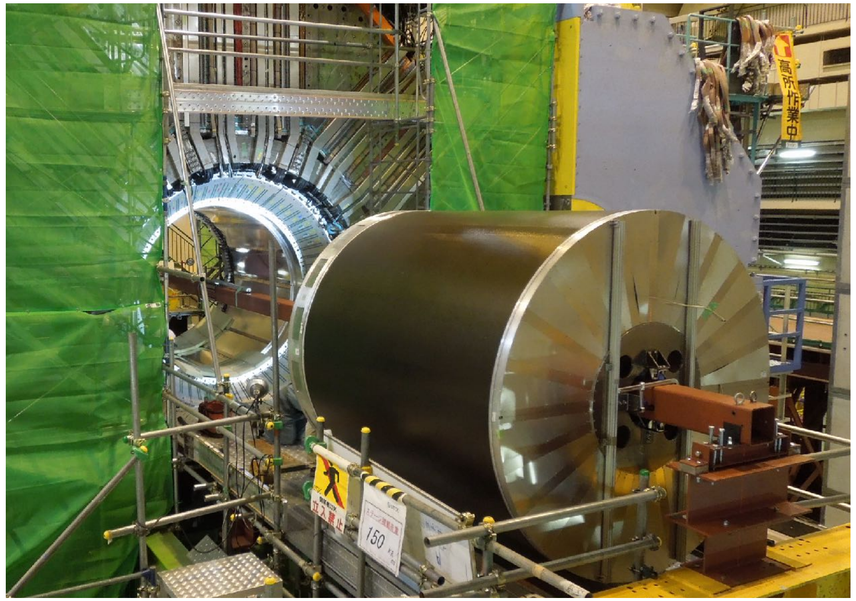
Central Drift Chamber

Structure and Components

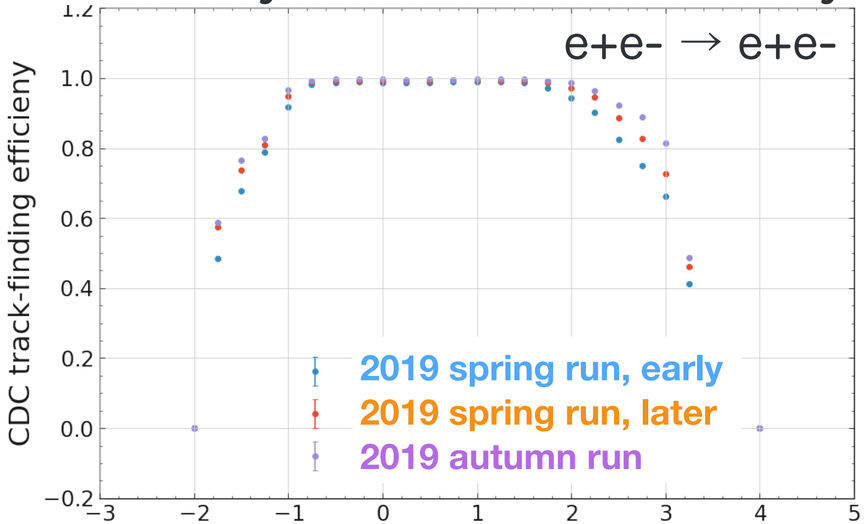
- Sense: 30-um Au-W, ~14k wire
- Field: 126-um Al, ~42k wire
- Gas: He:C_2H_6 = 50:50
- HV: ~2300 V for 2 x 10^4 gain
- 3D tracking using stereo layers



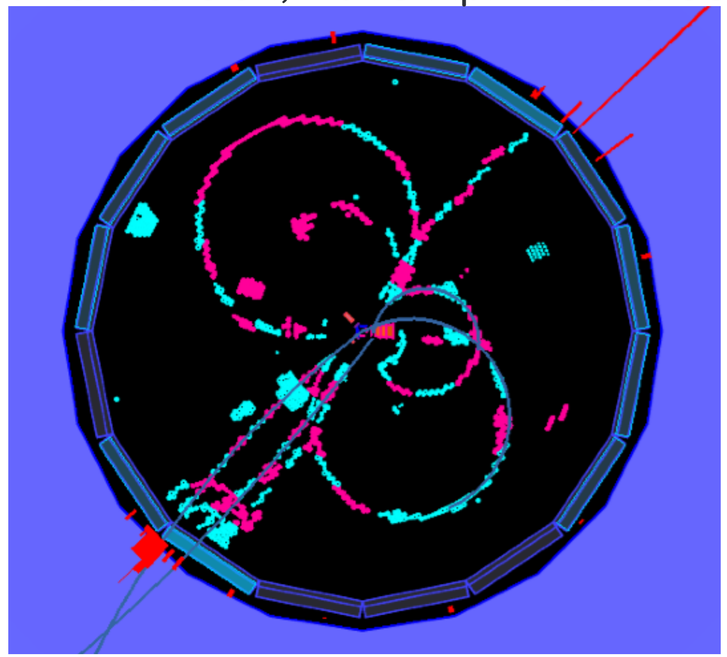




Geometry -> Detection efficiency



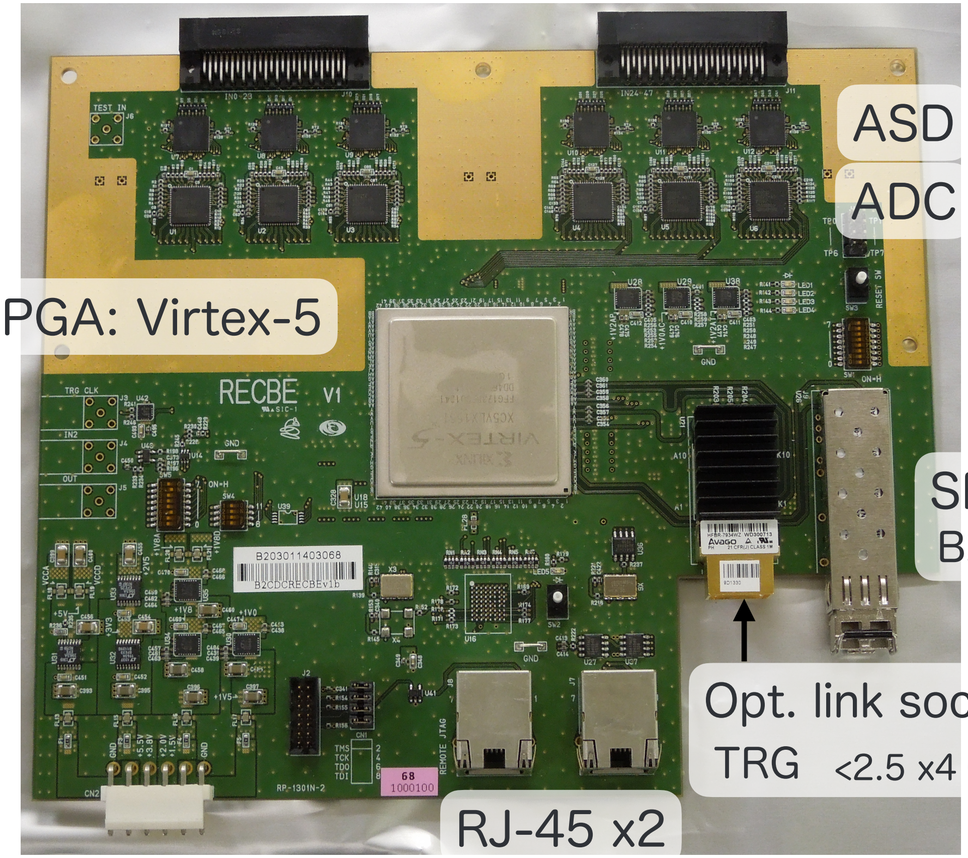
first collision, 2018 Apr. 26th 0:38



CDC FE Module

Role

- Amplifies and shapes CDC signals
  + digitizes them
  - ADC: 2 Vp-p, 10-bit, 31.75 MSPS
  - TDC: ~1 GHz
  - timing info. is also used for CDCTRG
- Receives trigger and transfers event data



Parameters

- 14336 channels
- 299 FEs: 48 ch/FE
- 1 FE reads 3-layer x 16 cells
- 7 PCIe40

[Current issues]

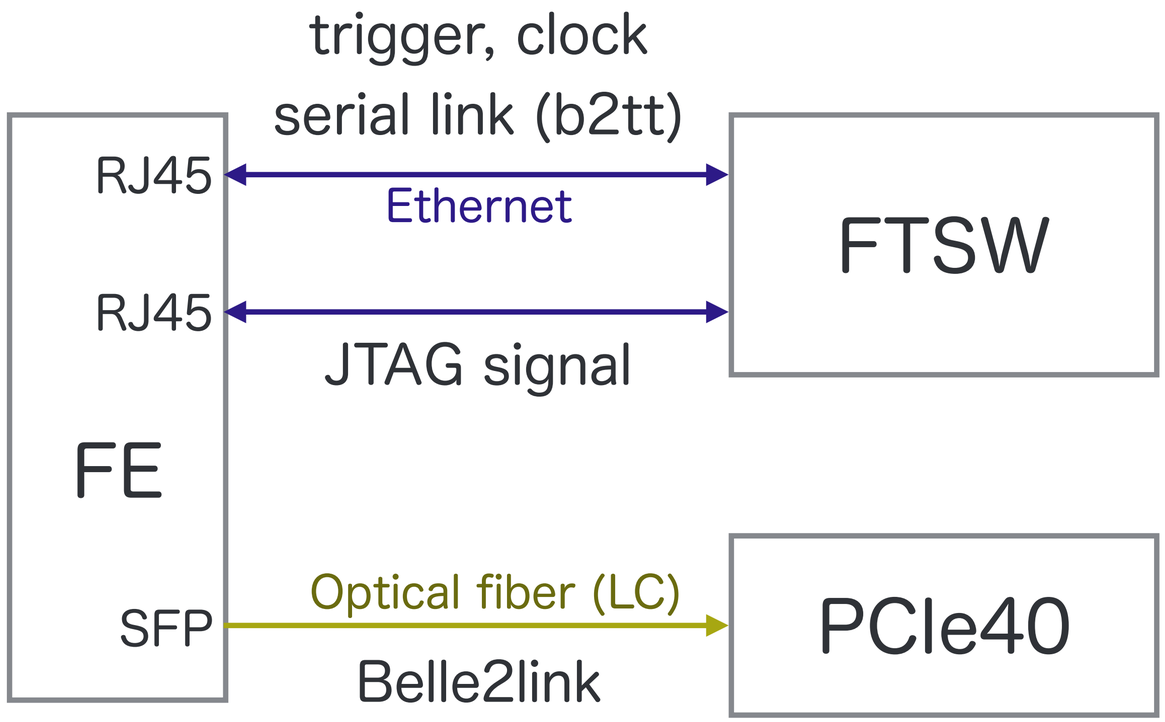
Crosstalk in ASIC

higher L1 rate <- Recent CDCTRG solves this

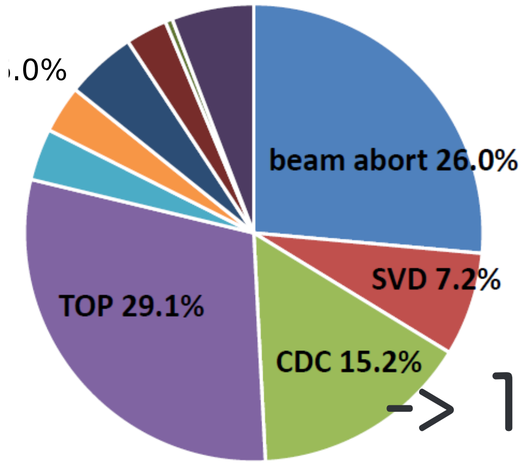
DAQ error during physics run

Soft error (Single Event Upset: SEU) due to radiation ??

CDC FE Module and FTSW/PCIe40



Run-stop
2025C



-> 15.2%

FE module

- Digitization of detector signals
- [CDC] 299 FE modules

FTSW for B2TT + JTAG

- 254 Mbps serial link (B2TT)
  [to FE] trigger and commands
  [from FE] FE-state check
- JTAG signal : FPGA configuration

PCIe40 for Belle2link

- Receive detector-signal data processed on FEs

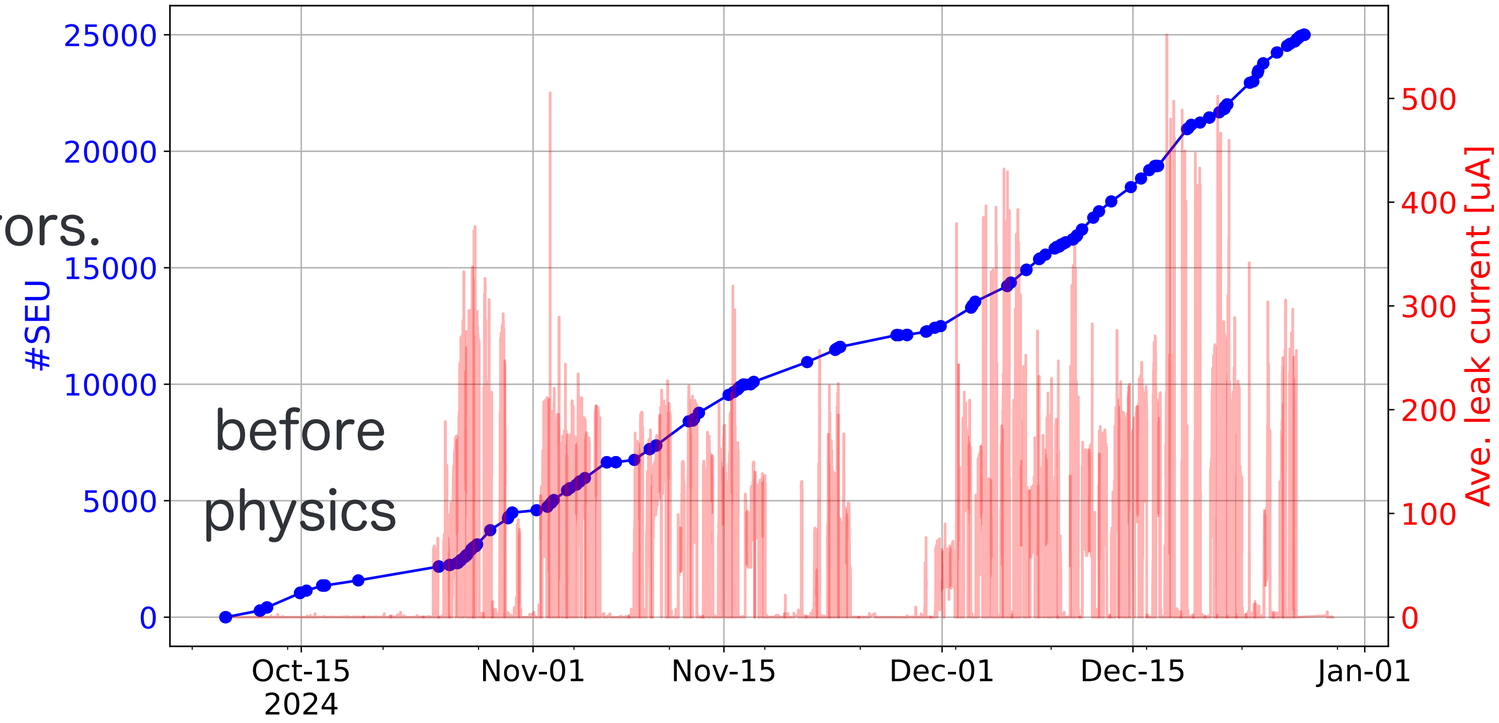
#SEUs on CDC FEE in 2024c

During LS1, we fixed the remote JTAG to repair SEUs correctly.

- Before LS1, an SEU-repair scheme had been implemented, but SEUs were not fixed.

#SEUs can be counted.

- #SEUs is logged when the firmware is programmed.
- ~25k err / 299 FEs for 80 days
  - Oct. 9 to Dec. 27
- Most of SEUs don’t cause DAQ errors.
  - The entier FPGA is monitored.



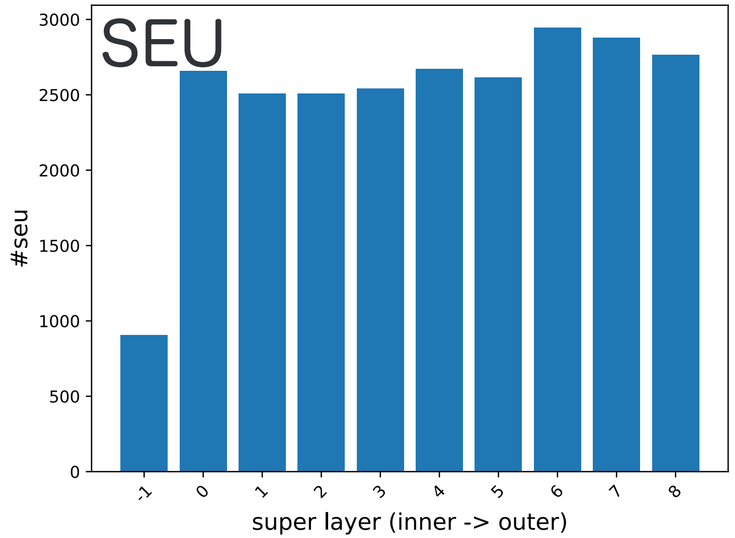
#SEU on CDC FEE in 2024c

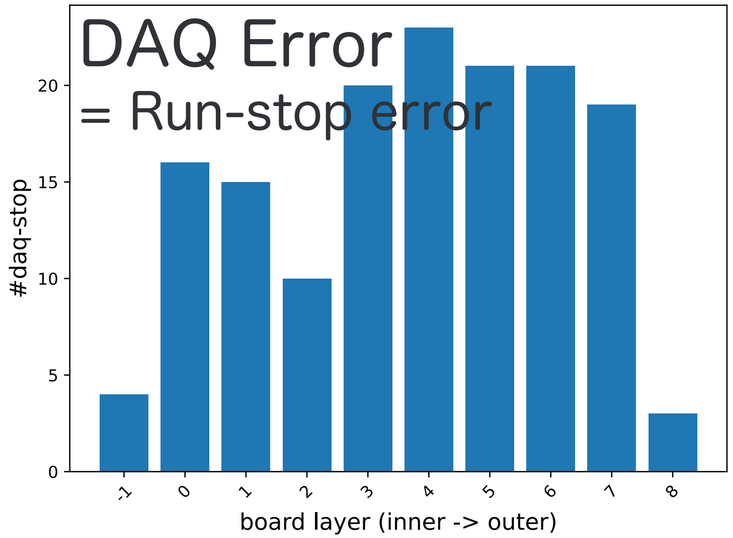
#SEUs per super layer is roughy constant.
-> The neutron background may spread radially from the center.

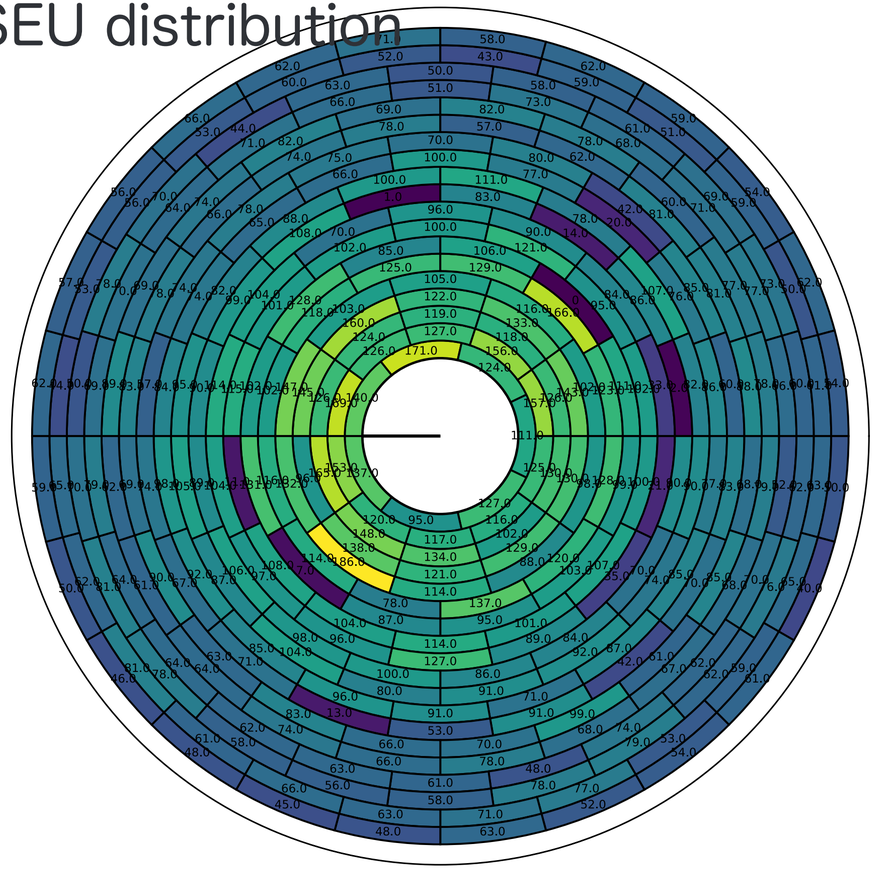
#SEUs per module is higher near the center

The DAQ-error distribution by SL seems to differ from the SEU distribution
-> DAQ errors may not be only due to SEUs. (Power?)

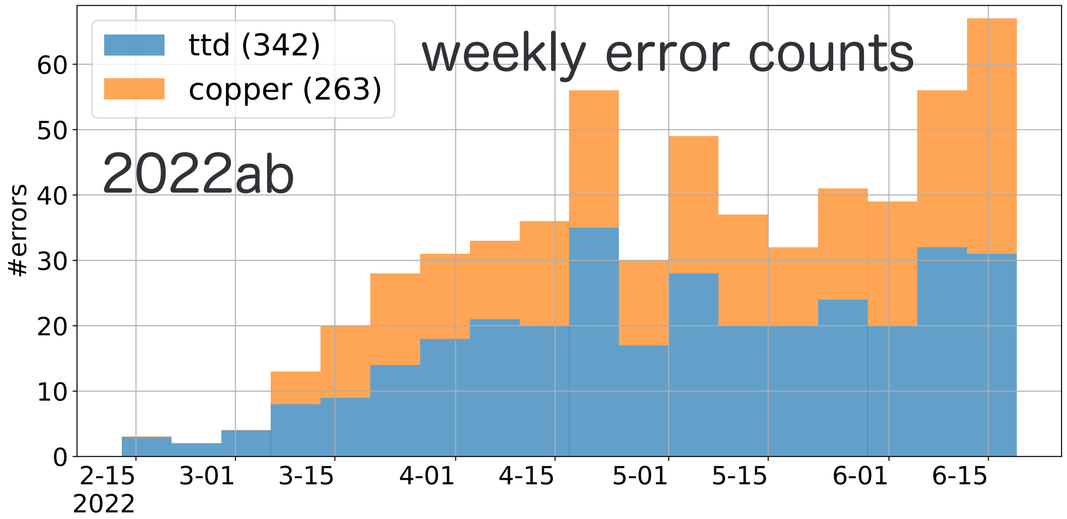
- Certain modules occurs DAQ errors frequently during physics runs.
- This might come from limited statistics.

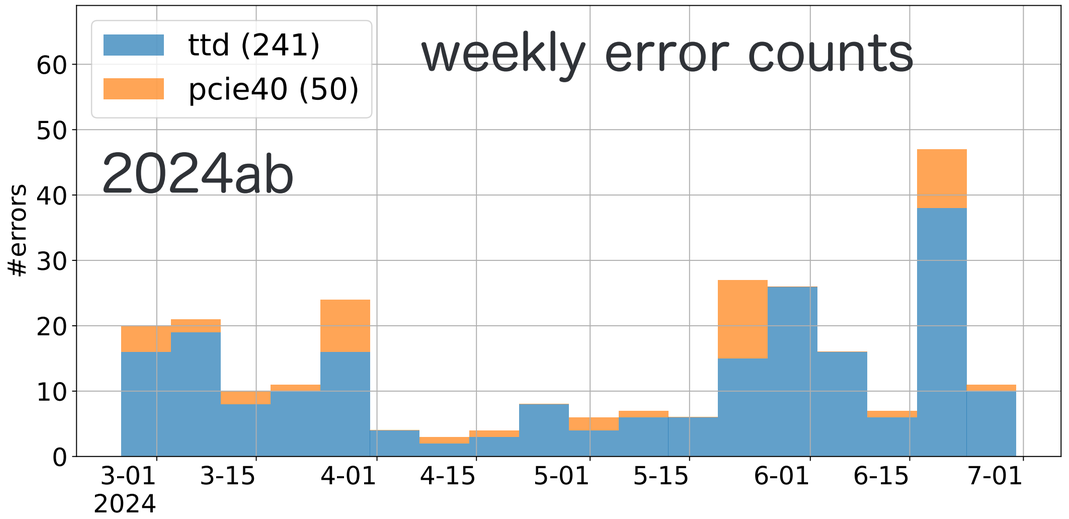






Comparison of DAQ errors before and after LS1





After LS1, the weekly total error count is ~half of before. (Note: run conditions are not considered.)

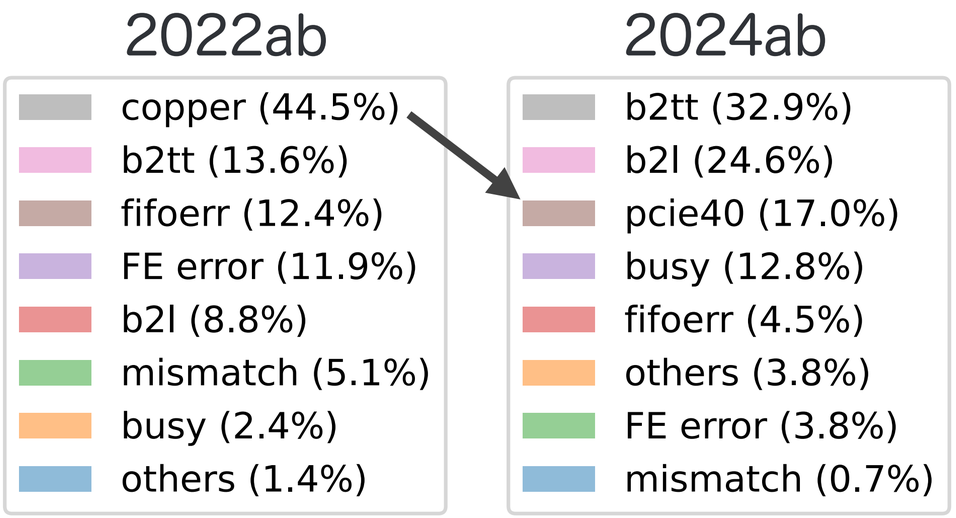
<u>Possible reasons:</u>

Activation of the SEU recovery module

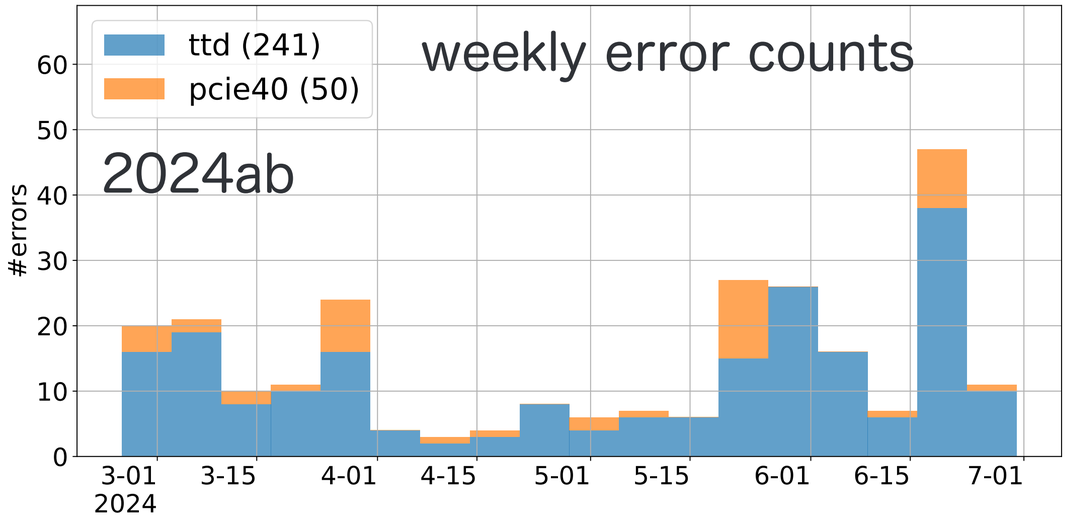
New radiation shield at QCS

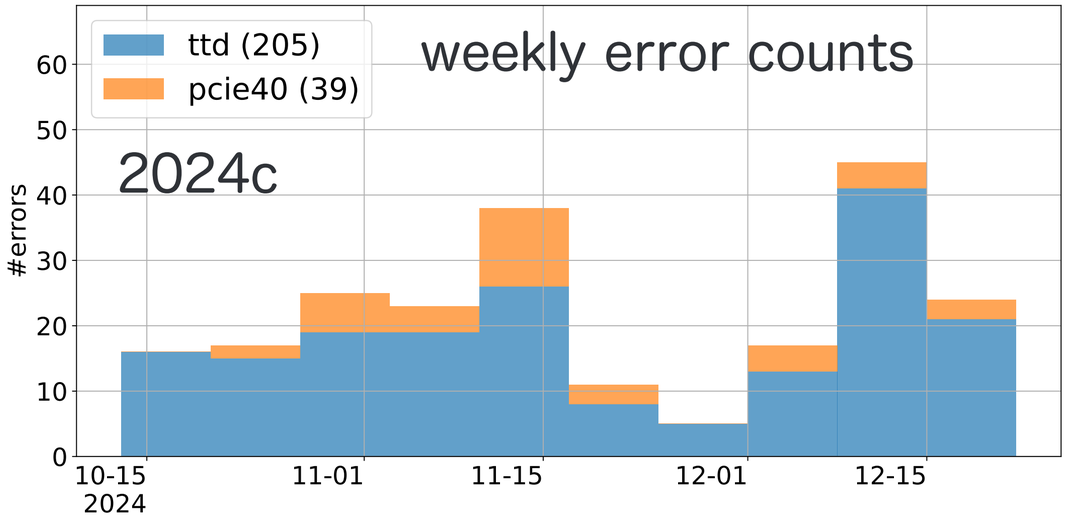
Change from COPPER to PCIe40.

- The reduction is much larger than for TTD.
- In the TTD-related module, error detection is so fast O(10-100us). It flags an error before the SEU recovery module corrects it O(ms).



Comparison of DAQ errors: 2024ab and 2024c

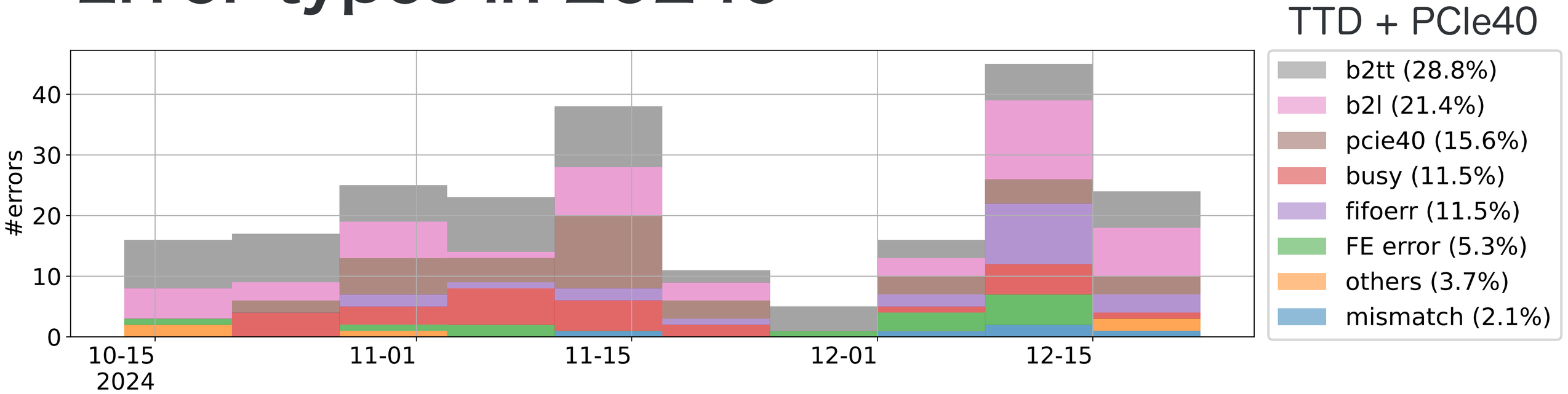




The weekly total error counts are similar between 2024ab and 2024c.

- #errors in 2024c may be slightly higher, likely due to higher beam background.
- The ratios of TTD to PCIe40 is similar too.

Error types in 2024c



Communication-related errors ~ 50%

- Error name: b2ttlost (27%), b2ttdown (1%), b2llost (20%), b2ldown (1%)
- Communication modules use a lot of resources.
- Probably because error detection in the communication modules is too fast.

→ Non-stop DAQ in 2025c may reduce dead time from b2ttlost and b2llost.

PCIe40 errors ~ 15%

- The unpacker module detects corruption in data sent from the FE module.

Idea for DAQ down-time mitigation

similar discussion in TRG-DAQ workshop 2022

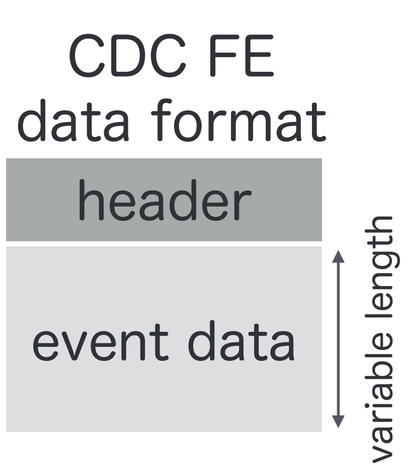
Keep DAQ running after an error is detected on PCIe40.

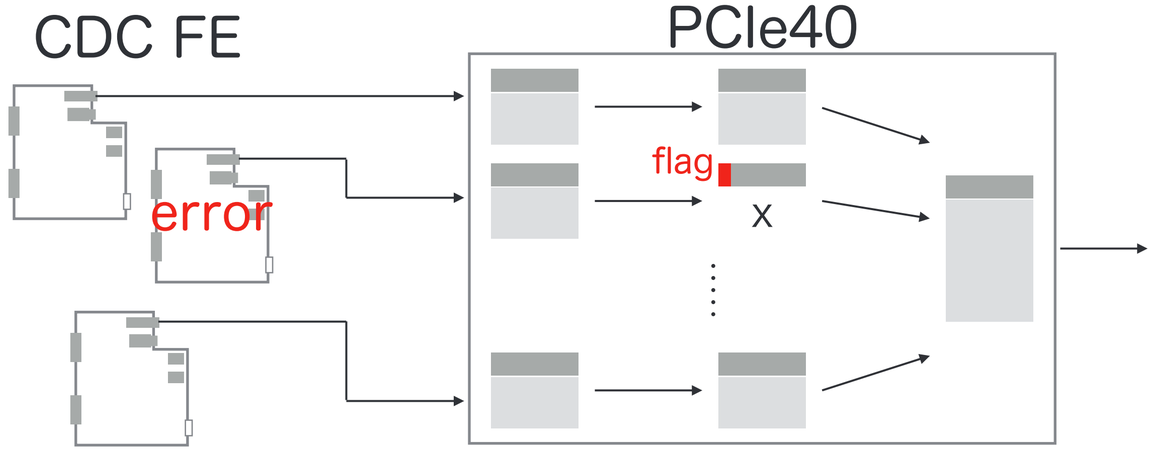
- Re-configure problematic CDC FE modules when we stop DAQ for other reasons
- This is similar to handling unpacker errors
- Matter of concern: soft errors can break the data structure??

PCIe40 removes the event data from a problematic FE module. (online masking scheme)

- PCIe40 processes only the header while adding error/mask flags.
- Yamada-san has already developed and tested (in a test bench?).

We don’t plan to apply it in 2025c, but we may consider operation if the error situation is not good.





Concern about gain degradation

This may affect TRG

Summary

BPAC (2025.03.05)

Large leak current due to high backgrounds leads to significant issues in operation.

- The current blow-up was already observed in early 2024c.
- [Near-term] Risk of Malter effect, and Gain degradation due to leakage current
- [Long-term] Gain degradation due to accumulated charge

We are considering various options depending on understanding of future operational conditions for CDC and improved knowledge of the machine's condition/parameters after LS2:

1. Use of the current CDC
2. Construction of a drift chamber

(3. Construction of a new detector/different technologies??)

Short-term studies towards 2027TDR are important:

- Performance studies in the upcoming operation, such as applying lower HV
- Aging studies using two test chambers at two sites with the current gas mixture and alternative candidates

In future runs, we may need to lower the HV to mitigate the risk of detector damage.

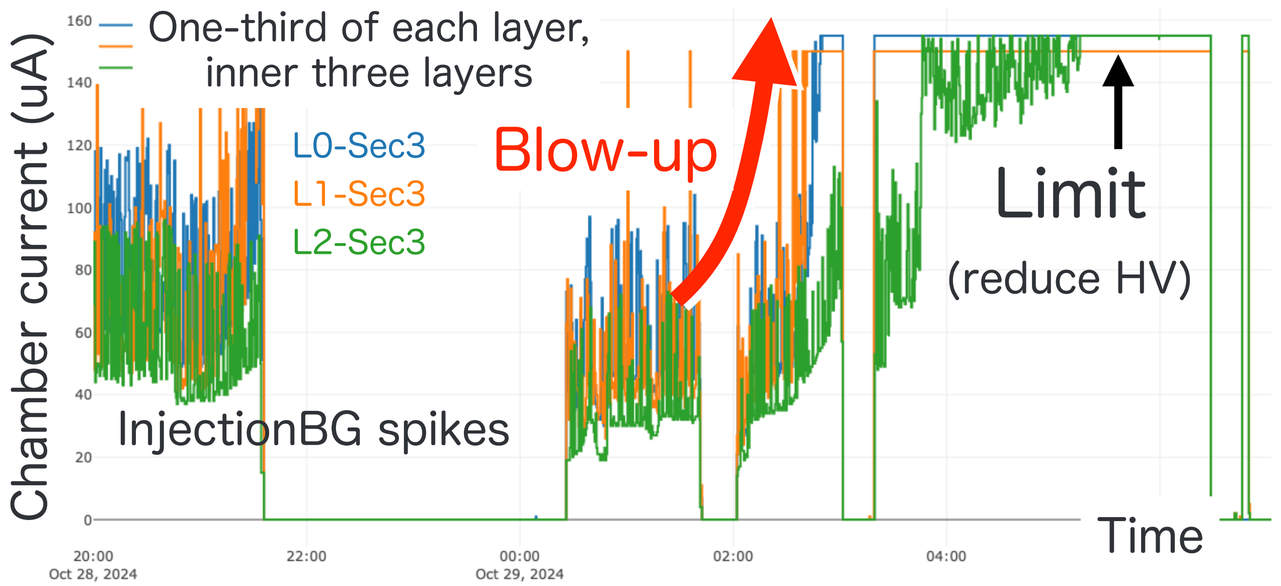
Chamber current blow-up and Countermeasures

Current blow-up at the end of Oct 2024

- Continuous high current poses a risk of detector damage
  - e.g.) Malter effect: Deposits on field wires enhance the local electric field and can cause persistent discharges

Parameters to control to keep the detector healthy

- Gas components (H2O, O2):
  appropriate amounts of H2O or O2 may lower the risk of the Malter effect.
- Chamber current (~ gas gain):
  lower gain to reduce chamber aging



Mitigation and study

- Gas components: update the gas system and reconsider the operating policy
- Chamber current: evaluate performance during 2025c

Performance study with lower HV and threshold

- Lowering the gain helps mitigate the risk of Malter effect and extends the chamber lifetime against wire aging.
- We request special runs during 2025c to evaluate the impact of gain degradation due to lower HV.
  - Maybe at the end of November or early December.

Group name	Necessary total time of runs [hours]	Schedule (select from "during 4/1-6/30", "in July", "any time")	Machine condition (Luminosity, energy etc.)	Purpose of the data	Priority ("high" or "low")
CDC (+Tracking)	8 hours ~ 0.9/fb w/ 100% live time	Early 2025c	~ 3E34	Study for impact of reduced HV (and lower thresholds) for SL0-1	high
CDC (+Tracking)	8 hours	Early 2025c	~ 3E34	Study for impact of reduced HV (and thresholds) for all SLs	high (next to study for SL0-1)

- We would appreciate any feedback from TRG.
  - while we don’t plan to optimize TRG conditions for these runs.

Summary

DAQ errors (run-stop error)

- After LS1, the number of DAQ errors decreased.
- About half of the errors come from communication modules (b2tt, b2l).
- In 2025c, non-stop DAQ is expected to reduce dead time. 🤷

CDC performance study for future operation

- There is concern about permanent damage in extreme beamBG environment.
- One mitigation idea is to run at lower HV to reduce the gain.
- During 2025c, we plan special runs with lower HV to evaluate the impact on performance.
- We would appreciate any feedback from TRG. 🤷