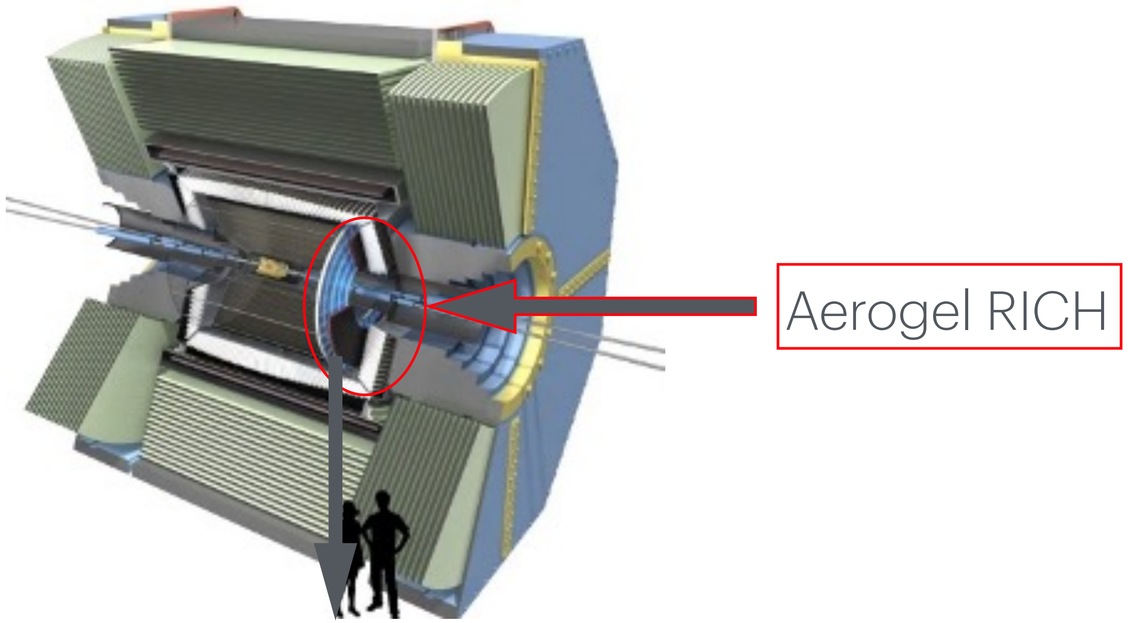
ARICH status and plans

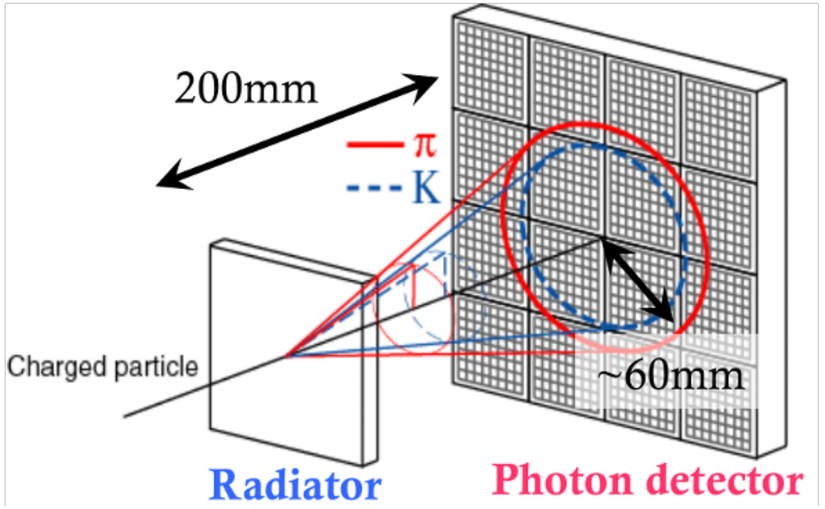
Sourav Dey, KMI, Nagoya

Belle II Trigger/DAQ Workshop 2025, Osaka, 23 October

ARICH @ Belle II

PID detector at the forward endcap





- Target: 4σ K/π separation at 0.5 – 4.0 GeV
- Ring Imaging Cherenkov Counter (RICH) with aerogel radiator
- Replace threshold type Aerogel Cherenkov Counter used in Belle
- Limited space available -> proximity-focusing RICH

Emission angle of the Cherenkov photons

$$\cos\theta_c = \frac{1}{\beta n} = \frac{\sqrt{(m/p)^2 + 1}}{n}$$

Cherenkov angle resolution of a track

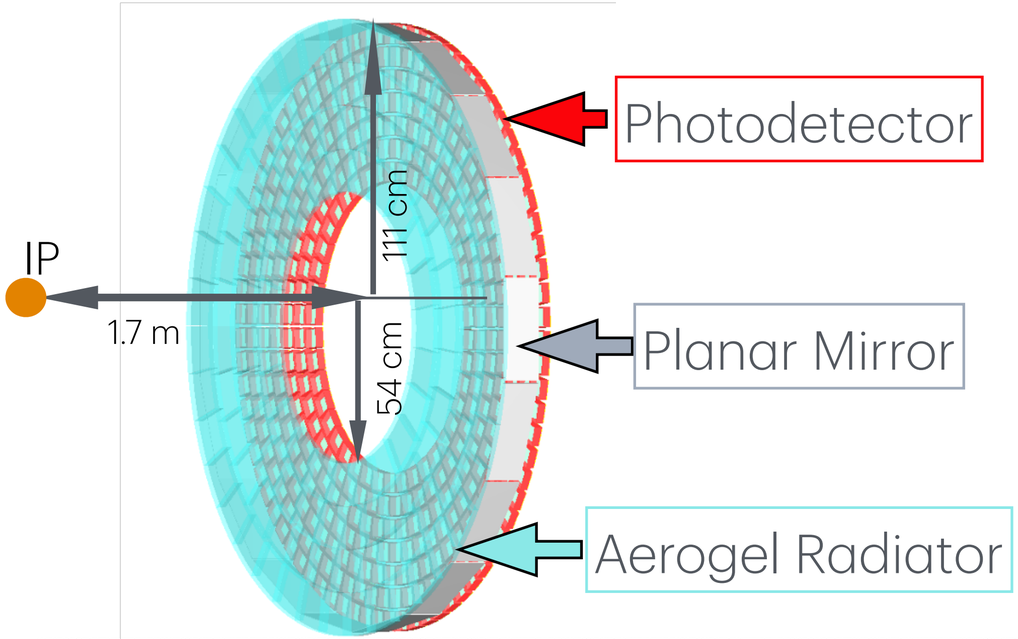
$$\sigma_{\text{track}} = \frac{\sigma_\theta}{\sqrt{N_{p.e.}}}$$

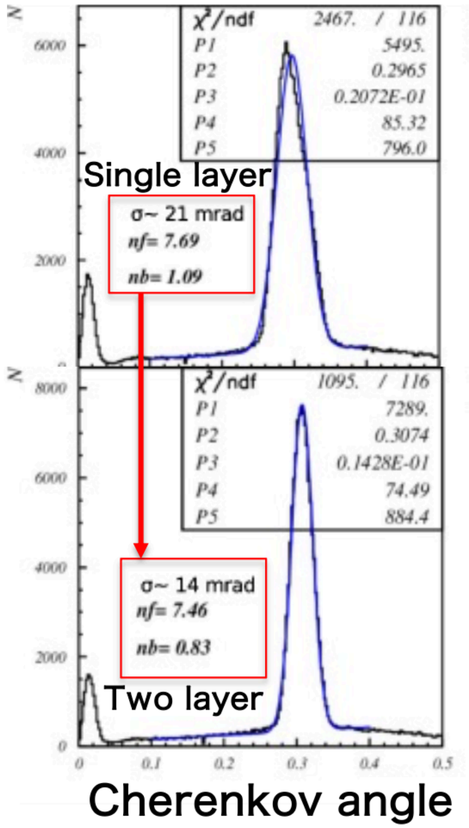
σ_θ = Angle resolution the detector

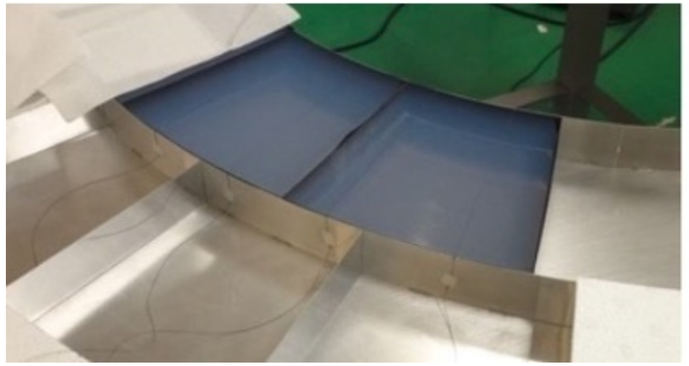
$N_{p.e.}$ = Number of detected photons

Radiator

Two aerogel layers with different indices:
$n_1 = 1.045$, $n_2 = 1.055$

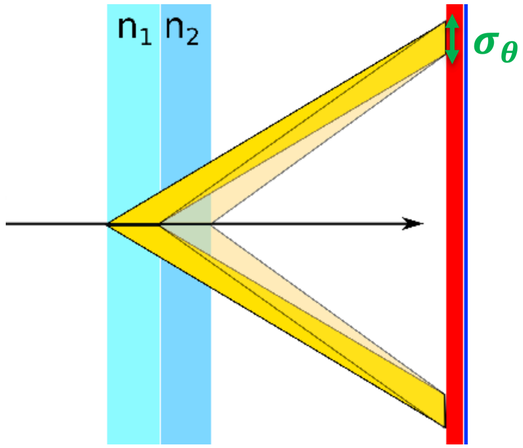






- Thicker aerogels produce more photons but make angle resolution worse.
- Two layers of aerogels with different indices.
  - Ring images overlap at the photo-detector
- Good transparency (~40mm)
  - 248 tiles in total
  - Cut with water jet from 18cm **x** 18cm tiles

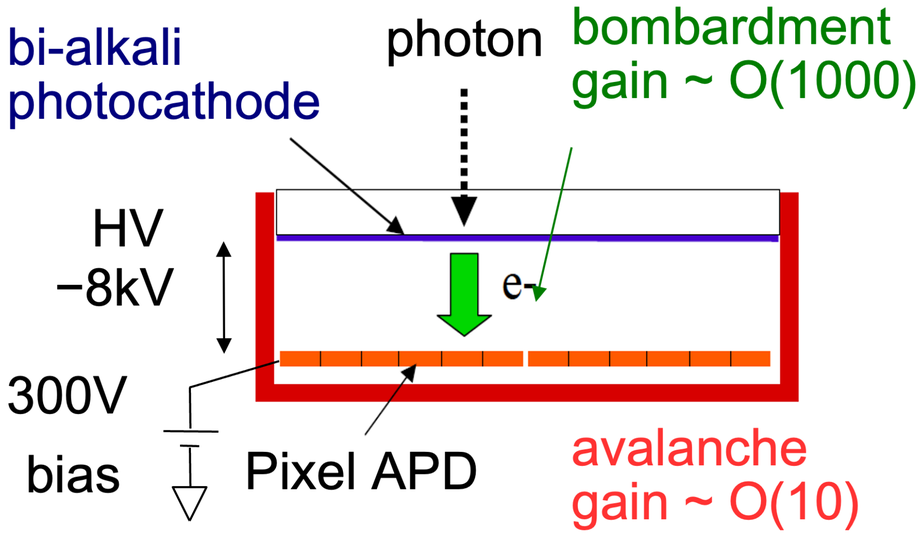
Important to increase $N_{p.e.}$ w/o degrading σ_θ

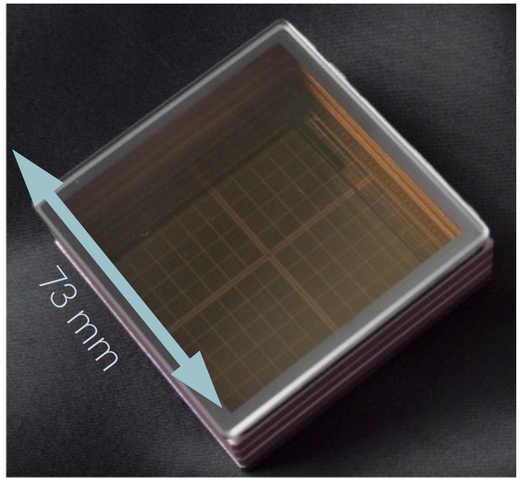


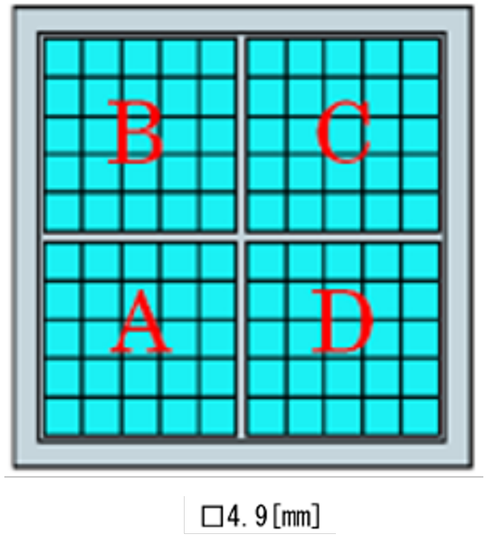
Photodetector

HAPD (Hybrid Avalanche Photo-Detector)
Hybrid: Vacuum tube + semi-conductor

- ~5mm pixel size. Sensitive to single photon
- Large coverage (3 m^2)
- Immune to 1.5T magnetic field
- Radiation tolerance (10^{12} cm^{-2} neutron)
- Good single photon detection efficiency

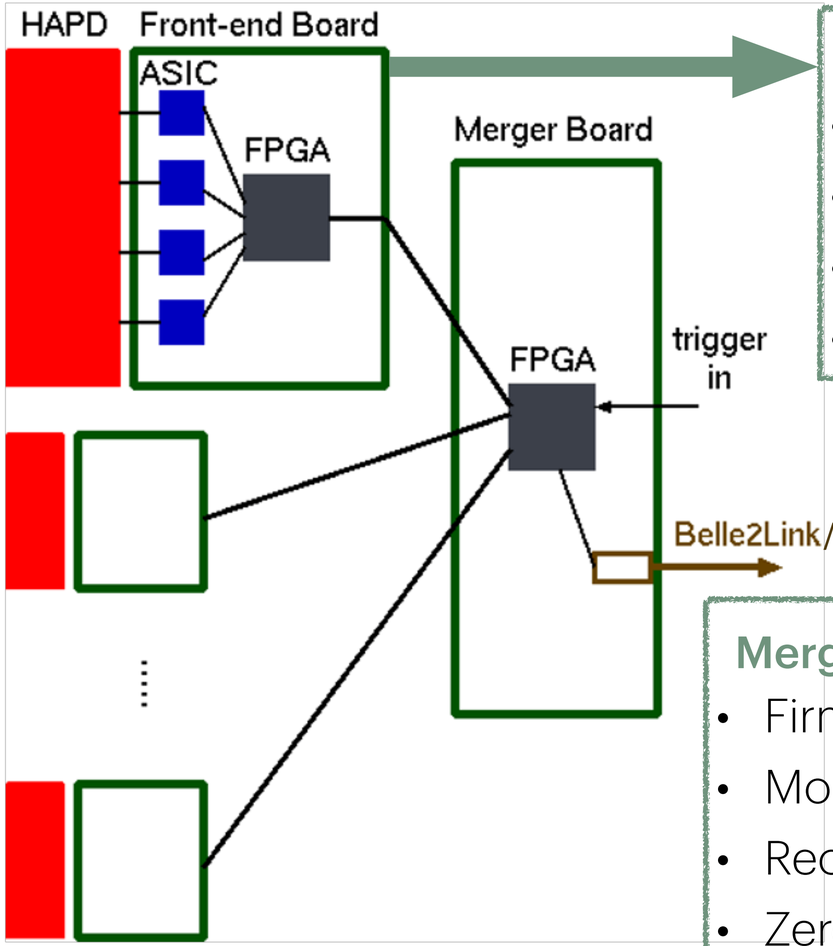






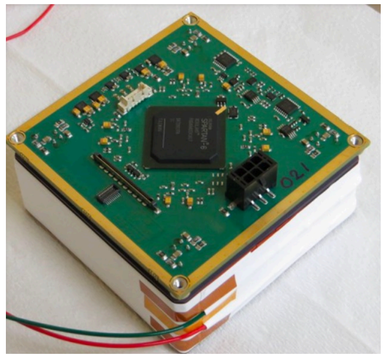
- Developed with Hamamatsu Photonics.
- 144 channels (36-ch APD chip×4)
- Gain ~ 70000
- Peak QE ~28%
- Size 73mm×73mm
- Effective area 63mm×63mm (65%)

Readout electronics



Front-end Board

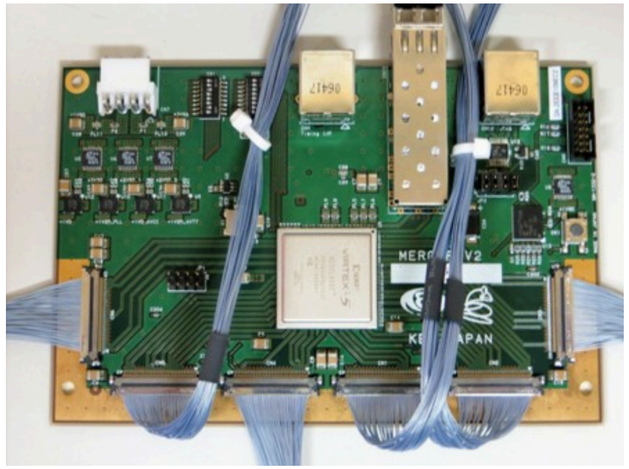
- Digitize signals from HAPD
- 4 ASIC + Xilinx FPGA (Spartan6)
- ASIC : preamp + shaper + discriminator
- 420 FEBs in total



Total 60480 channels
1-bit ON/OFF information is enough

Merger Board

- Firmware download, parameter setting
- Monitor temperature, voltage, SEU etc
- Receive hitdata from 5-6 front-end boards.
- Zero suppression
- Combine FEB data and send to DAQ
- 72 merger boards in total

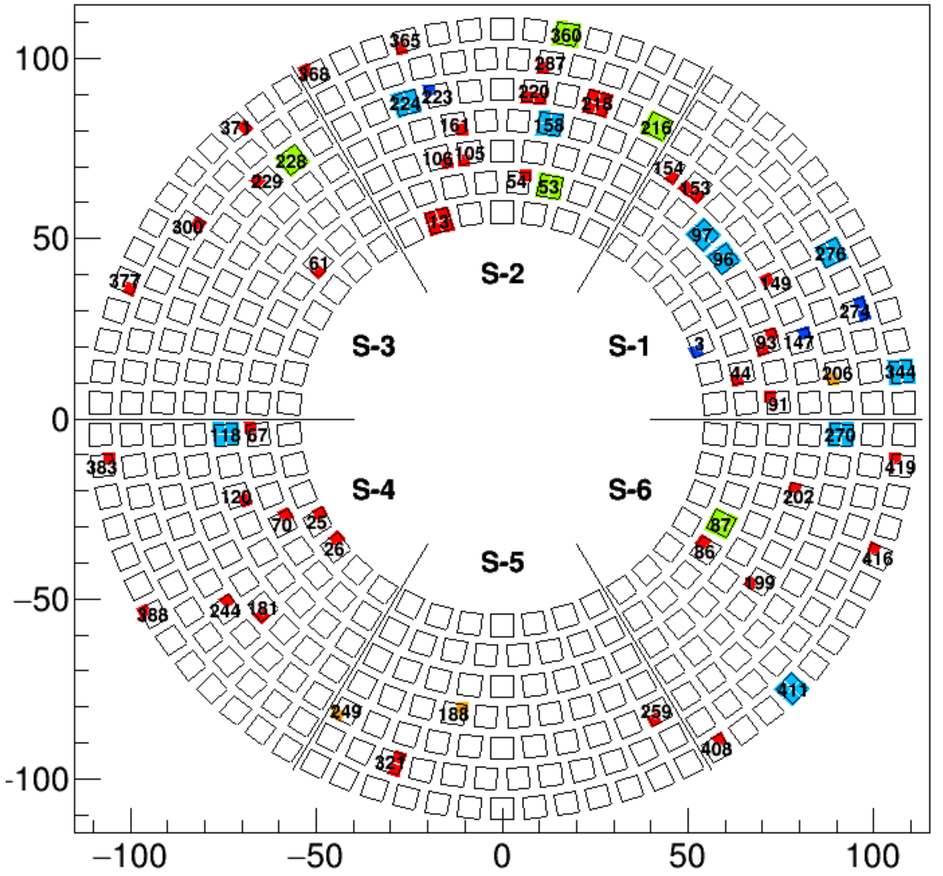


ARICH APD Status

- ARICH APDs are stable, no major problems
- The masked channels due to turn off HAPDs are basically same (~ 6.7%)
  - Disabled bias: 56
  - Disabled guard: 5
  - Disabled hv: 9
  - Total number of masked APDs: 112

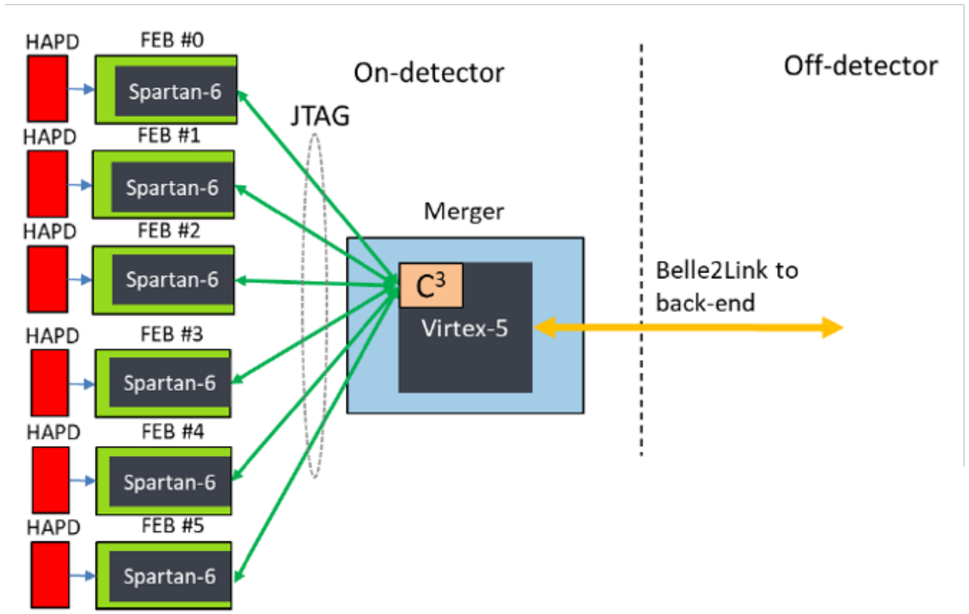
	2019	2020	2021	2022	2023	2024
Ratio	4.8%	5.6%	6.0%	6.5%	5.4%	6.6%

Red: disabled APDs due to bias problem
Blue: disabled APDs due to guard problem
Green: disabled APDs due to HV problem
Orange: set voltage of these APDs to 175V



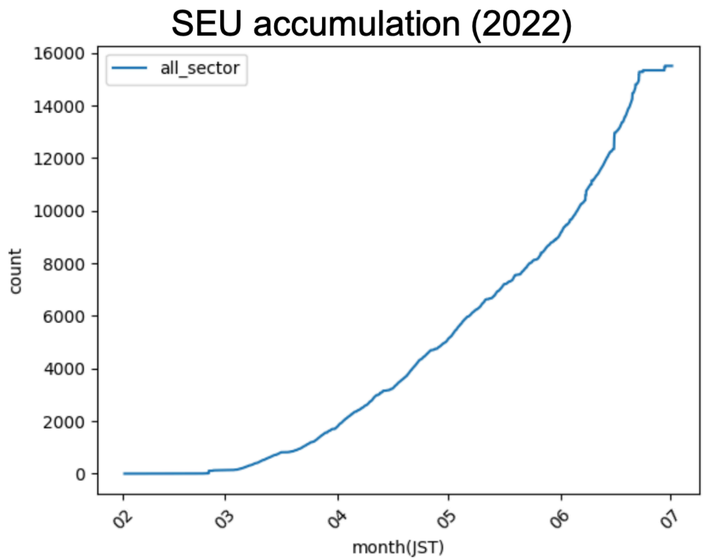
SEU in the Front-end

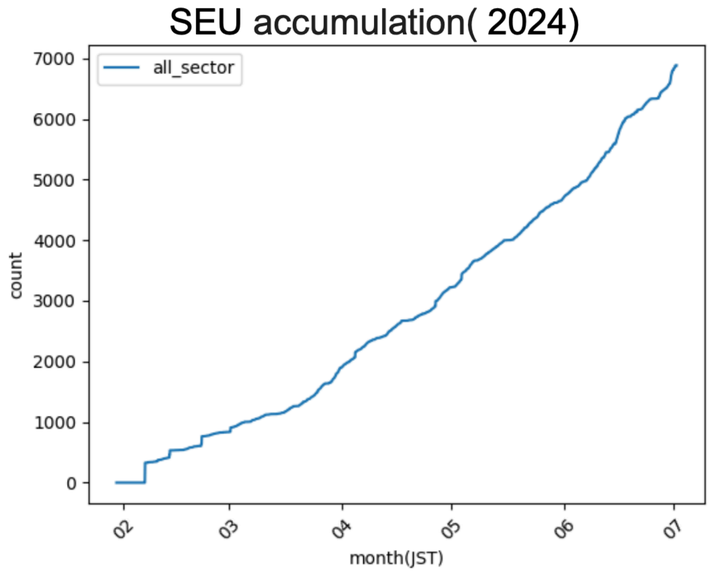
Single Event Upset in the FPGAs : effect from neutrons



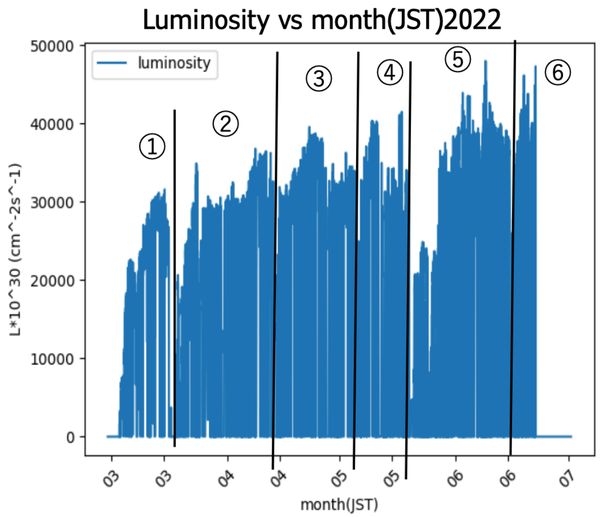
- Frequent SEUs expected at Spartan 6
  - Boron is used as p-type dopant
  - old estimation: 8 SEUs / h / HAPD in the firmware
- Configuration consistency corrector (C3) is implemented in the merger firmware since June 2020: DAQ efficiency improved!

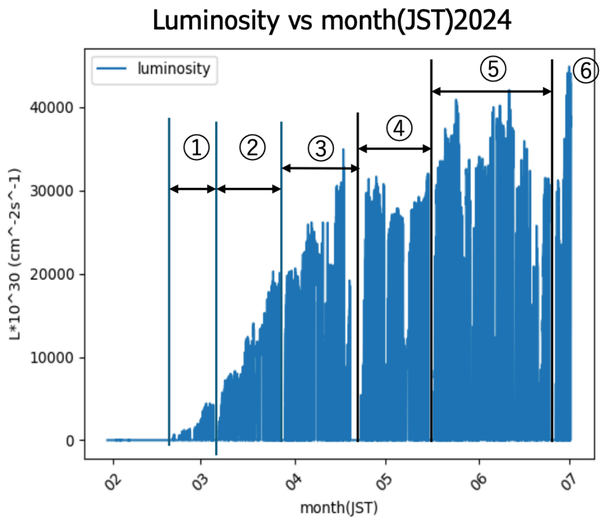
Real-time majority voting + partial reconfiguration of the firmware

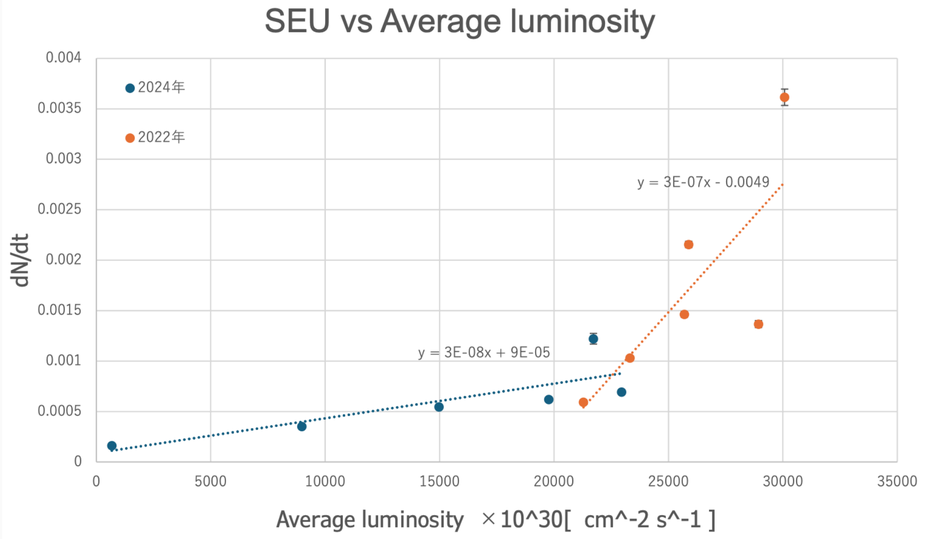


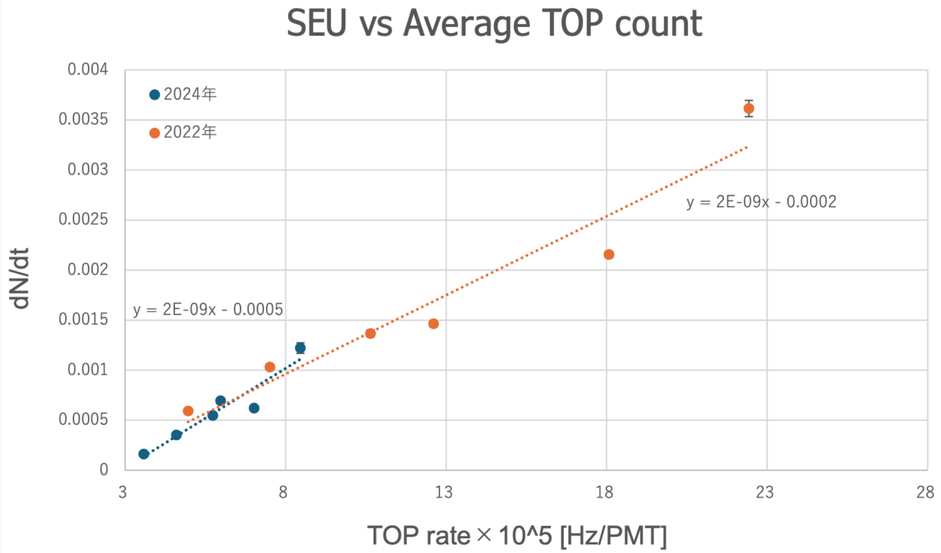


More on SEU





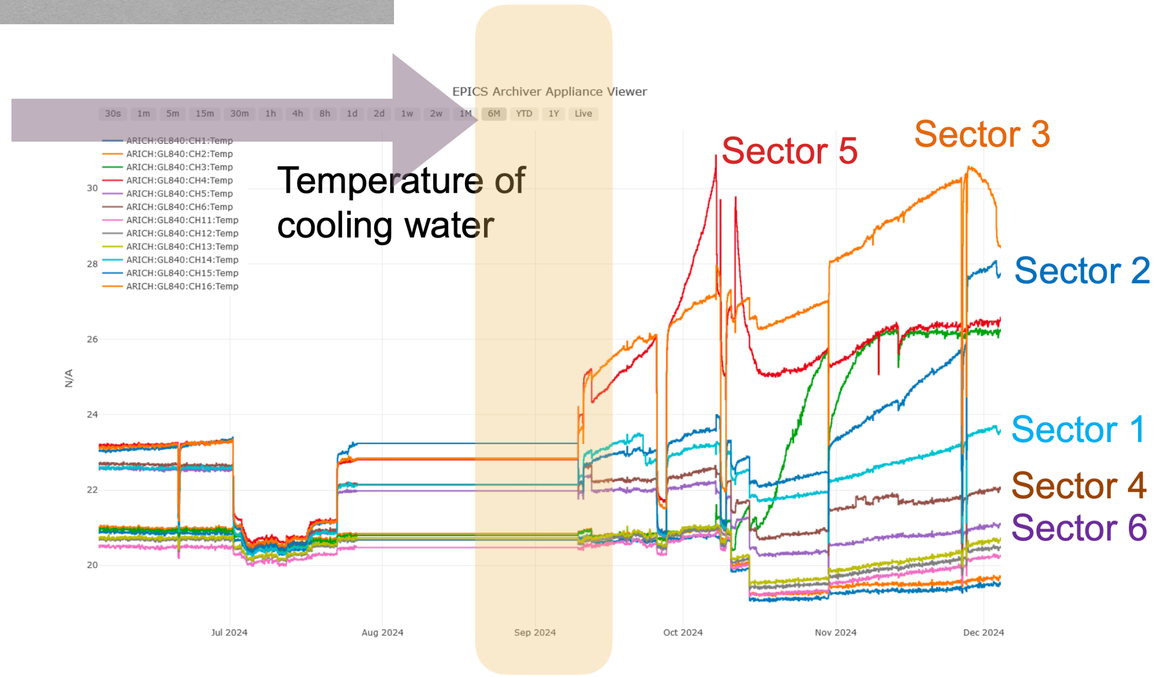


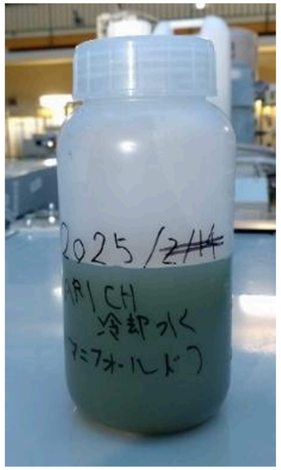


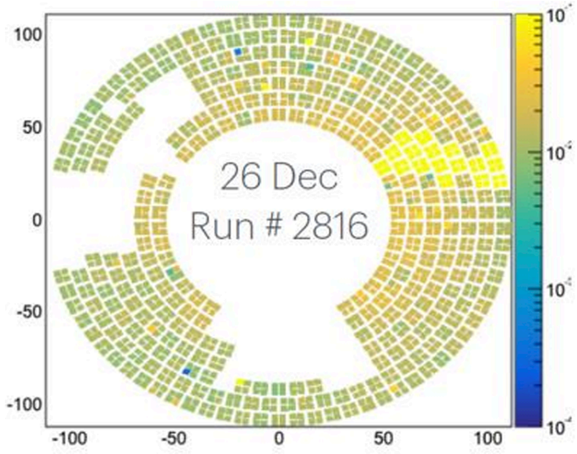
- operating periods: determined based on luminosity graph. vertical axis represents peak luminosity
- A clear correlation was observed between TOP MCP PMT rate and SEU. The TOP rate is considered to be directly related, whereas luminosity, HER, and LER currents may have an indirect correlation
- Regarding spatial distribution, the overall values decreased. In 2024, the events were primarily concentrated in Sector 1. However, whether this shift toward Sector 4 was influenced by the shielding effect requires further investigation

ARICH cooling water problem

- ARICH suffered a problem of decrease of the cooling water flow in 2024c run
- The flow was significantly reduced in Sector 3 and 5, and we needed to turn off ~50% of the electronics in these sectors (10-20% of the entire ARICH).
- The replacement of the chiller and the addition of anticorrosion agent were considered to be source of the problem.
  - Aluminum pipe inside ARICH + installed chiller included copper components : Mixture of copper and aluminum in the system
- After 2024c , we opened the pipe near the detector, found green muddy impurities : probable source of clogging. Forward end yoke was opened in June to access ARICH pipes for investigation.

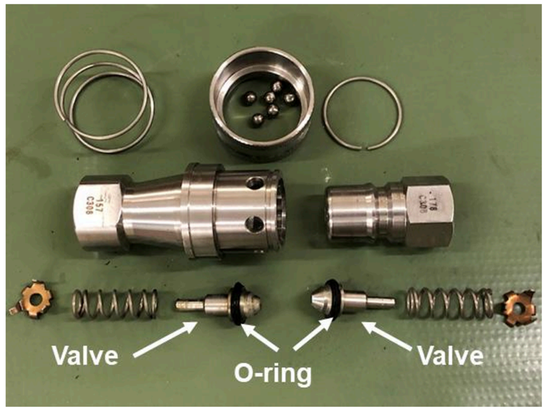






ARICH cooling water problem

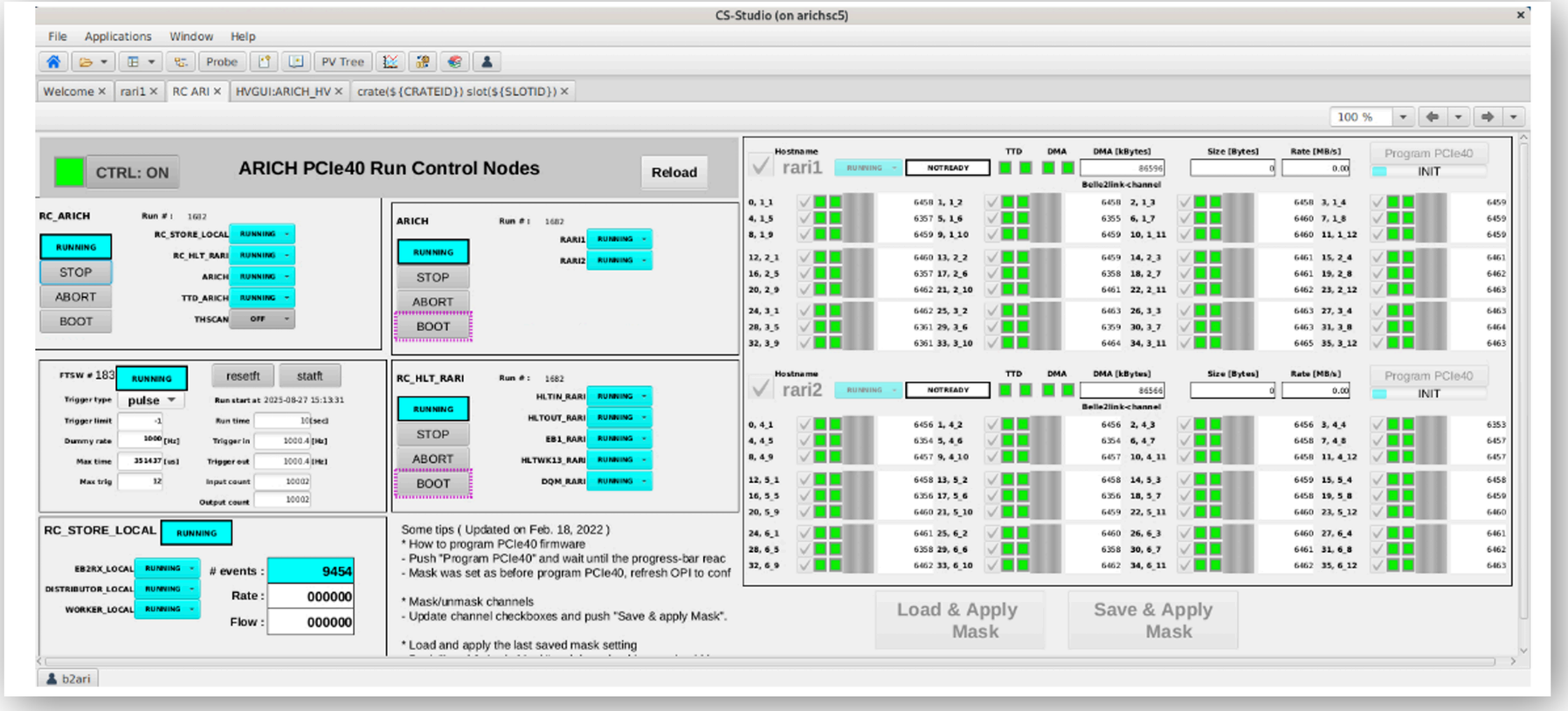
- We found that the couplers were clogged
  - Swell of the O-ring (made of chloroprene rubber) : Probably due to the anti-corrosion agent ?
  - No problem in Aluminum pipes inside ARICH or flexible tubes
- Solution:
  - Remove the couplers
  - Replace the FEP tubes to nylon tubes
  - Replace the chiller to a copper-less one
  - Add filter to the waterline
- We resumed the commissioning of ARICH from middle August. Water flow is normal (6L/min) after removing the couplers. Temperature is stable (detector, electronics).



ARICH is fully working now

ARICH DAQ Status

- ARICH DAQ is fully functional, All the mergers are ON now



Recent problems

One LV board got broken for the first time. Currently no spare module

Two HAPDs got problematic (HV, noisy)

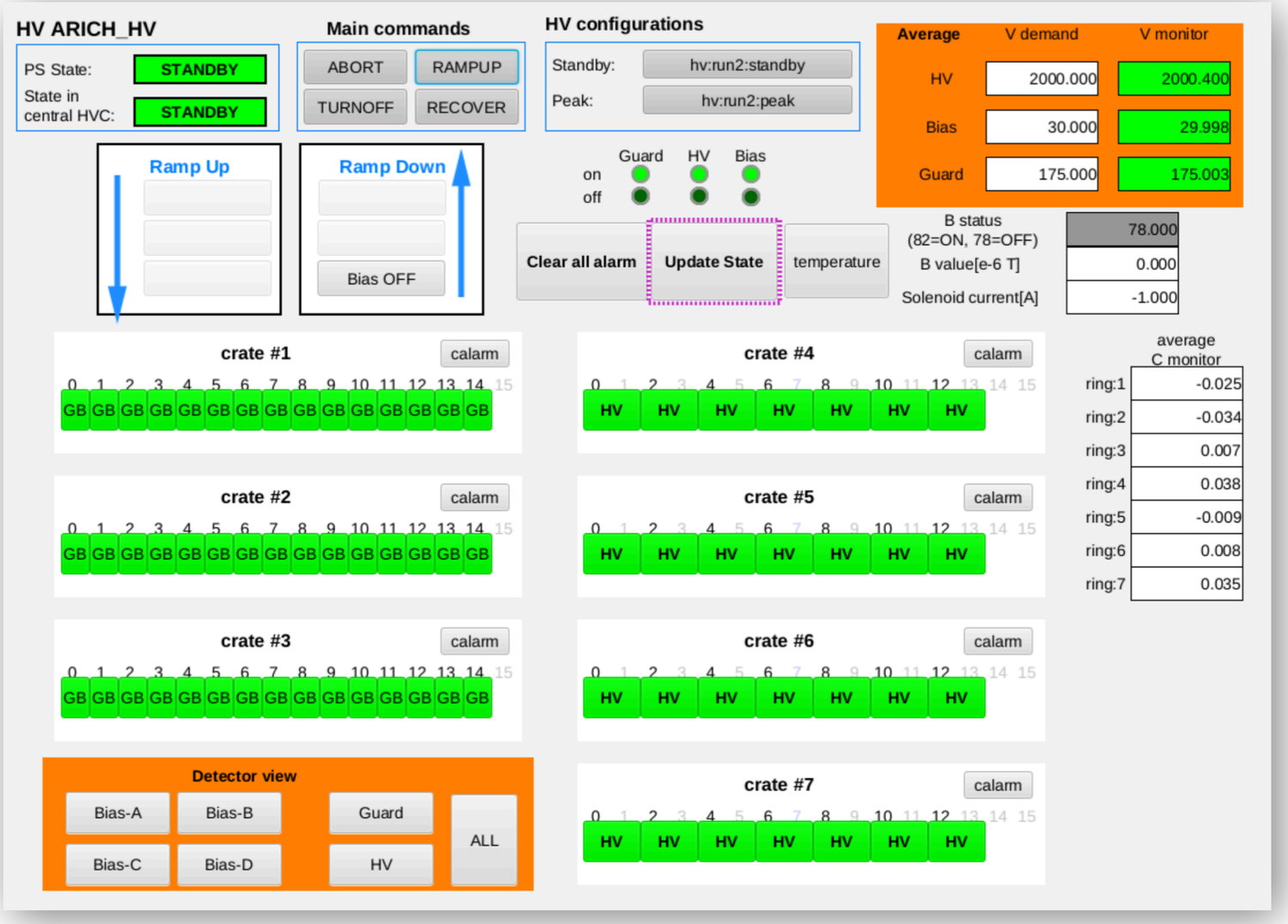
ARICH DAQ Status

Some Updates

- Hardware patches to FTSWs were applied : improves the stability of FTSW initialization during cold start
- Conversion of GUI from CSS to Phoebus is finished: local DAQ panel, HV panel, LV panel
- Update of HV control software
- Update of servers (CentOS7 to Rocky9)

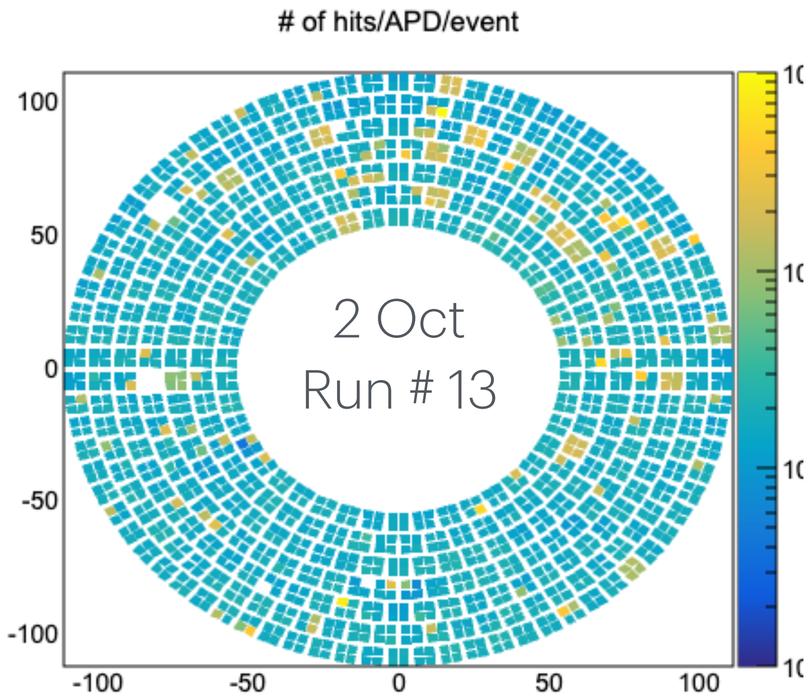
Readiness

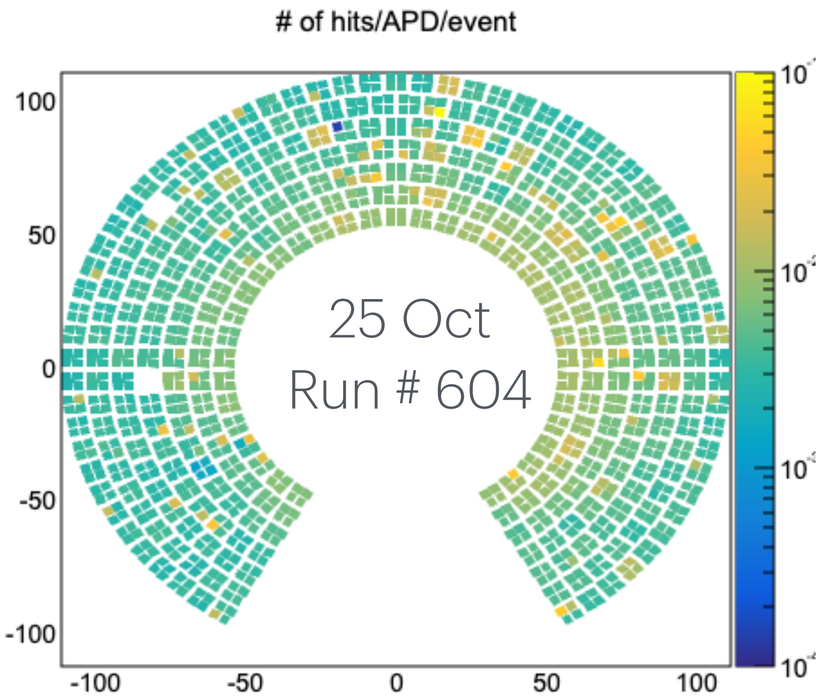
- We are having a training to ARICH experts
- Need more local experts
- ARICH is basically READY

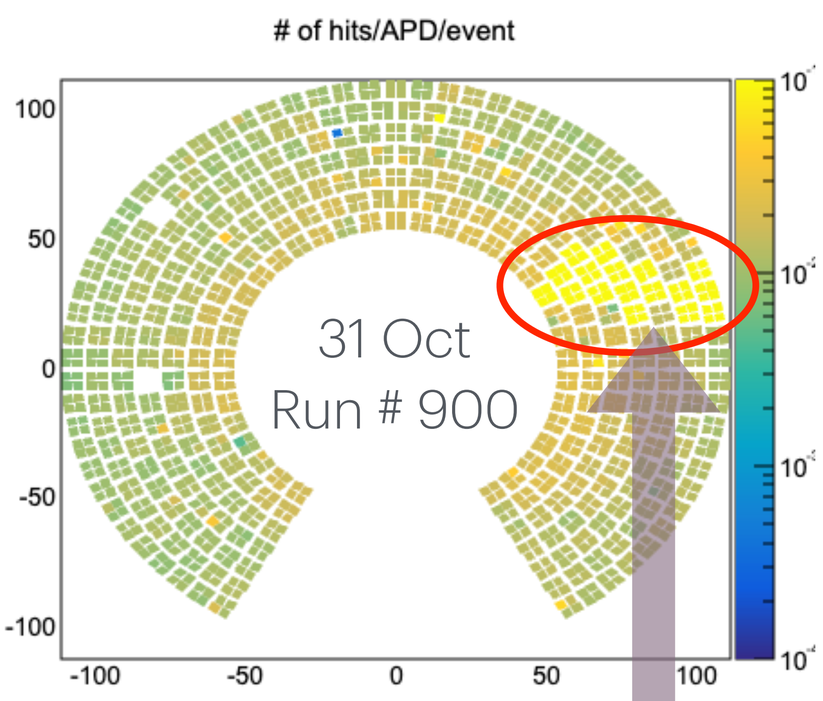


2024c Operation: α noise

How condition of ARICH changed…





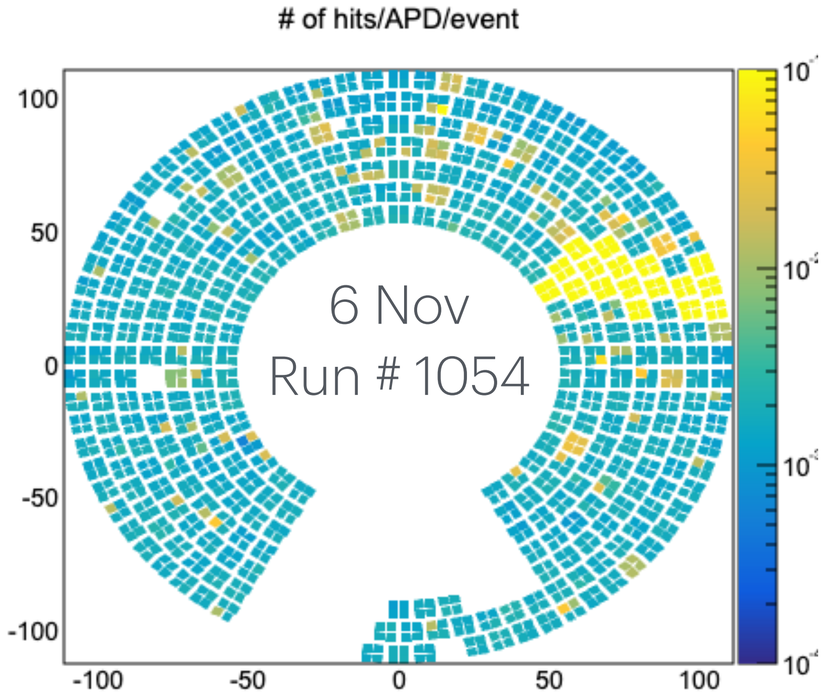


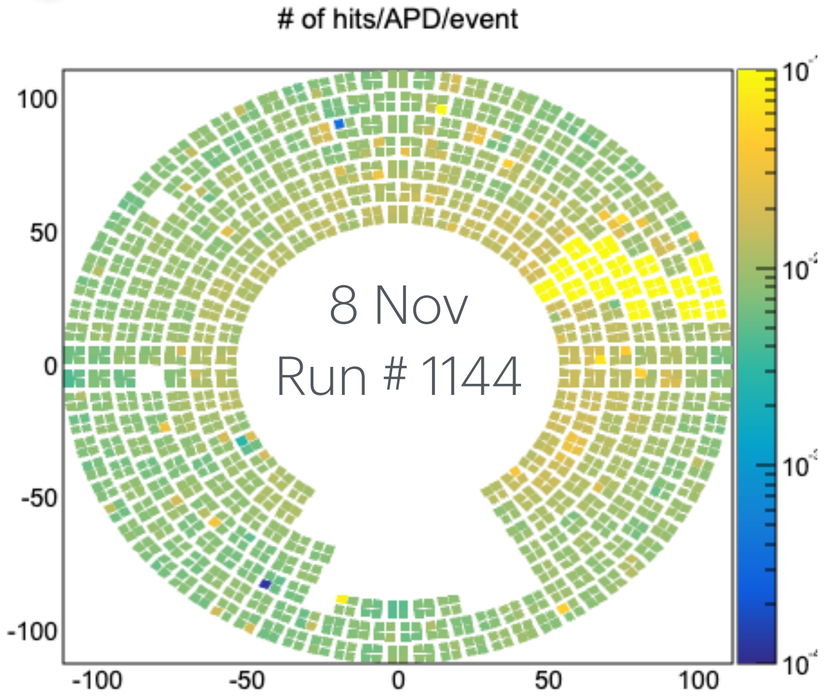
Beginning of 2024c

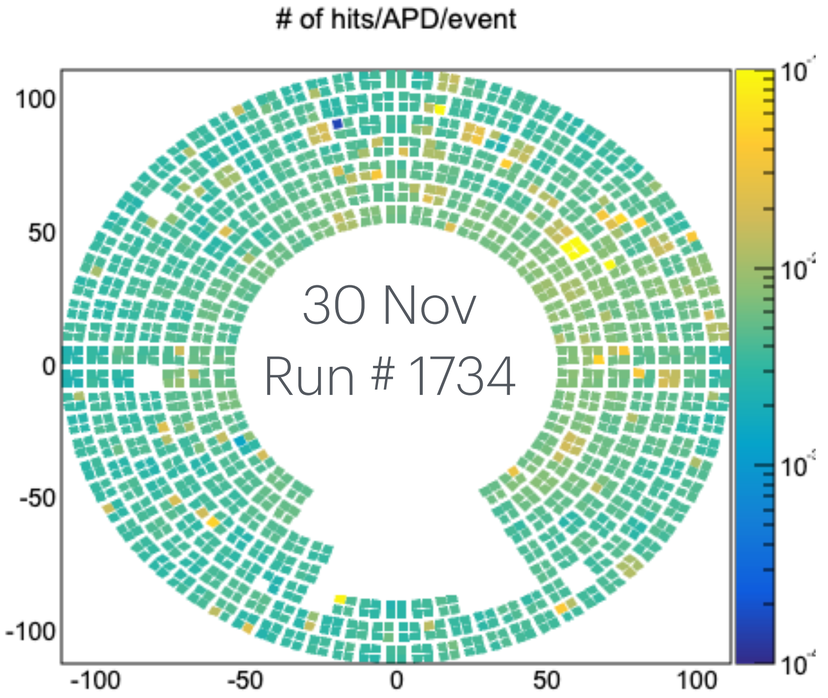
Noise appeared

2024c Operation: α noise

How condition of ARICH changed…





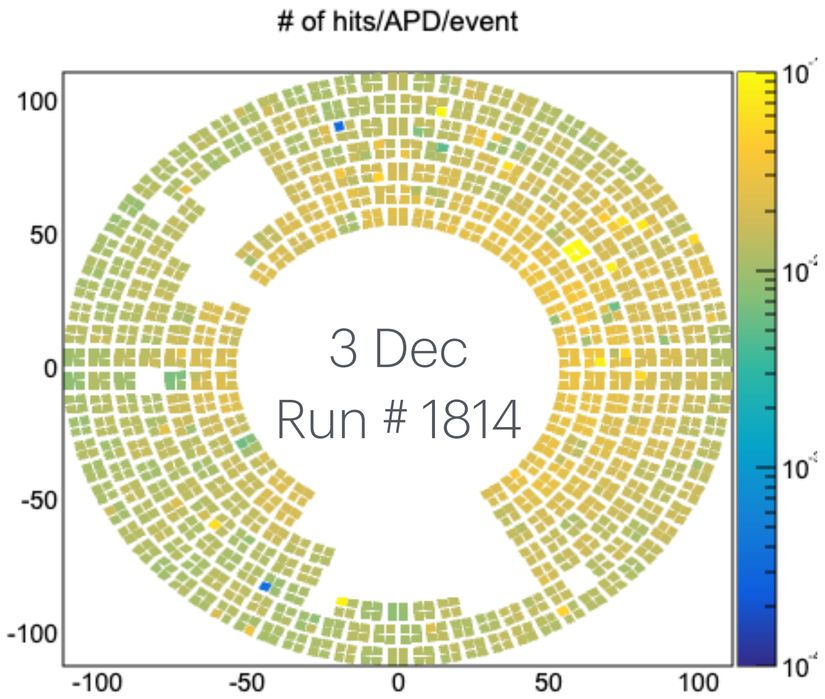


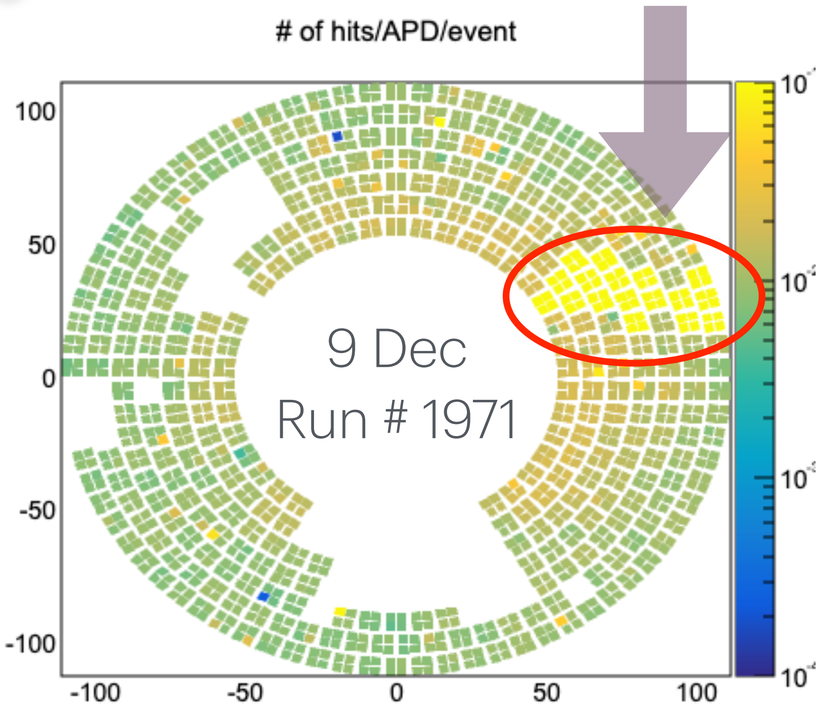
Noise disappeared

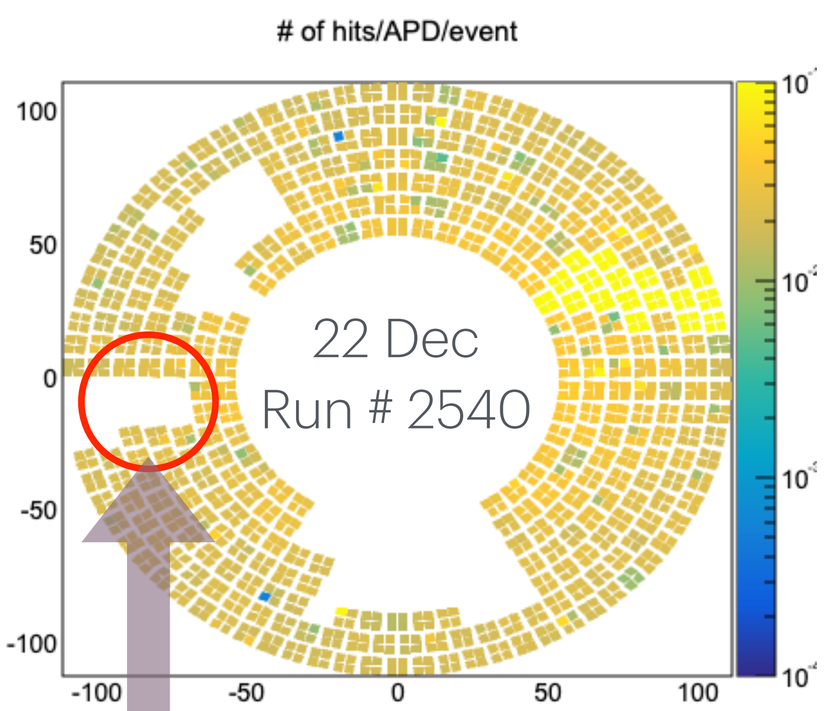
2024c Operation: α noise

How condition of ARICH changed…

Noise reappeared



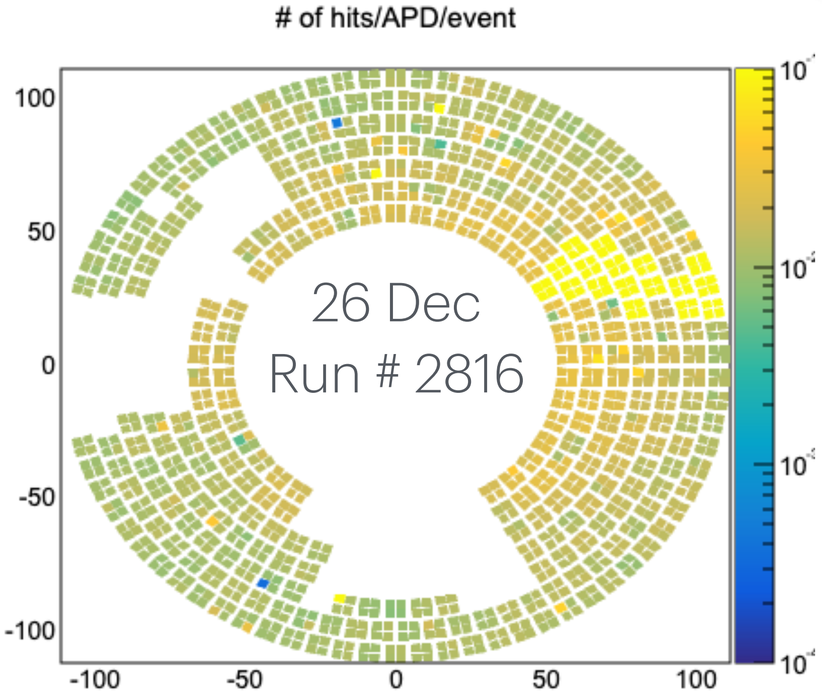


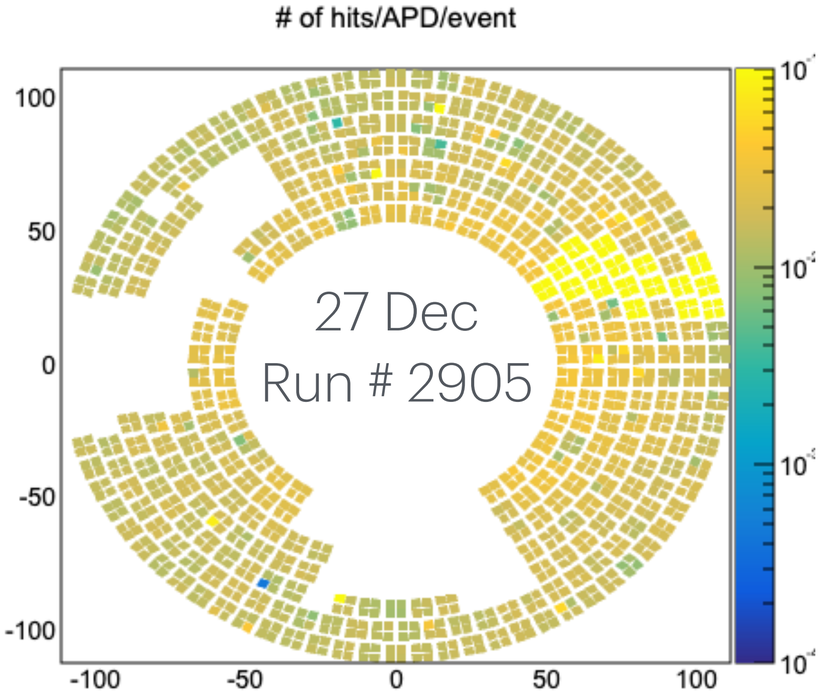


merger 4_4 was disabled due to DAQ problem

2024c Operation: α noise

How condition of ARICH changed...





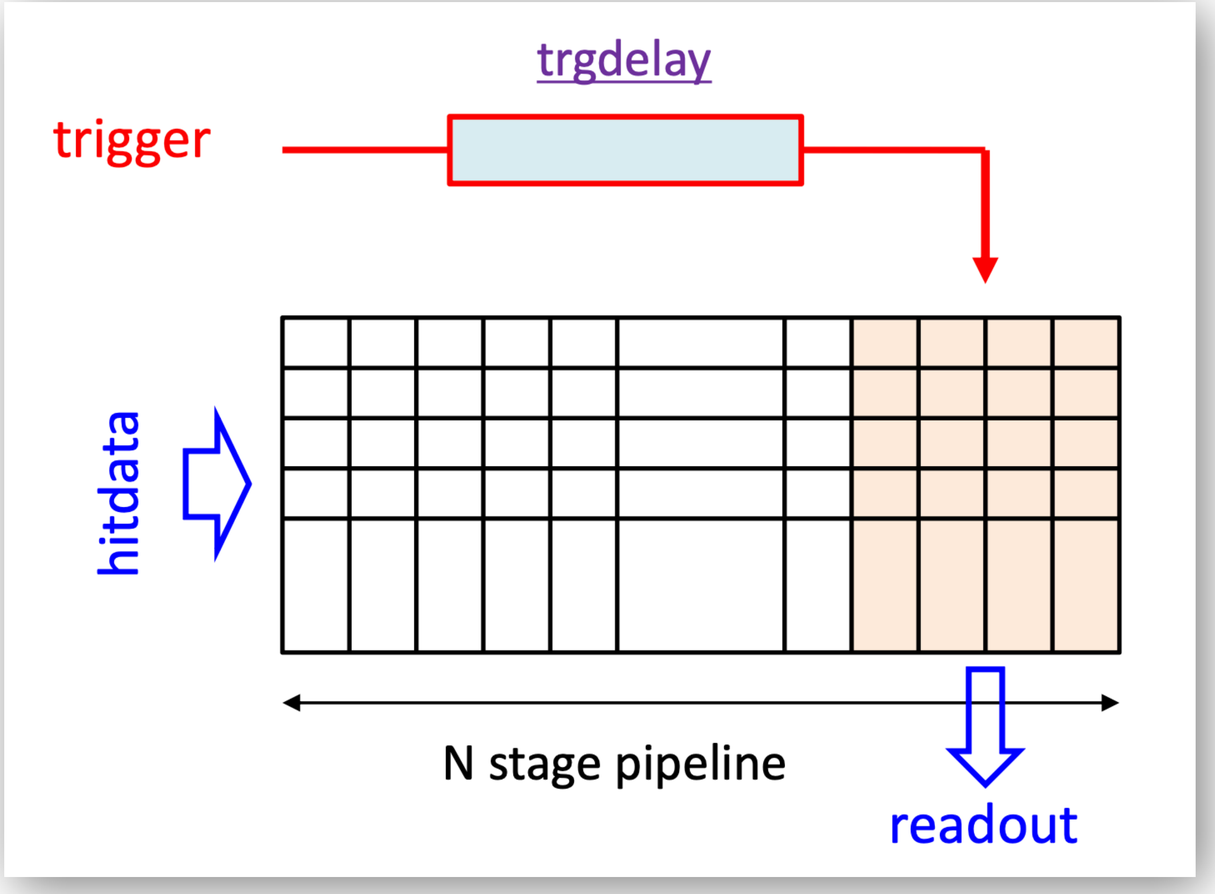
End of 2024c

Long-standing Sector 1 noise is not seen now. Not understood

noise in sector 1 has negligible impact on performance

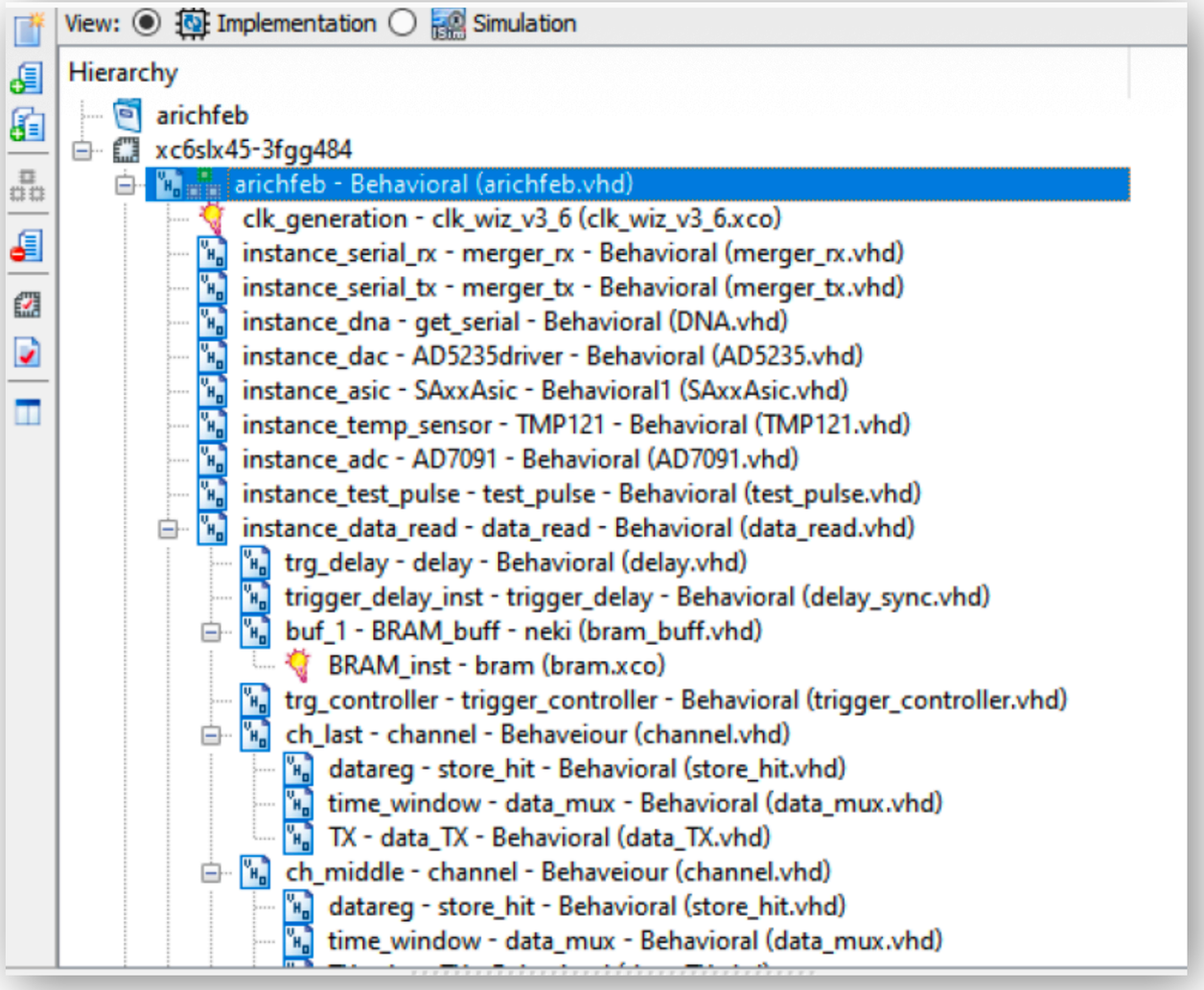
FEB timings

- System clock : 63.5 MHz (508 MHz / 8), i.e. 1 clock = 15.7 ns
- The data inside pipeline is shifted every hdcycle clocks
- The pipeline has N stage, where N = 8 (up to v0.7), 24 (v0.8), 56 (v0.9-)
- The trigger signal is also delayed by trgdelay * hdcycle system clocks
- The last 4 stages of the pipeline are read out, on each trigger delayed
- Larger trgdelay results in time window in a future side
- Hitdata is kept for around (N – 2 – trgdelay) * hdcycle * 15.7 ns.



FEB timings

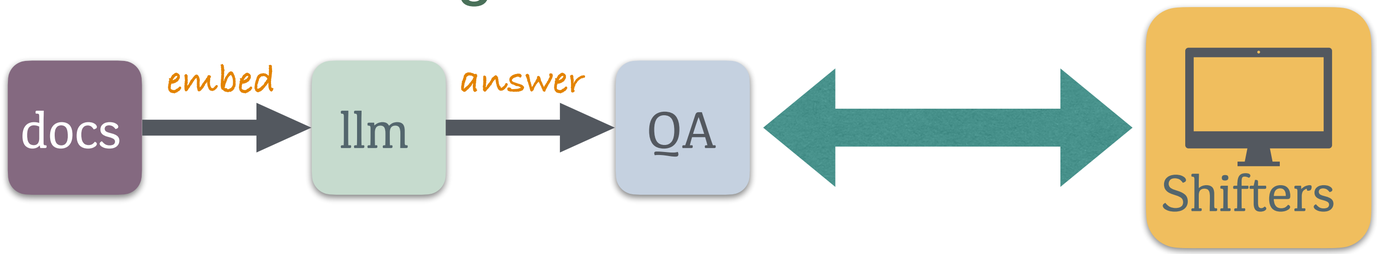
- Additional delay with BRAM
  - Hits are first stored in BRAM circular buffer with independent read and write
  - After selectable number of clock cycles hits are inserted in current pipeline
  - Pipeline can bi extended for ~ 15k cycles, possibly more
- BRAM configuration:
  - Native
  - Simple dual port RAM
  - Common clock
  - No ECC
  - Width 144 bit
  - Length 14799



ARICHbot : A proposed AI Assistant

Objective:

- Assist ARICH shifters during runs with a RAG (retrieval augmented generation) based tool
- Real-time ARICH query support during runs
- Boosts shifter efficiency: reduce manual error, gives suitable advice , especially in crucial times
- A lot of technical/Physics knowledge are hidden in mattermost chats, internal presentations
  - **Will serve as an interactive knowledge base for the future**



Highly likely that this plan will evolve

INPUTS:

- BELLE II Technical Design Report, Belle II Physics Book
- Chat dumps from mattermost, old rocket chat dumps (probably)
- Different presentations, manuals
- Scrap/dump of Xwiki page of ARICH

Public docs

Internal, private docs

Security:

- Full Safety: Local training, zero data leakage
- No link to cloud: the whole process could be air-gapped if requested / necessary
- Members of ARICH should understand agree about the security policy

Progress:

- A functional framework with RAG pipeline is established, with TDR only. Mistral-7B model is used. Will also explore llama3 model later
- First version of the code is available here: `https://github.com/souravampire/ARICHbot`
- We are testing the performance:
  - Occasional hallucination problem, optimizing : pdf vs text
- For the public documents, we better do a fine tuning
- A robust plan will be to fine-tune with published docs, and then use RAG for internal docs
- Also, optimizing vector-database choice: chromaBD, pinecone

Plan:

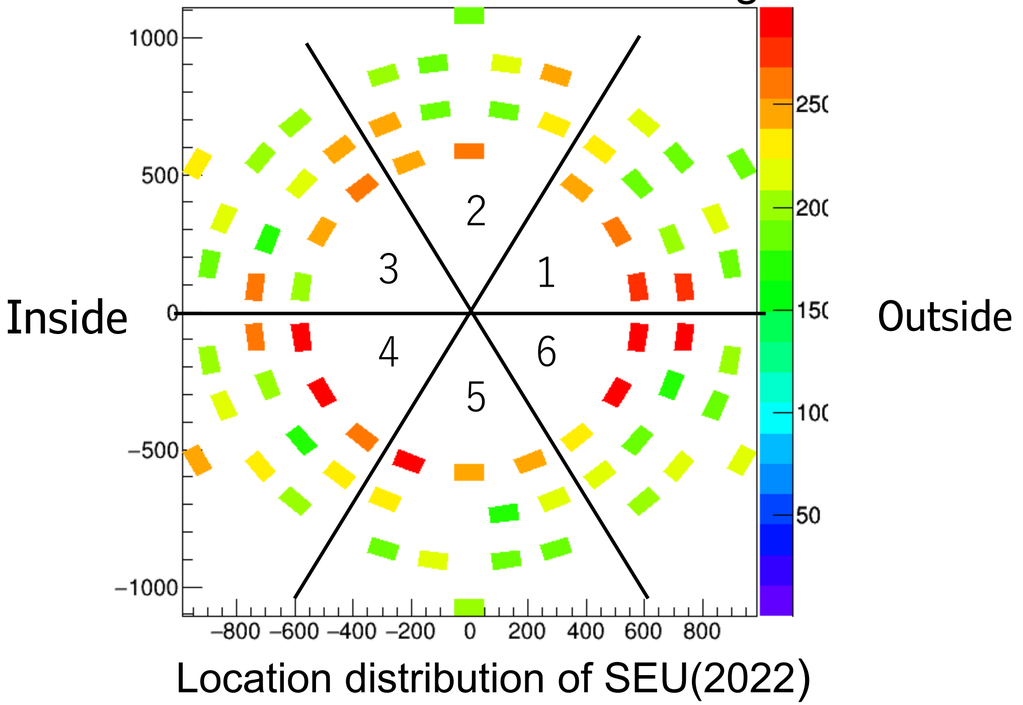
- Future: Expand to other sub-detectors
- Linux/macOS compatibility

Thank you for your attention

Backups

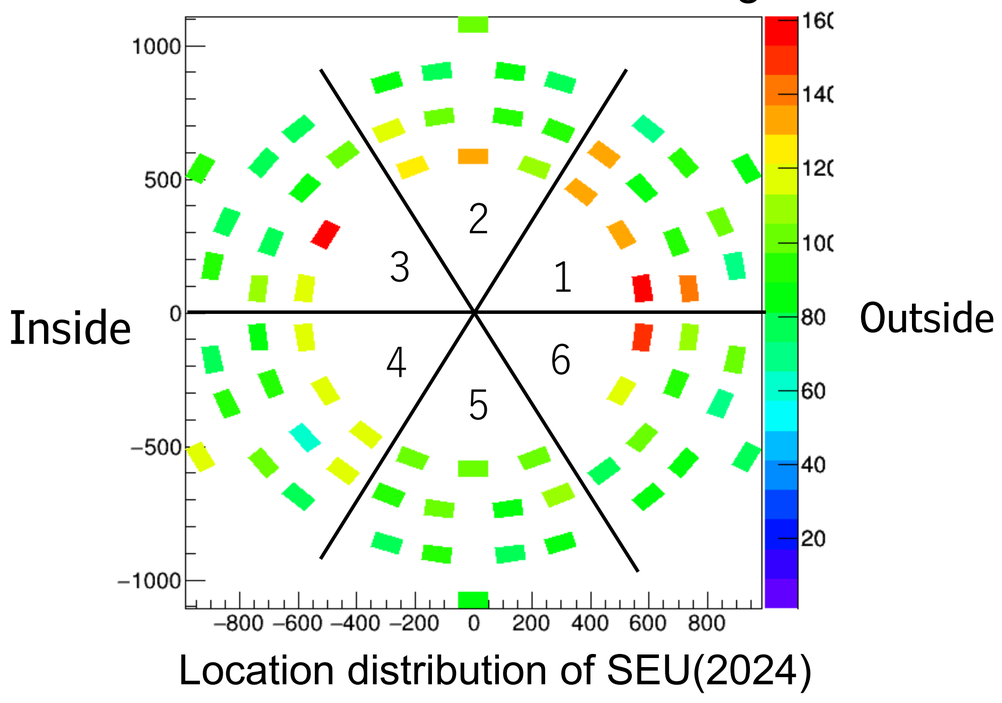
Comparison of Positional distribution in 2022 and 2024

Mgr2_1 and Mgr5_5 were excluded due to a data bug



Location distribution of SEU(2022)

Mgr3_1 and Mgr6_1 were excluded due to a data bug

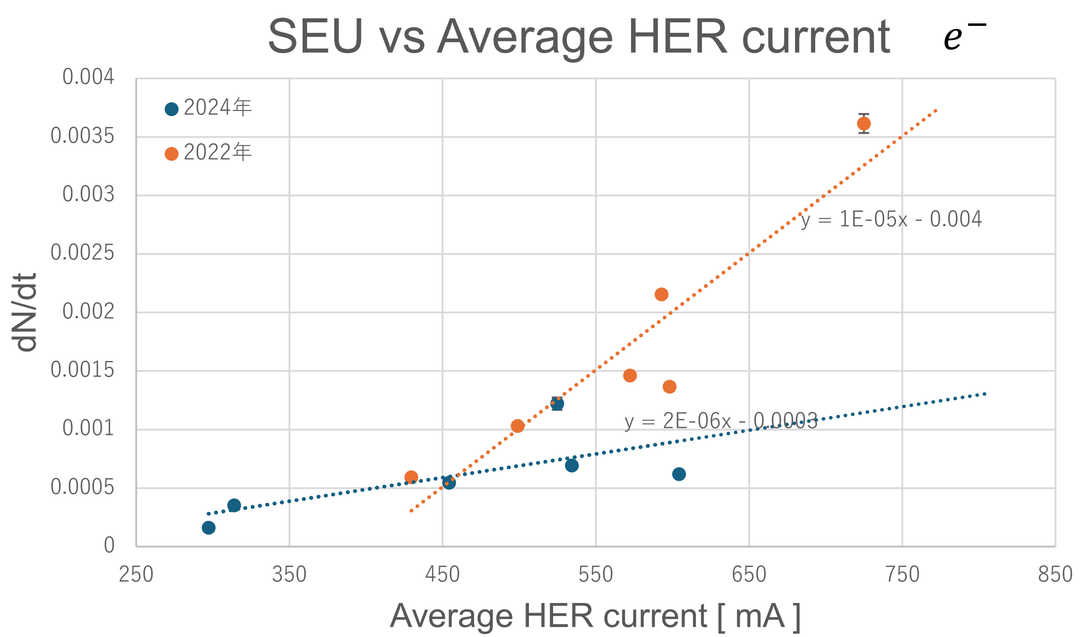


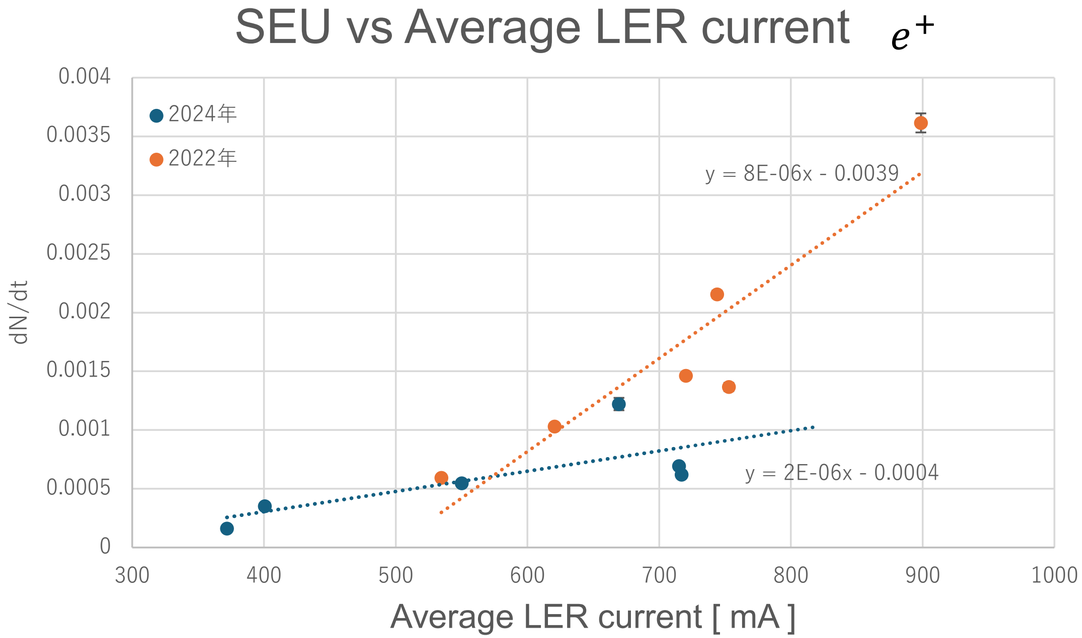
Location distribution of SEU(2024)

・These graphs plot the cumulative values for each merger board in fiscal years 2024 and 2022.

・Based on two graphs , it can be seen that SEUs occur more frequently toward the inner radius, and additionally, the outer side of the ring—specifically Sector 1—shows generally higher values.

SEU vs Average HER & LER current

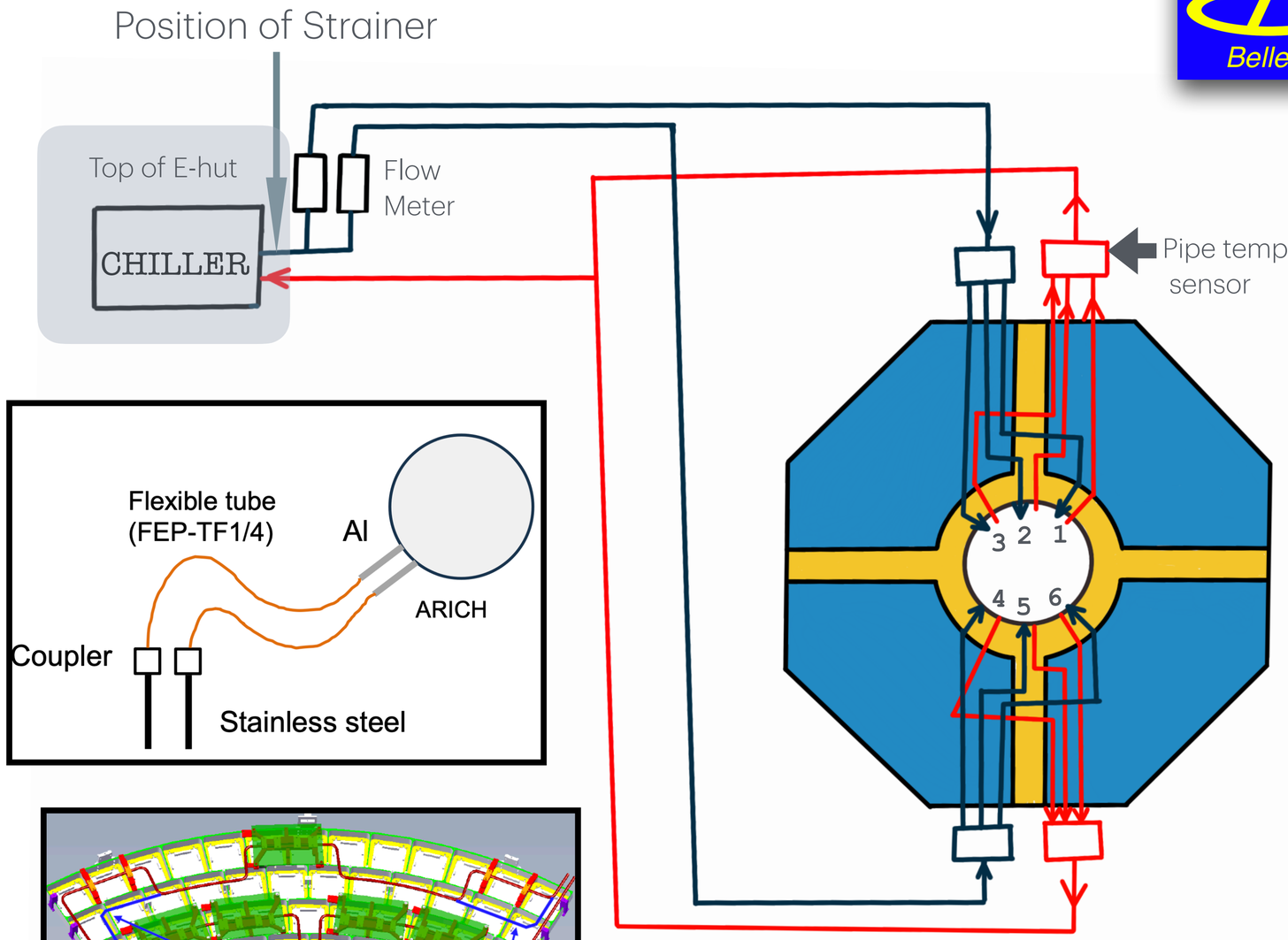


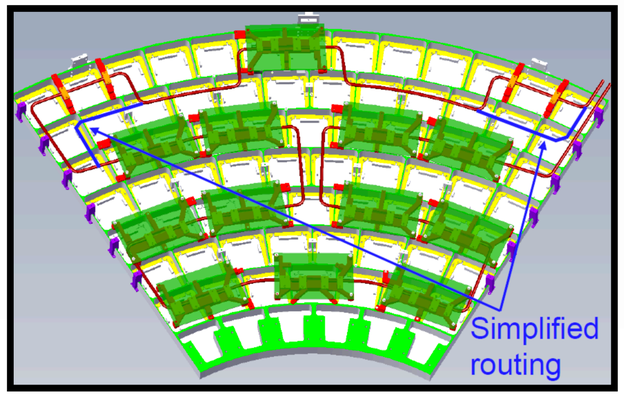


- The division intervals were based on the same time segments used for luminosity.
- For each segment, the slope of SEUs was plotted using the average HER and LER currents and the integrated values from all sectors.
- The same procedure was applied for 2022, and the results were also plotted.

ARICH Cooling System

- Cooling pipes are attached to the merger FPGAs and the structure.
- FEBs are attached to the structure
- ✓Additional cooling plate with a thermal pad GP300 is attached to the FEB FPGAs.
- HAPDs are connected to the FEBs.





Stainless pipes outside ARICH.
Plastic tubes at endcap.
Aluminum pipes inside ARICH.
Couplers (Joints) exist in the endcap.