Any updates for capability of FEE for higher(e.g.100kHz) or triggerless DAQ since last TRGDAQWS ? https://indico.belle2.org/event/7727/timetable/#20221202.detailed

	Is 100kHz L1 rate O.K. ?	Triggerless DAQ could be possible ?	Future upgrade
SVD https://indico.belle2.org/event/7727/contributions/49250/attachments/19754/29292/221202-SVDReadoutLimit_TRGDAQWS.pdf	No. (APV25 buffer)	Triggerless DAQ is not possible for the SVD.	SVD will be replaced in LS2
CDC	Max. acceptable trigger rate: ~250 kHz/FE • Limitation of the current FEE • throughput: 1 Gbps via SFP (2.5?)		Possible future improvements • throughput: 20 Gbps • 2 lanes of 40G QSFP on the upgraded FEE
TOP		**After LS2 upgrade:** – Assuming 15 MHz/PMT and 400 bits/hit: 200 Gbit/s per module, 3 Tbit/s total – SiPM: >50 MHz in same area, >**10 Tbit/s**	Full board stack redesign in LS2 ?
ARICH		FEB condition • Issue maximum 10 triggers within 26.4 us. • ARICH fully relies on this condition - Overflow never happens at f = 1.0/(26.4/10) ~380 kHz is the limit	

	Is 100kHz L1 rate O.K. ?	Triggerless DAQ could be possible ?	Future upgrade
ECL https://indico.belle2.org/event/7727/contributions/49254/attachments/19779/29325/2022.11.29_trgdaq_ecl_mikhail.remnev.pdf	?	?	FEE upgrade before LS2 ?
KLM https://indico.belle2.org/event/7727/contributions/49255/attachments/19776/29322/2022.12.02.KLM.highrate.triggerless_v3.pdf	• Buffer size on FEE is not enough to store such a large amount of data • Current FPGA transceiver is not capable of sending at such high-rate data etc.	Most likely a “triggerless” mode on would use trigger bits only (no waveform) or would require new FEE.	
TRG https://indico.belle2.org/event/7727/contributions/49256/attachments/19775/29321/b2gm221202_trghighrate.pdf	• GDL data • ~2.6 kB/ev = ~76MB/sec@30kHz, >0.6 sec to be read. Cannot handle >30kHz. • For 100kHz, needs to increase B2L line on GDL.		