

CDCFE upgrade

Yu Nakazawa (KEK)

October 23, 2025

Belle II Trigger/DAQ Workshop 2025 @Umeda, Osaka

Why we have to upgrade the CDC FEE?

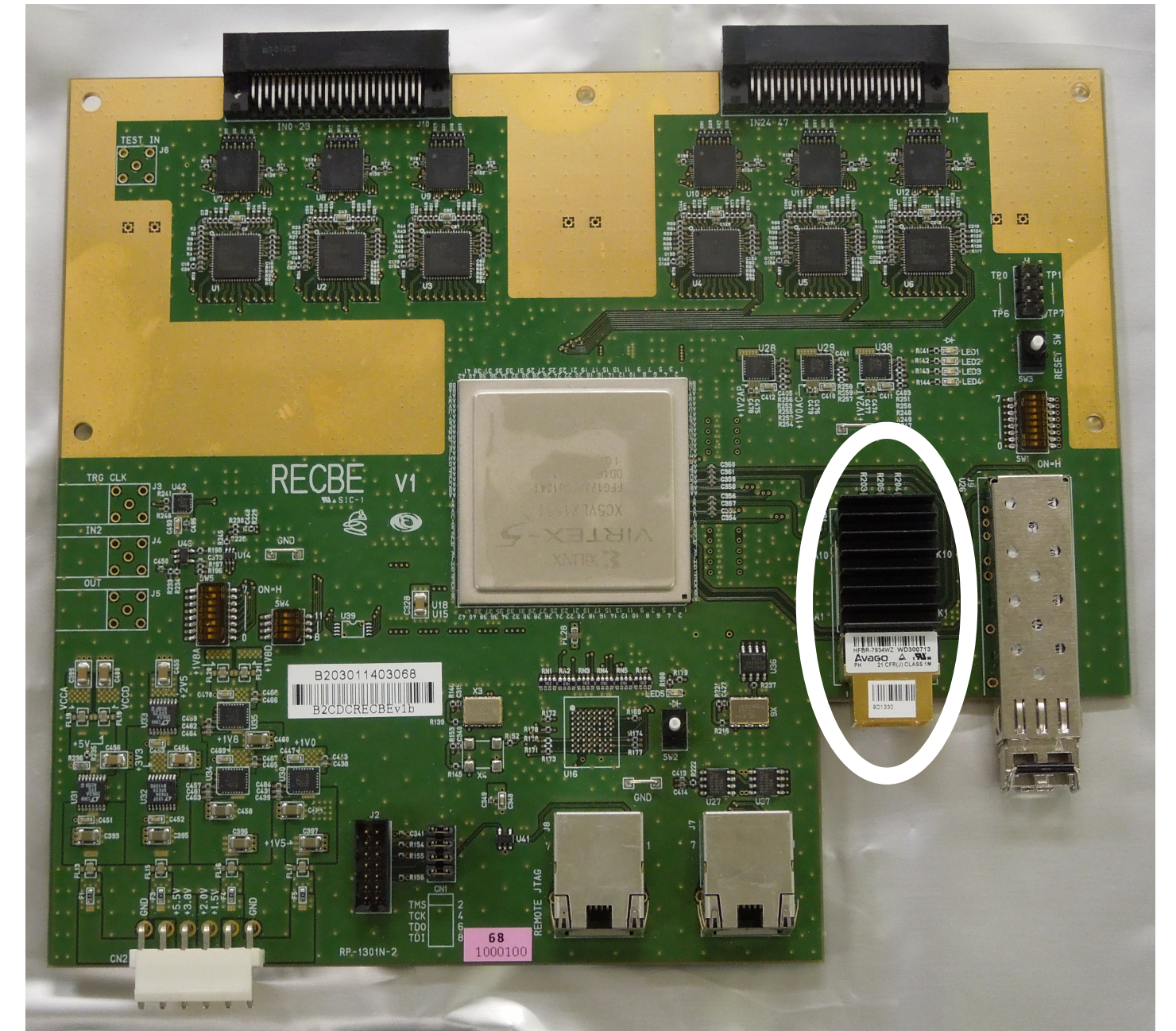
Lack of Radiation tolerance of the optical module for CDCTRG

- Requirement: 1 kGy
- Tolerance: 0.3 kGy

This could be broken until the end of Belle II.

Possible options

- Swap to the same module mounted on the TRG board (CDC Merger), and use other optical module on it with minor? board modification
 - Develop the new CDC FE satisfying the required radiation tolerance
- This is the baseline plan while adding some new motivations.



Motivations

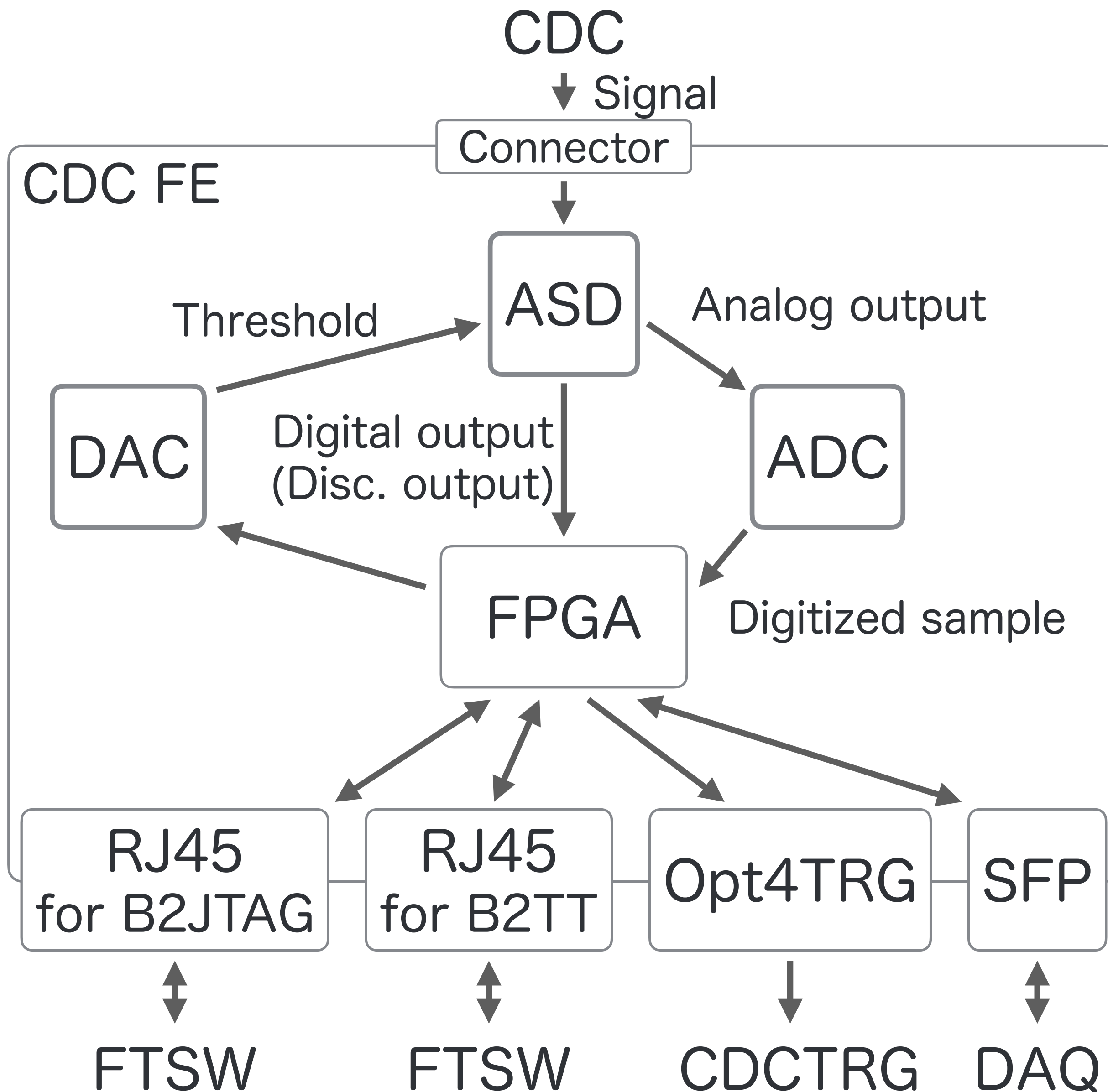
Reduce ASIC crosstalk

Satisfy the requirement of the radiation tolerance (req. 1 kGy)

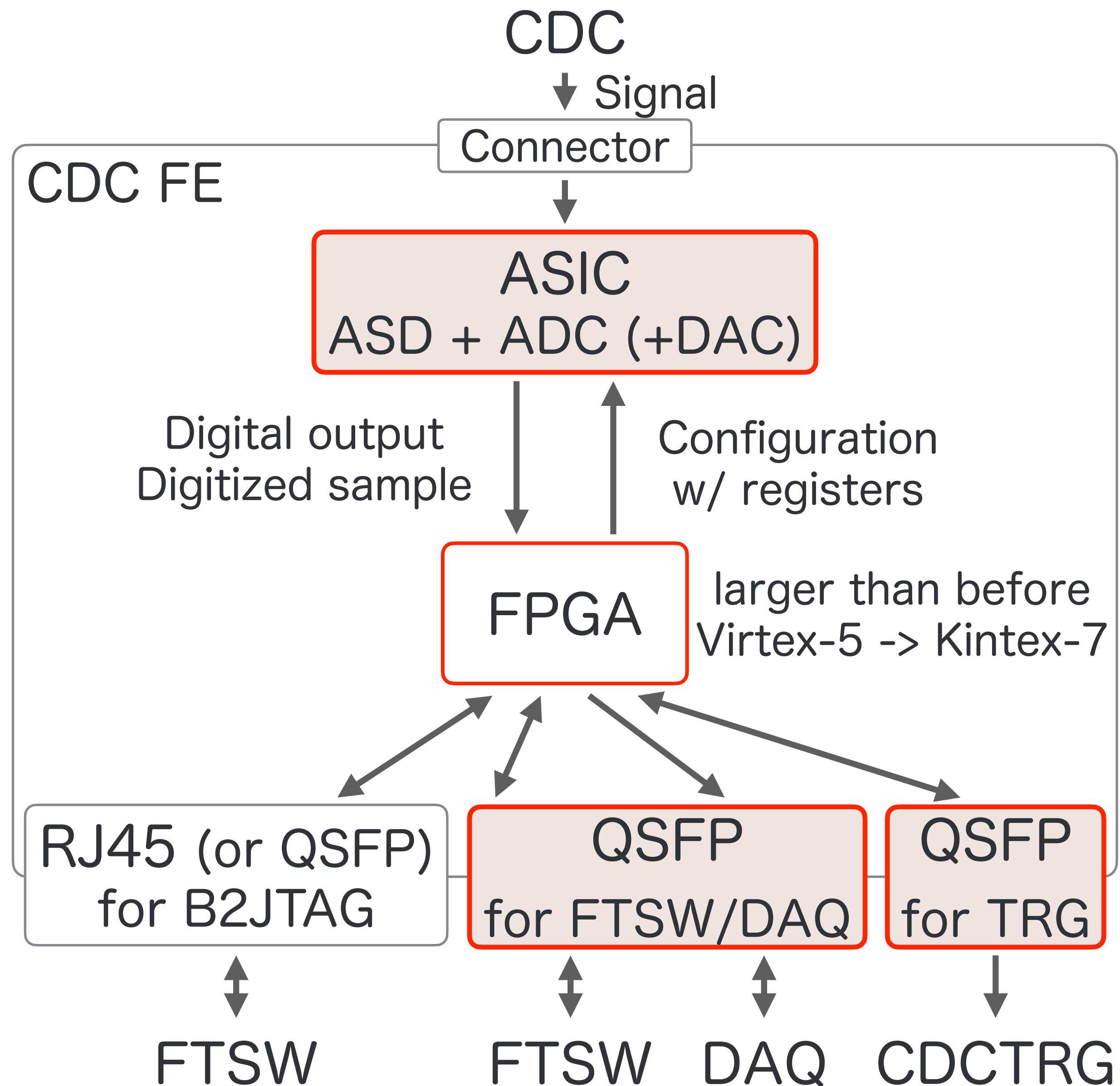
- H. Bae will report later

Transfer all hit data to CDCTRG

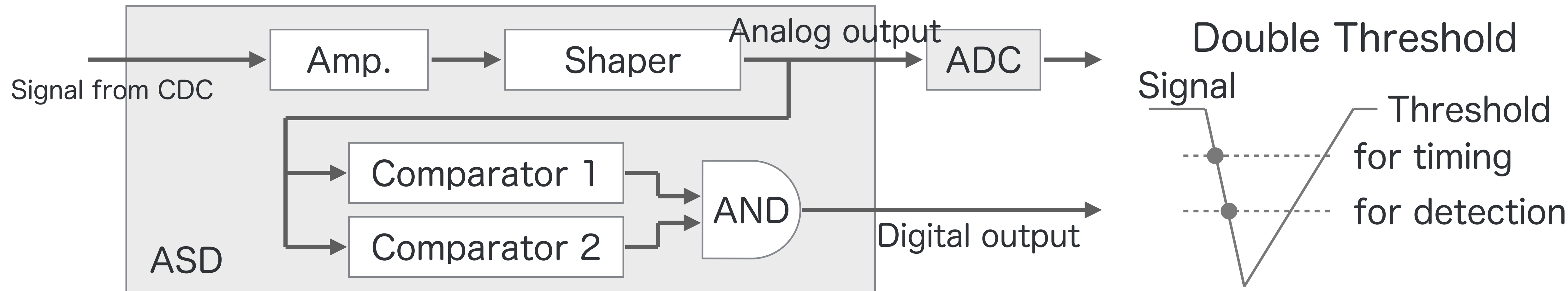
Current FE



Upgraded FE



ASIC design by M. Miyahara (KEK Esys)



ASD+ADC in a chip (8 ch/chip)

- Apply double thresholds for timing information
- Can adjust parameters by accessing registers
 - R/C for amp. and shaper, timing, and so on
- Suppress crosstalk by differential-type circuit

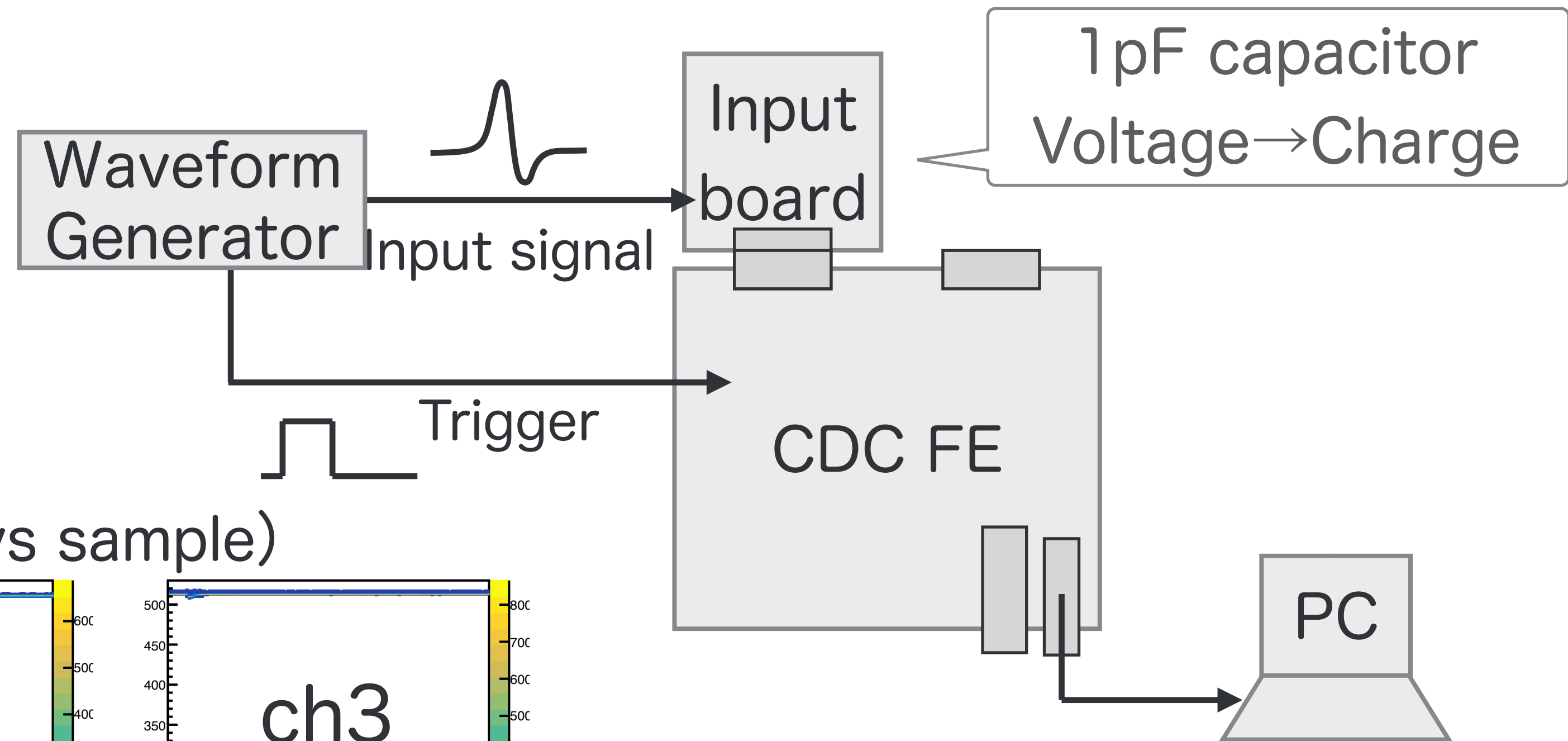
	Current	New
Gain [V/pC]	(Analog) 1.1, (Digital) 7	0.9
Linearity of gain [pC]	0.4	1.1
ADC sampling [MSPS]	31.25	63.5
ADC	10 bit, 2 Vp-p	10 bit, 2 Vp-p
Compactor	x	10 bit, 3 Vp-p
Analog crosstalk [mV/pC]	14	1.0
Power (ASD+ADC) [mW/ch]	134	41.3

Note: ADC sampling can be up to 100 MSPS for new ASIC

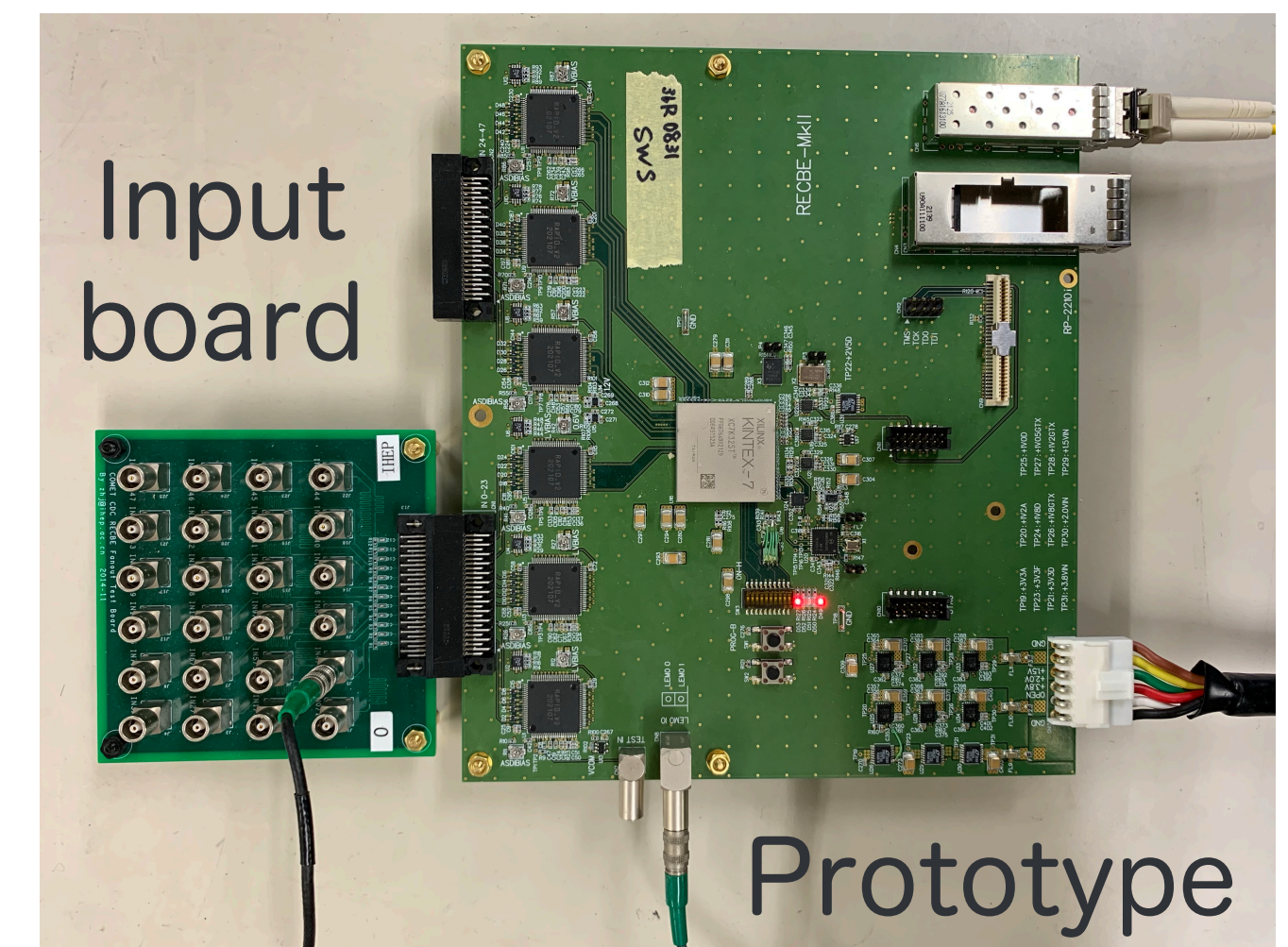
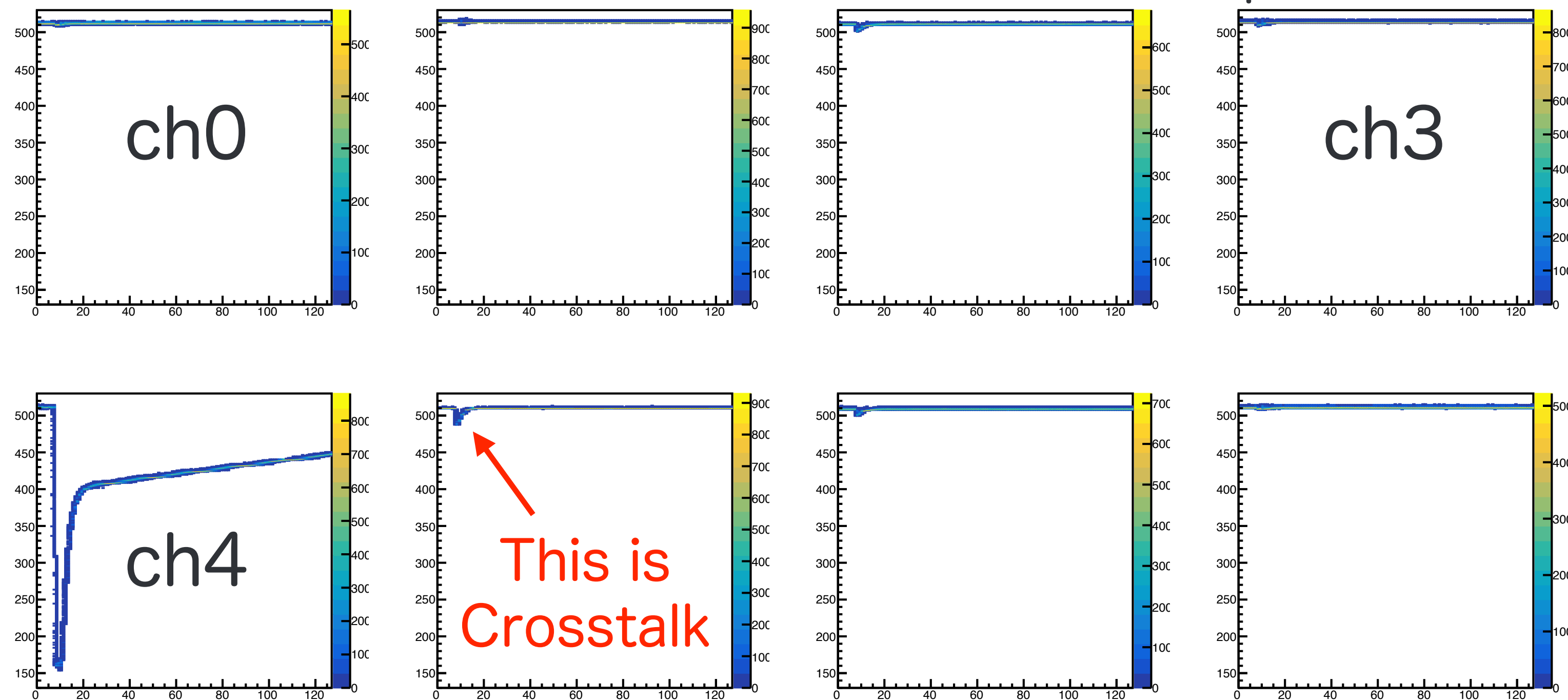
Motivation 1: Crosstalk reduction

What is crosstalk?

- Signal from waveform: 10 V $\rightarrow$ 10 pC (ch4)
- ASIC Threshold (baseline = 511)
508 for both



Overlaid waveforms (ADC value vs sample)



Motivation 1: Crosstalk reduction

Xiaodong Shi, Yu Nakazawa

Two types of crosstalk were found.

Analog-part-induced

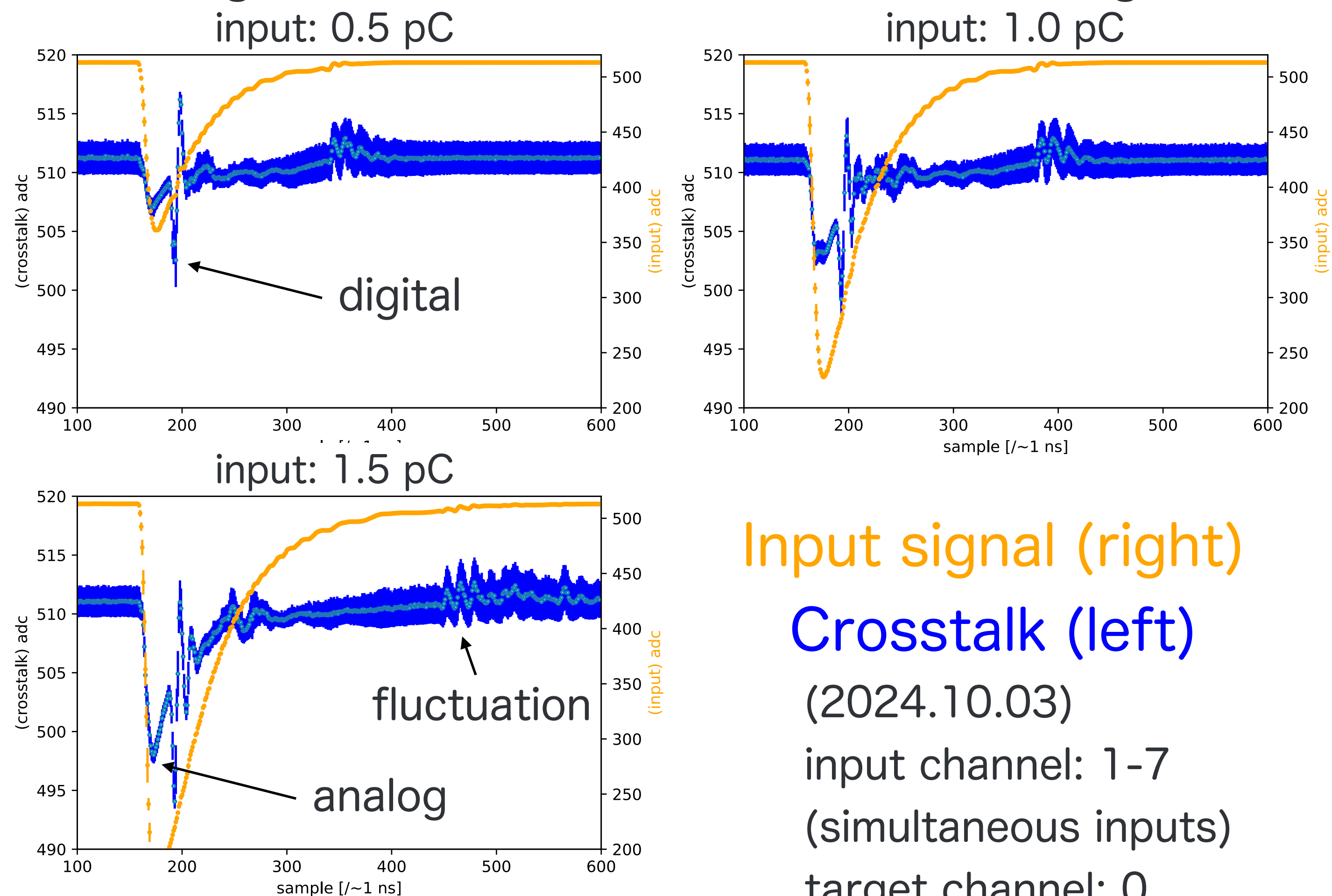
- correlated with the input charge
- occurs simultaneously with the input

Digital-part-induced

- Independent of the input charge (<10 ADC)
 - occurs with a delay after the input
- + small baseline fluctuation

The double-threshold technique can still cut most crosstalk.
Further studies for digital-induced crosstalk are necessary.

Average waveform at 1-ns intervals using TDC



Input signal (right)

Crosstalk (left)

(2024.10.03)

input channel: 1-7

(simultaneous inputs)

target channel: 0

Motivation 2: Radiation tolerance

Original radiation requirement for 10-year operation

- Neutron: $1 \times 10^{12} \text{ n}_{1\text{-MeV}}/\text{cm}^2$
- Gamma ray: 1 kGy
- I don't know how these numbers were determined. I'd like to re-evaluate them considering recent conditions.

Strategy

- Use parts identical to those already evaluated in the current modules as possible as we can. (e.g., regulators)
- Evaluate and select any new components individually. (done)
 - Optical module: QSFP+ 40G
 - Power section: LVDS buffer, Operational amplifier, Voltage monitor, etc
 - Clock: Clock Jitter Cleaner
 - ASIC (-> having sufficient tolerance)
- Perform irradiation tests on a FE prototype before mass production (not yet)

Motivation 3: High-rate TRG data transfer

Upgrade point: 14.8 Gbps -> 40 Gbps

- Assuming an 8b/10b protocol, the payload is 80% -> effective rate is 32 Gbps
- The impact on the TRG performance is under discussion in TRG.
- In the early phase of operation, we can run with the current data format and algorithms of CDCTRG.

Raw data size on the CDC FEE FPGA

- 1 sample per channel: ADC 10 bits + TDC 16 bits
- ADC sampling: 63.5 MHz
- The ADC sampling period is split into 16 sub-intervals to carry TDC timing. $\text{LSB} = 1\text{ ns}$

Possible data sent to TRG

- ADC: 9 bits/ch/sample (baseline is 511, and chamber signals are lower than it.)
- TDC: 4 bits/ch/sample
- Within one sample, only the fastest TDC value per channel is valid.
 - Multiple TDC hits in the same sample are not recorded.

Possible data format (Req.: < 32 Gbps)

Scenario 1: Full data -> 39.624 Gbps ❌

- 1 sample per channel: ADC 9 bits + TDC 4 bits
- Transfer sampling rate: 63.5 MHz
- If CDCTRG also handles CDC DAQ, additional 10 Gbps for the current DAQ is possible.
- This needs one extra QSFP lane (1/4 QSFP) in addition to one QSFP -> Firmware/cabling need to be changed.

Scenario 2: Half sampling rate -> 21.336 Gbps ○

- 1 sample per channel: ADC 9 bits + TDC 5 bits
- Transfer sampling rate: 31.75 MHz
- Sum/Average for down-sampling is necessary.
- (Full ADC = 10 bits is still possible. -> 22.86 Gbps)

Scenario 3: Half ADC resolution with full sampling rate -> 30.48 Gbps ○

- 1 sample per channel: ADC 5 bits + TDC 4 bits
- Transfer sampling rate: 63.5 MHz

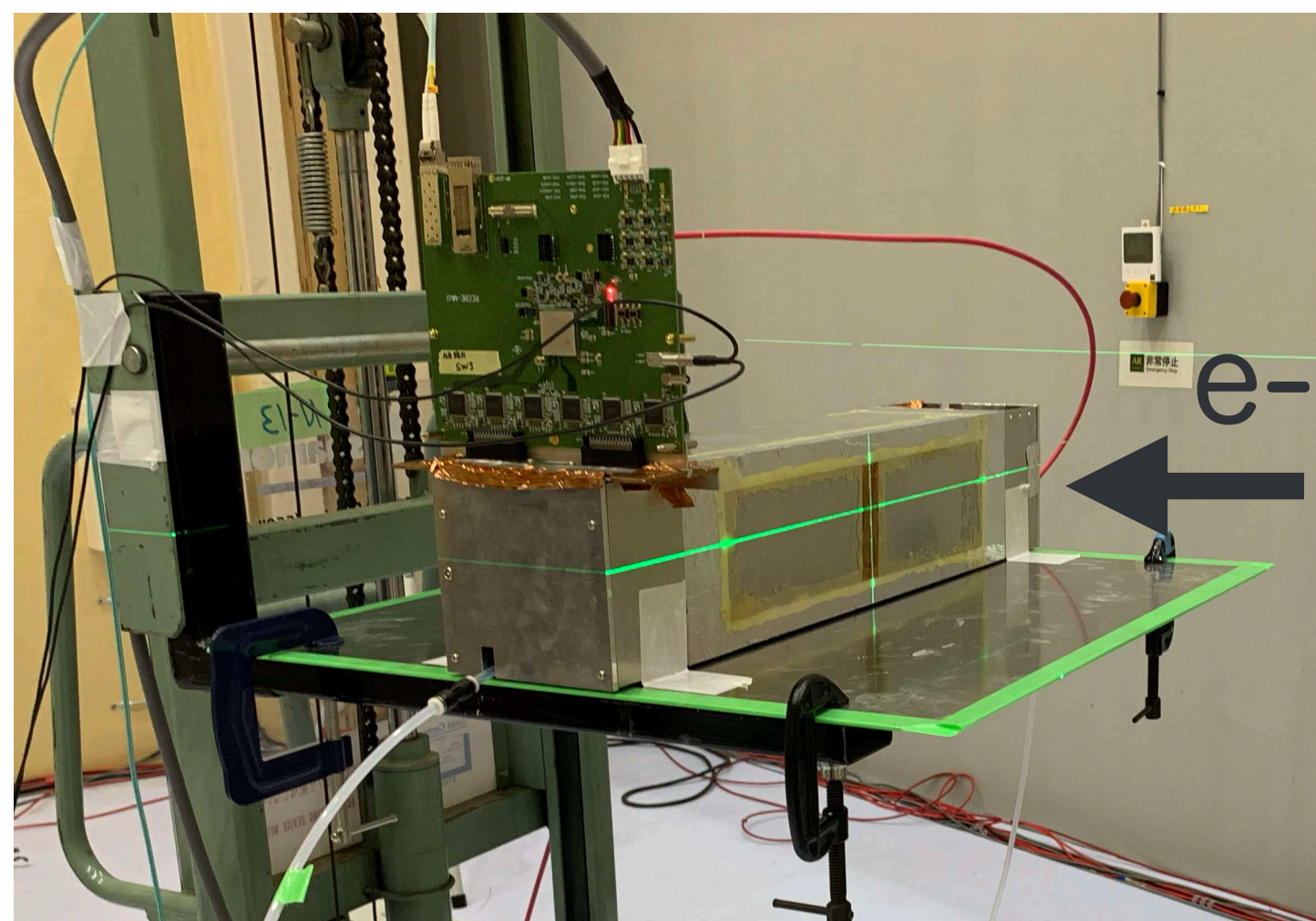
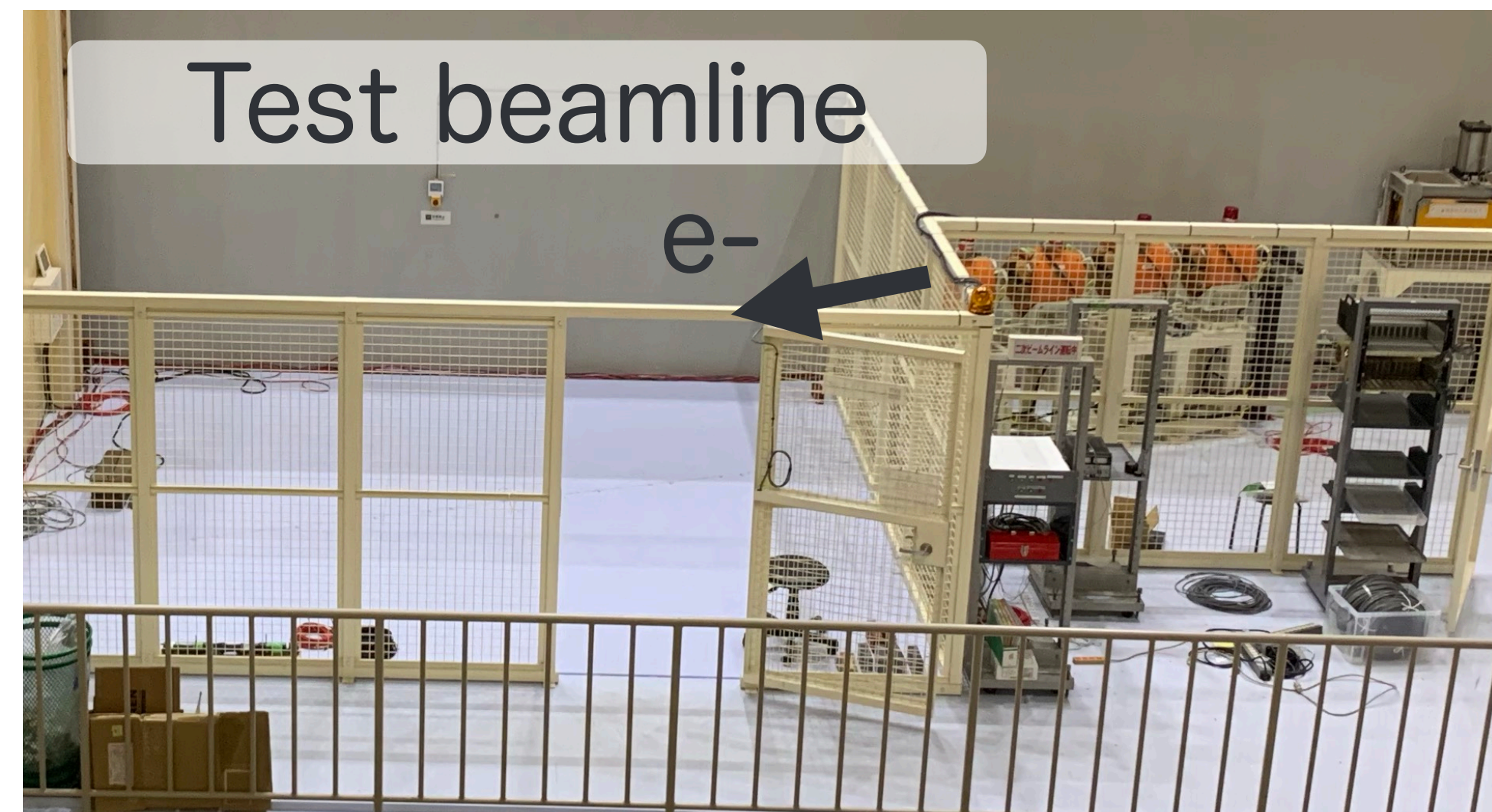
Performance

Performance study

w/ (NPC) Y.Ma, M.Niiyama, M.Takizawa
(UT) A.Gonnokami, (OMU) M.Oki, E.Nakano

- Tested at the KEK PF-AR test beamline
- Beam: 3-4 GeV electrons, DAQ rate ~ 100 Hz
- Trigger: coincidence of 2 scintillators in the beamline
- Main target: spatial resolution
- Measurements under identical conditions for both the new and current modules.

(Same HV, signal thresholds (as close as possible), and analysis tools)



[Chamber]

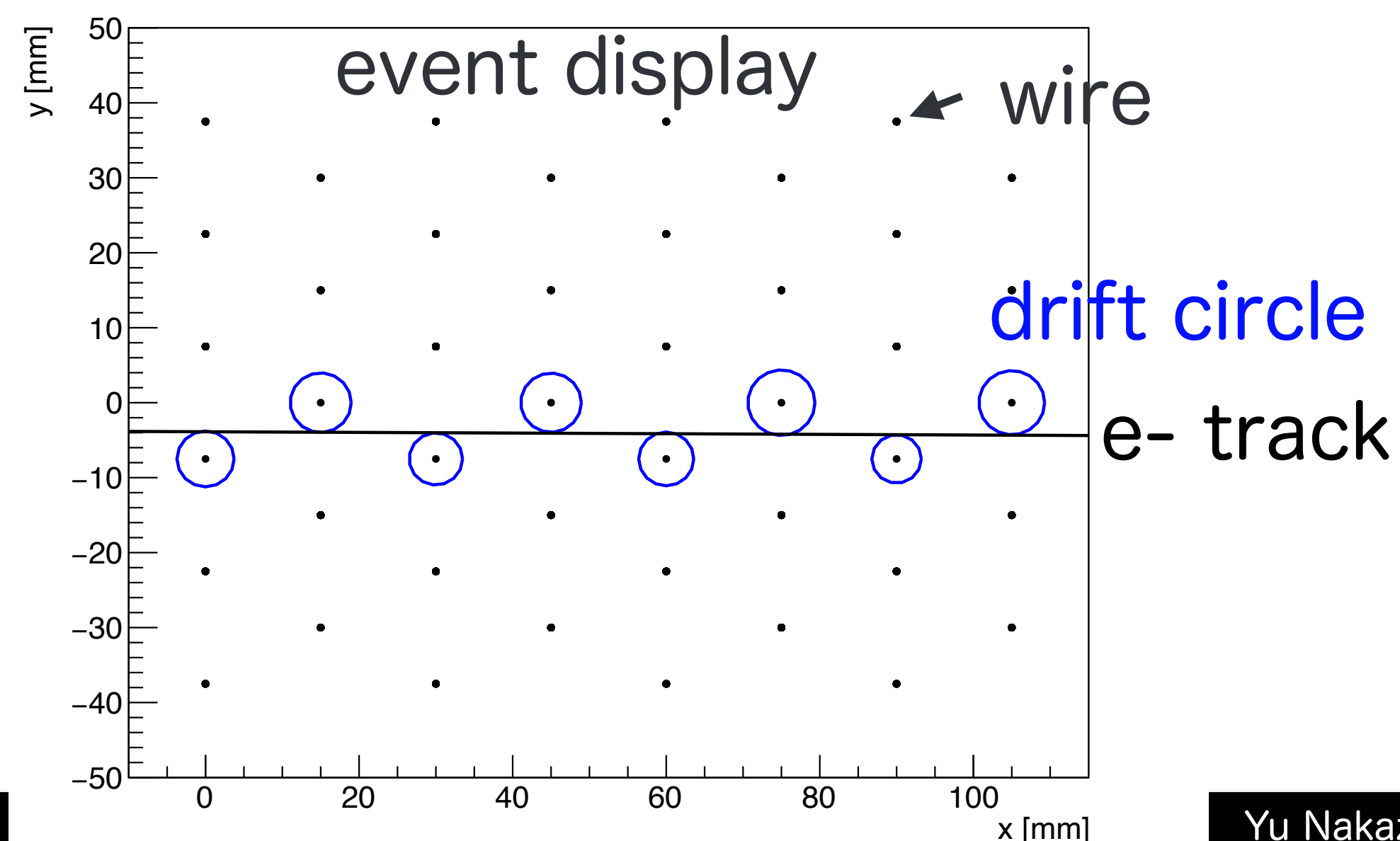
Cell: 15 mm x 15 mm

Layout: 8 layers

44 wires

Gas: He:C₂H₆=50:50

HV: 2.3 kV



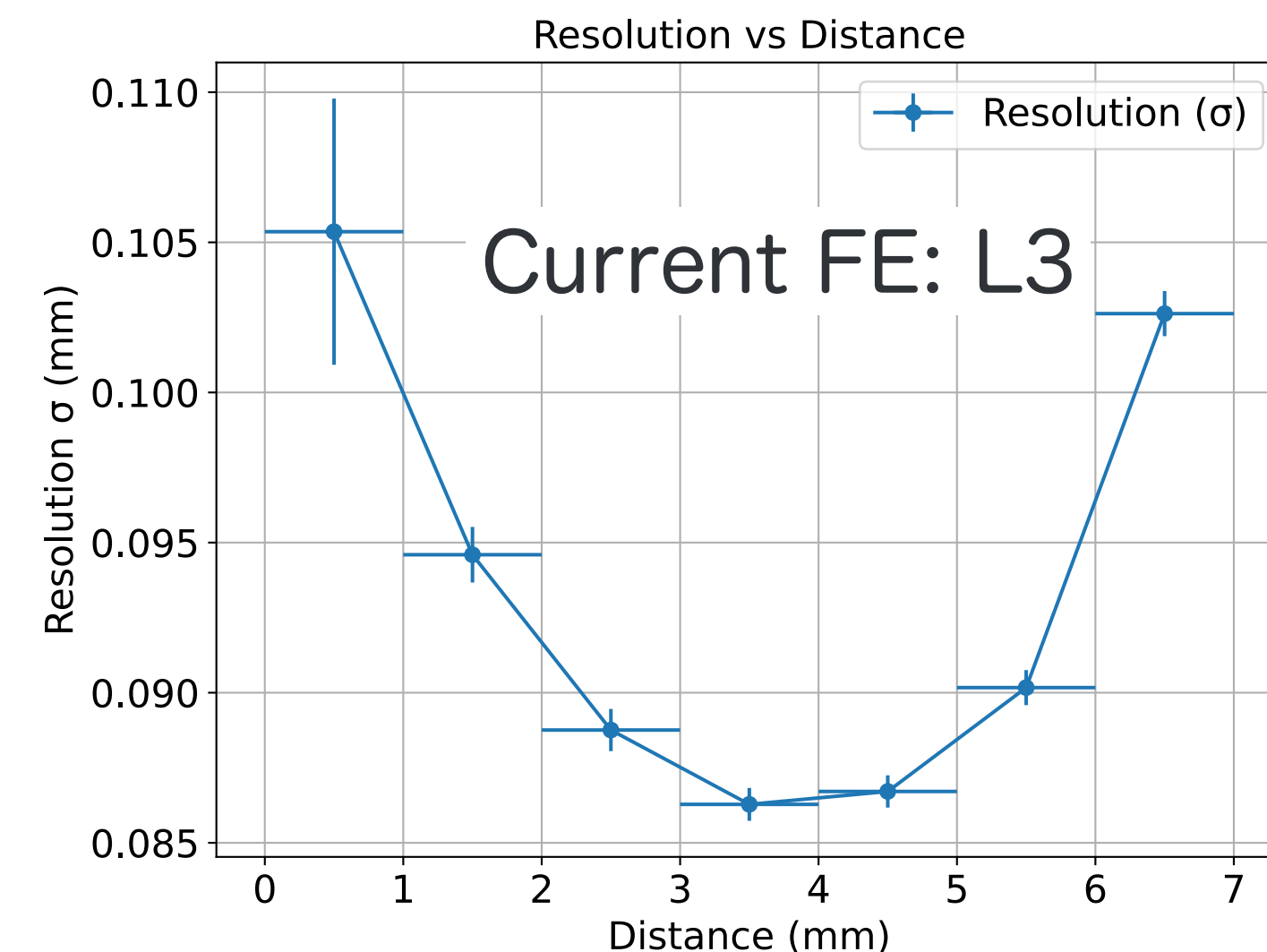
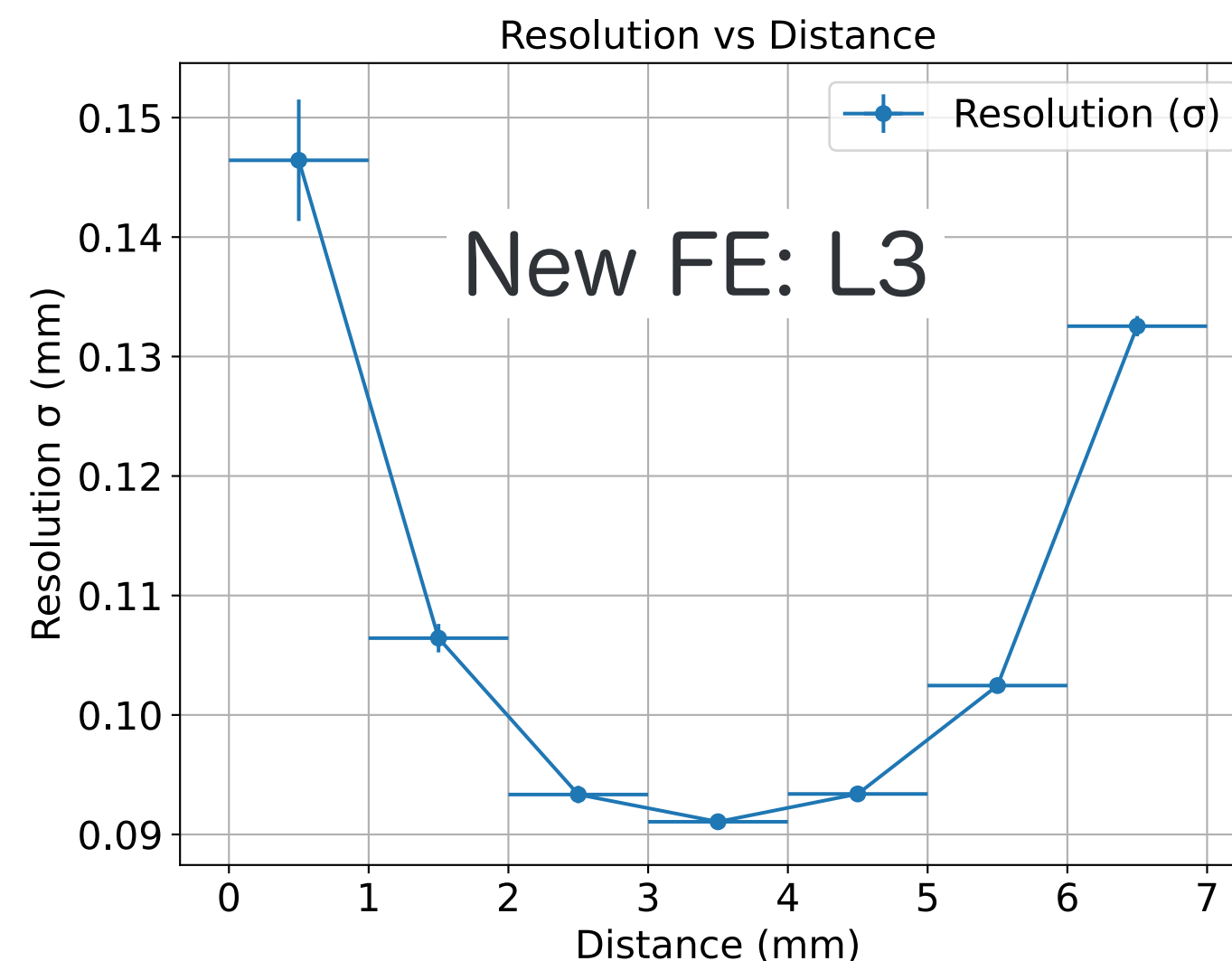
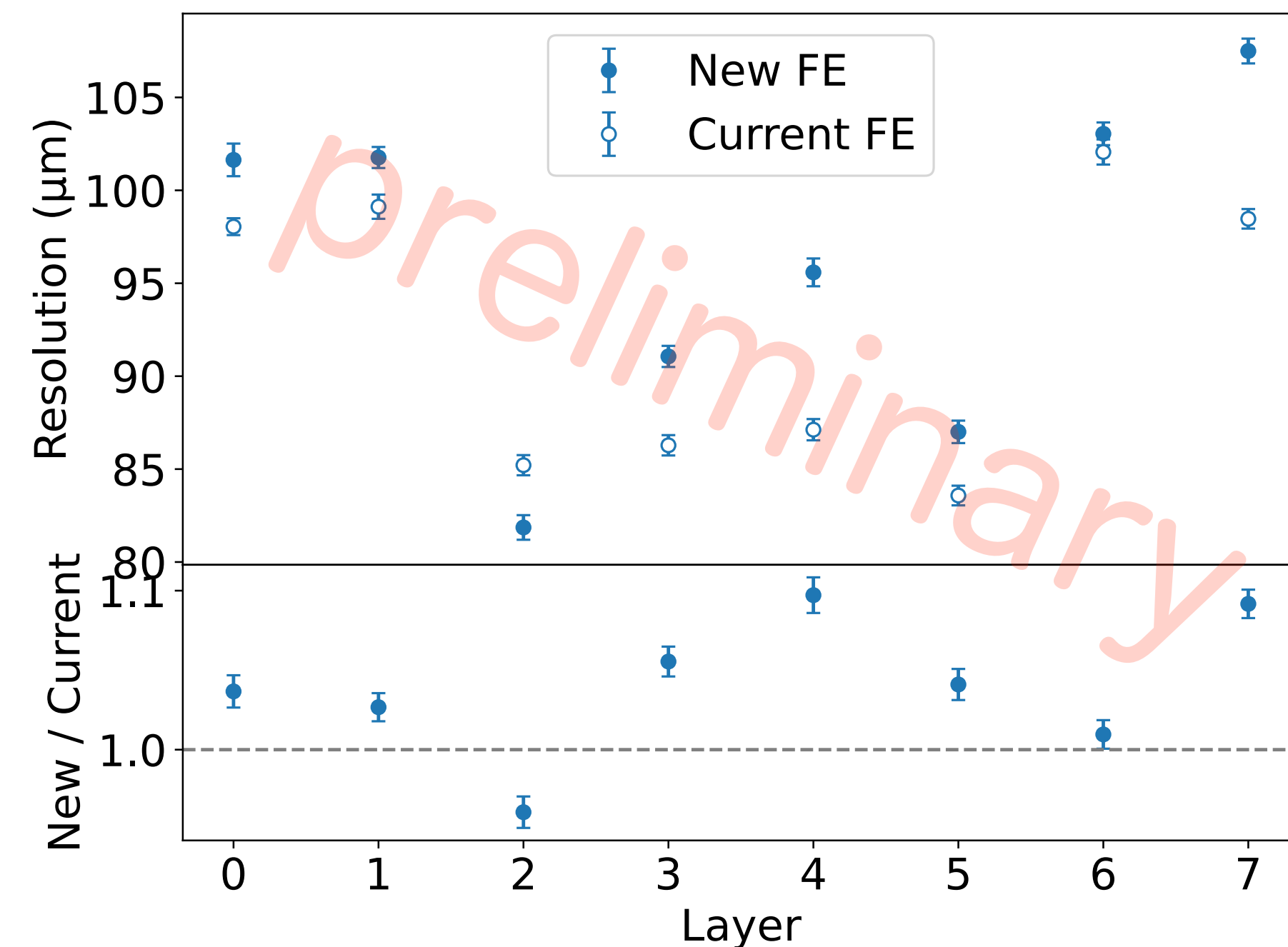
Spatial resolution

The spacial resolution is ~ 1.05 times higher than that of the current module.

- Looking at drift distance 3–4 mm to check the best resolution.
- Many charged particles have $p < 1$ GeV/c in physic runs; multiple scattering dominates.
- The impact on the analysis may be minimal?
-> needs to be confirmed

Issue: 30-40% worse resolution near the wire and at the cell edge

- Possible reason1:
Because the used chamber has a staggered-cell geometry, track reconstruction near the wires and at the cell edges is difficult. A $\sim 5\%$ difference in resolution may be amplified
- Possible reason2:
With the lower ASIC gain, the time-walk effect for small signals may be significant.



Summary

The current CDC FE may need to be replaced in the future due to insufficient radiation tolerance of the optical module.

Upgraded FE module is almost finalized.

- New dedicated ASICs have already been developed.
- Parts meeting the requirement of the radiation tolerance have been found.

Performance evaluation is in progress.

- Basic performance of ASIC has been measured.
- Spatial resolution and dE/dx resolution have been evaluated using a test chamber.

Next: better understand the spatial resolution and evaluate performance at lower gas gain

- Plan: perform a beam test with the test chamber

We would like to start mass production in 2026 if the remaining issues are solved.

- Review will start soon (1st: next week).

List of main tasks

Radiation hardness

- Perform irradiation tests using a FE prototype before mass production.
- Re-consider the requirements of the radiation tolerance including recent machine conditions.

CDCTRG

- Consider what we can do with such data.

Perfomance

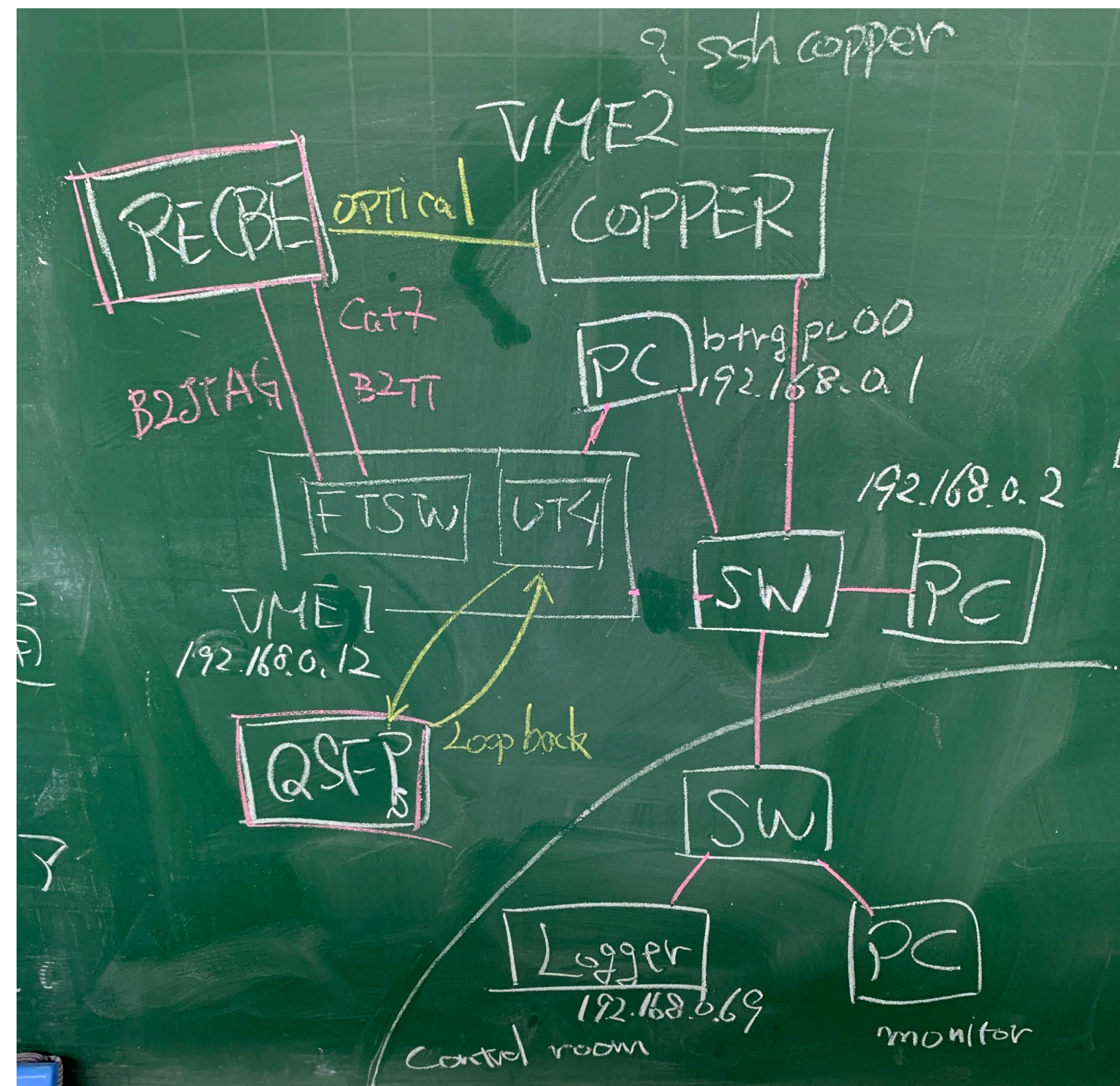
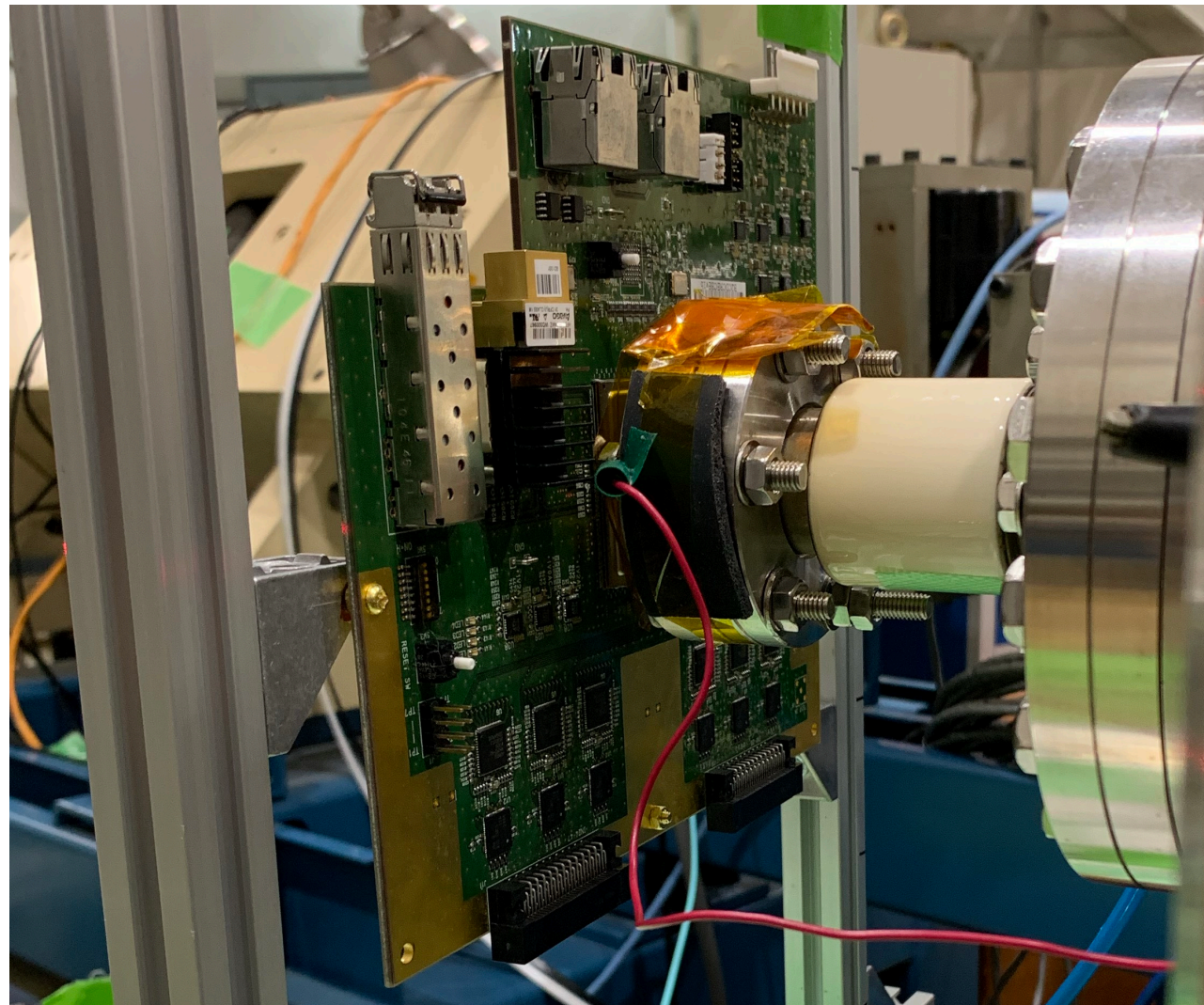
- Perform a detailed study of digital-part-induced crosstalk.
 - Evaluate the impact on the momentum resolution, and determine acceptable limits for degradation of the spatial resolution (performance study)
 - Investigate why the resolution degrades at the cell edges.
 - Evaluate the spatial resolution at lower gas gain as discussed recently.
- } beam test

Others

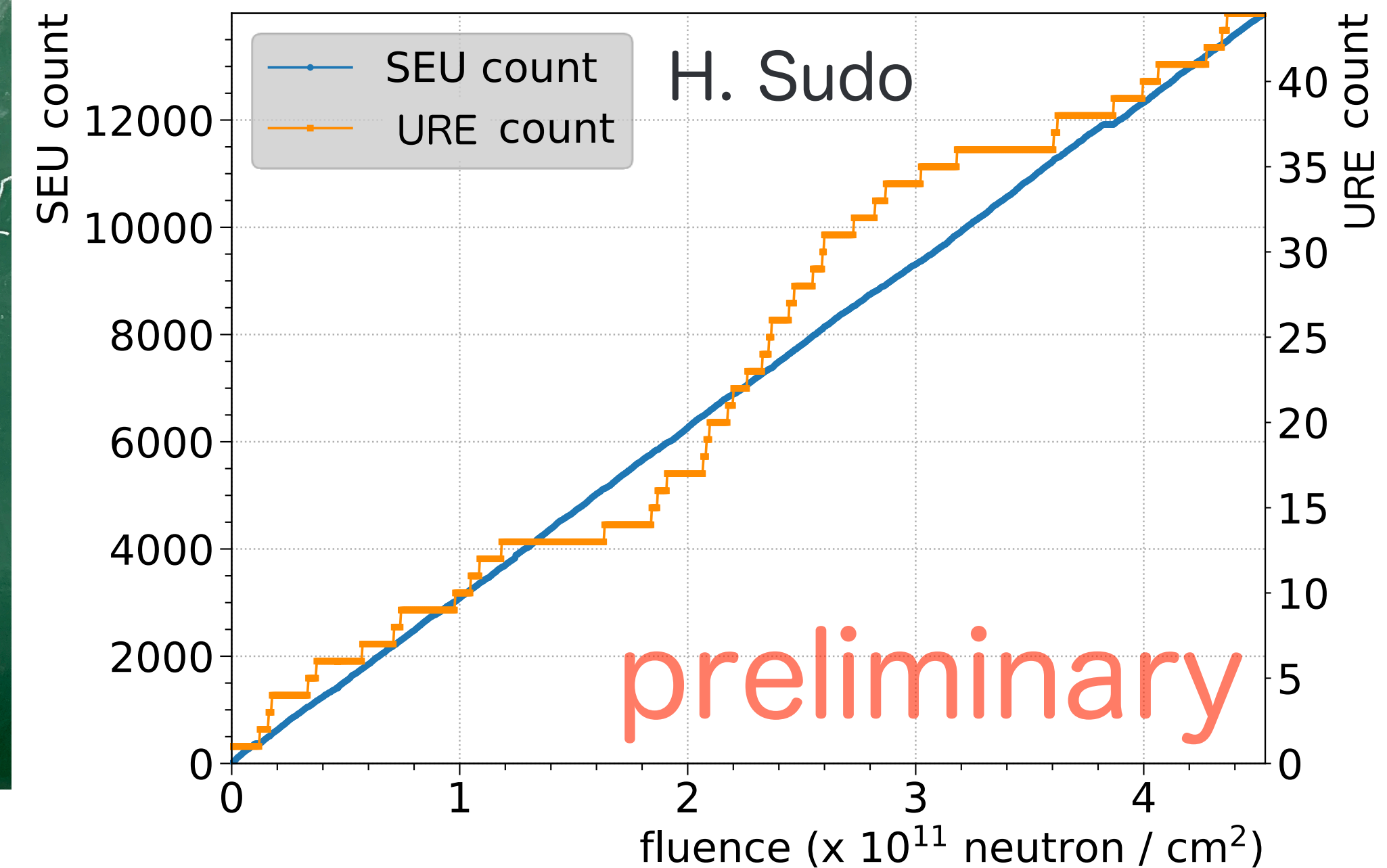
- After fixing the firmware, the power consumption needs to be measured.

Backup

Current FE



w/ T. Koga, H. Sudo,
T. Hotta, M. Niiyama, M. Sumihama

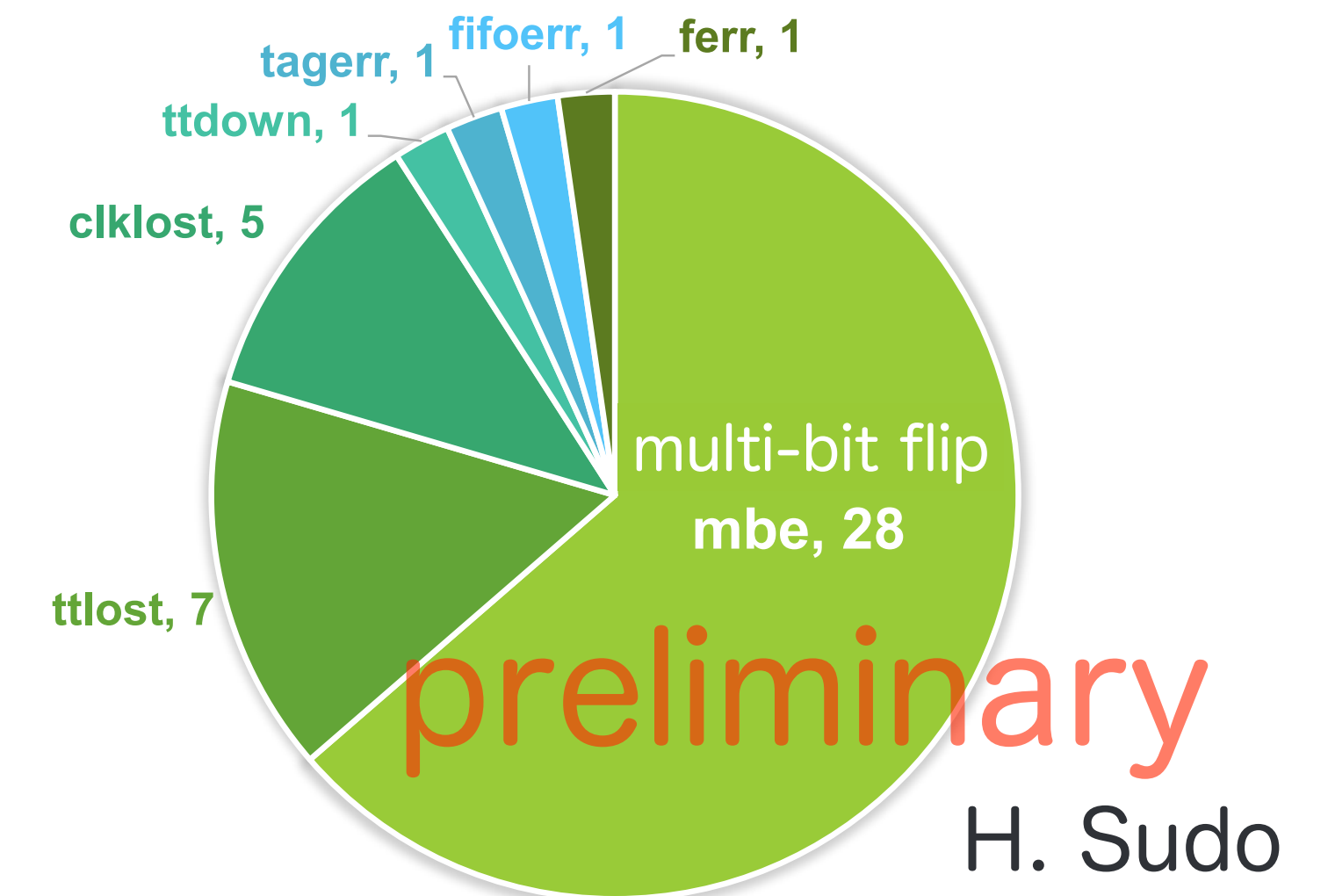


Total fluence: 4.5×10^{11} n/cm²

SEU Controller successfully detects and corrects SEUs

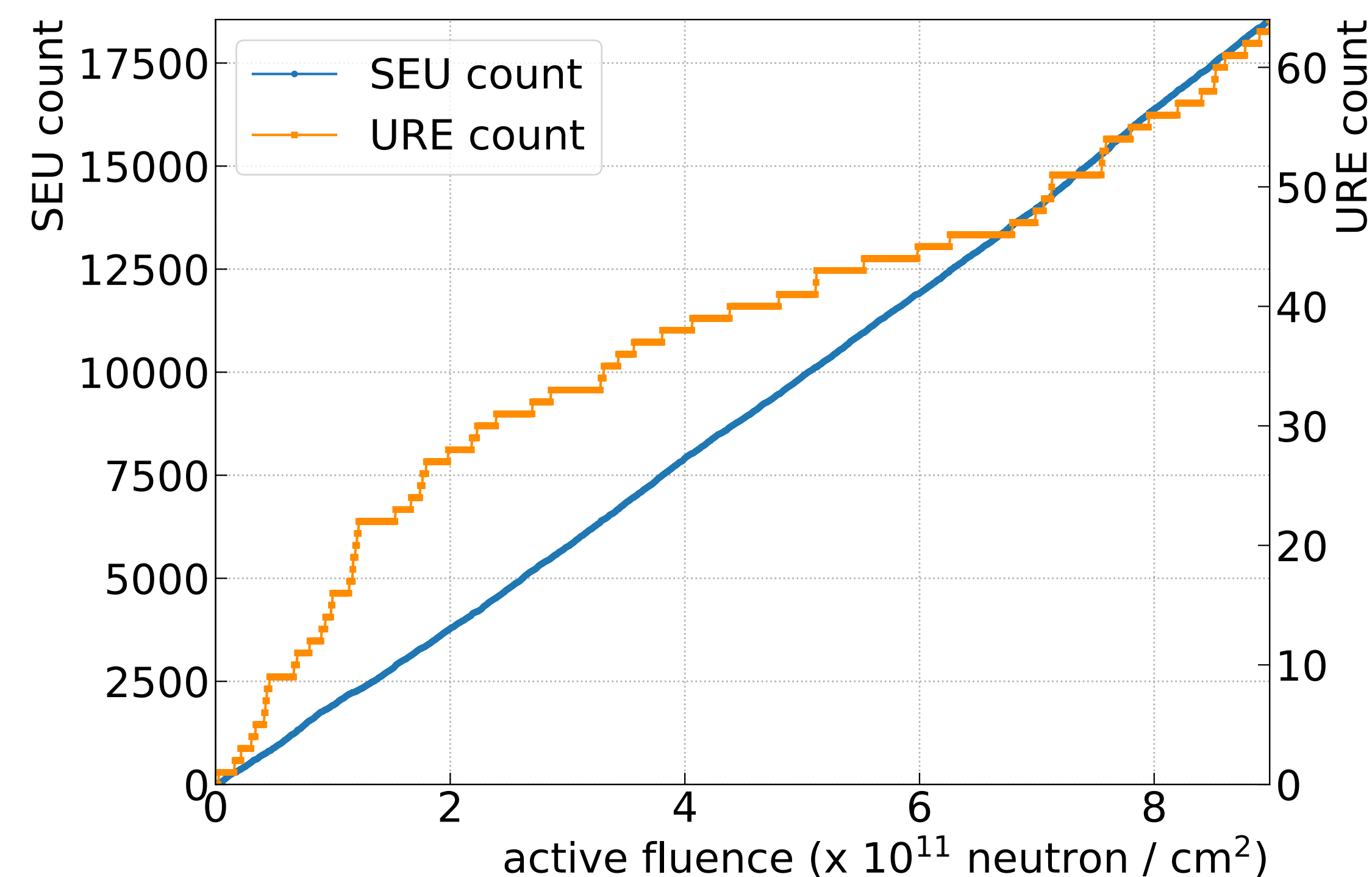
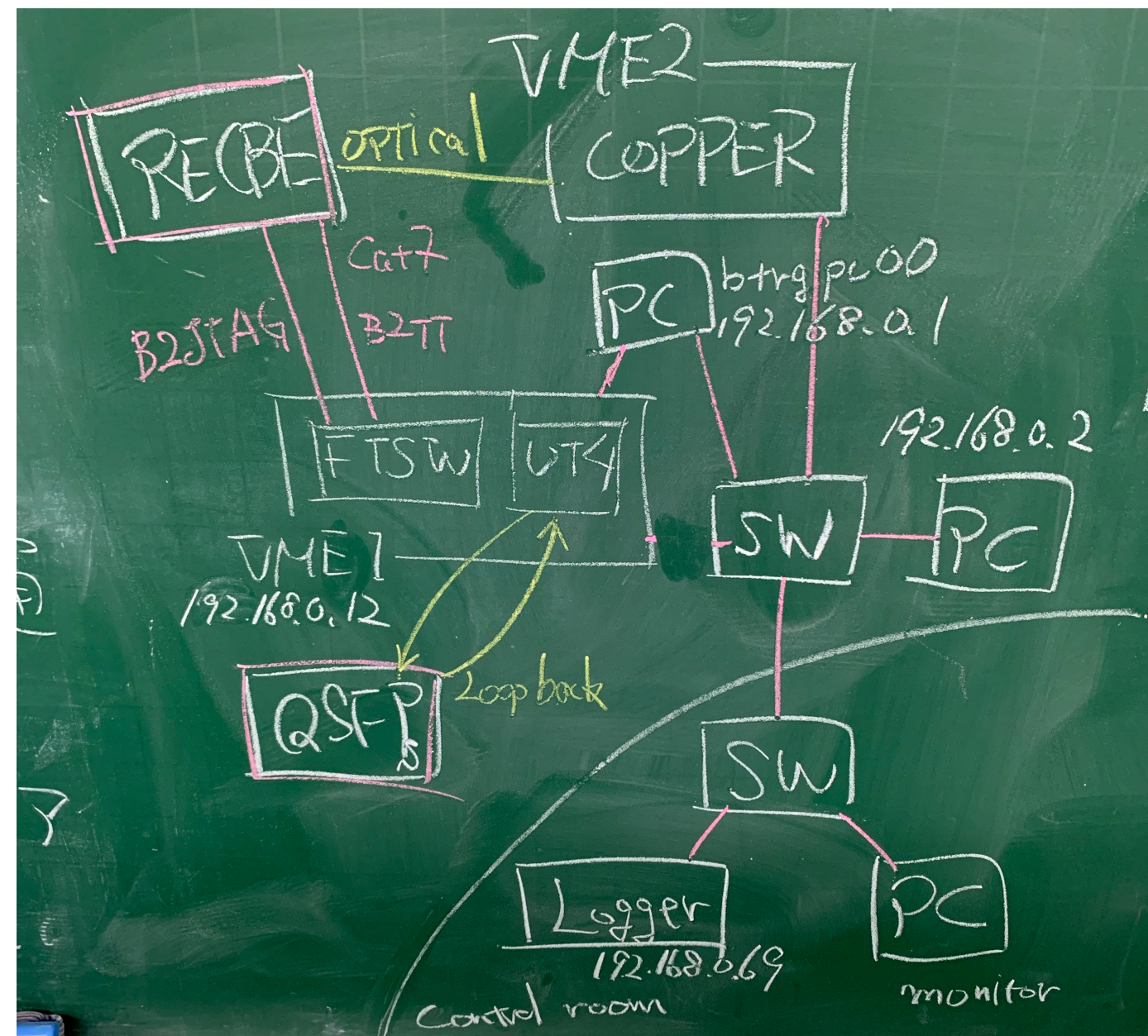
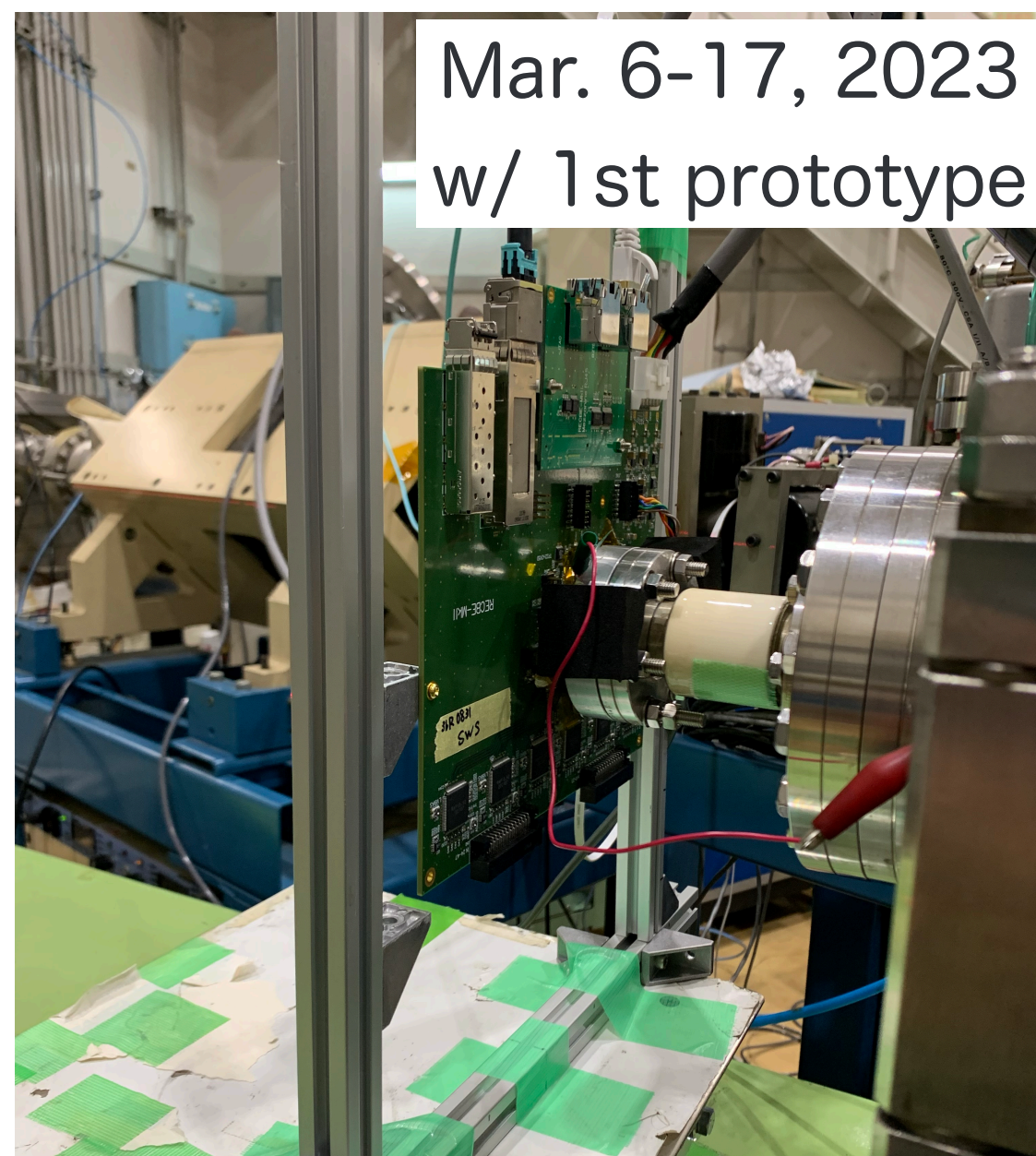
- SEU rate: 3.1×10^{-8} SEU/(neutron/cm²)
- URE rate 1.0×10^{-10} URE/(neutron/cm²)
 - URE = UnRecoverable Error including multi-bit flips and all the FTSW-detected errors
 - requires FPGA re-configuration to fix

The error check cycle on b2tt is fast, so it detects SEUs to be corrected before the repair module does. => major errors in the past physics runs



Neutron irradiation for FPGA

w/ T. Koga, H. Sudo, Y.-T. Lai,
T. Hotta, M. Niiyama, M. Sumihama



Neutron beam: $^9\text{Be} + d$ (3 MeV) $\rightarrow$ $^{10}\text{B} + n$ (~ 2 MeV)

Test firmware: almost the same as the current CDC FEE

- No change in the FPGA between the 1st and 2nd prototypes.

Result: No permanent damage has been observed.

- SEU rate: 2.1×10^{-8} SEU/(neutron/ cm^2)
- URE rate 7.1×10^{-11} URE/(neutron/ cm^2)

(*) UnRecoverable Error (URE) requires firmware configuration to fix this error

Neutron irradiation for FPGA

w/ T. Koga, H. Sudo, Y.-T. Lai,
T. Hotta, M. Niiyama, M. Sumihama

Error related to trigger communication

- A PRBS pattern is transmitted.
- Detections of errors in the pattern: 14 times

pseudorandom binary sequence: PRBS

Current vs Upgraded FEE

- double logic size, but the error rate is equivalent or possibly smaller than xc5vlx155t!!
- thanks to the smaller technology of FPGA.

	Config. logic block # of slices	technology [nm]	SEU rate [n/cm ²]	URE rate [n/cm ²]
Current FEE xc5vlx155t	24,320	65	3.1×10^{-8}	1.0×10^{-10}
Upgraded FEE xc7k325t	50,950	28	2.1×10^{-8}	7.1×10^{-11}

Handwritten red annotations:
- An arrow from 24,320 to 50,950 with "x2".
- An arrow from 3.1×10^{-8} to 2.1×10^{-8} with "x2/3".
- An arrow from 1.0×10^{-10} to 7.1×10^{-11} with "-30%".

Note: Since conditions are different, the URE rate may not be the same as during physics runs.

Block diagram of ASIC

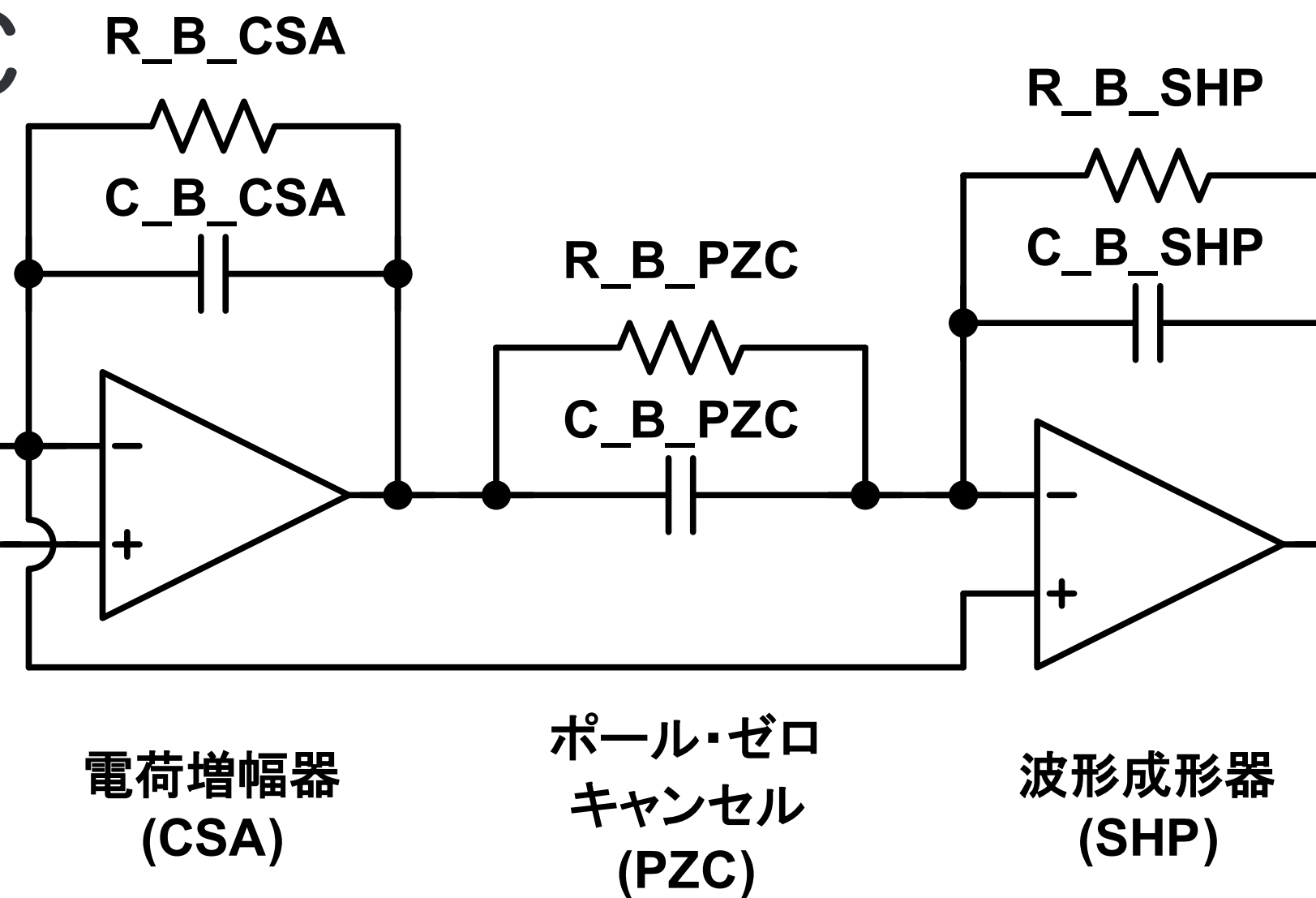
ASICに書き込んでいる値を確認してください。

オペアンプが線形で動く範囲は
0.3~3V程度まで。

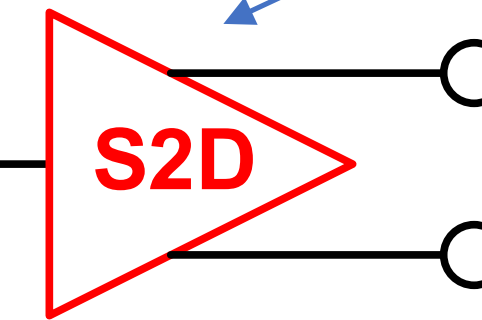
Analog input
Common V

アナログ入力 IN#
コモン電圧 VCM
(ベース電圧)

1.65V



$1.65V \pm V_o$



アナログモニタ,
ADCへ to ADC

差動信号振幅
 $GC_BUF \times V_o$

S2Dが線形に動く範囲は
 $\pm 0.75 \sim 0.8V$ くらいまで。

GC_BUF[1:0]
b'00 = 約0.5倍
b'01 = 約0.7倍 <- default
b'10 = 約1.0倍
b'11 = 約1.65倍

Fixed latency
固定遅延

3.2ns~25.6ns,
8step調整

Minimum pulse-
width correction

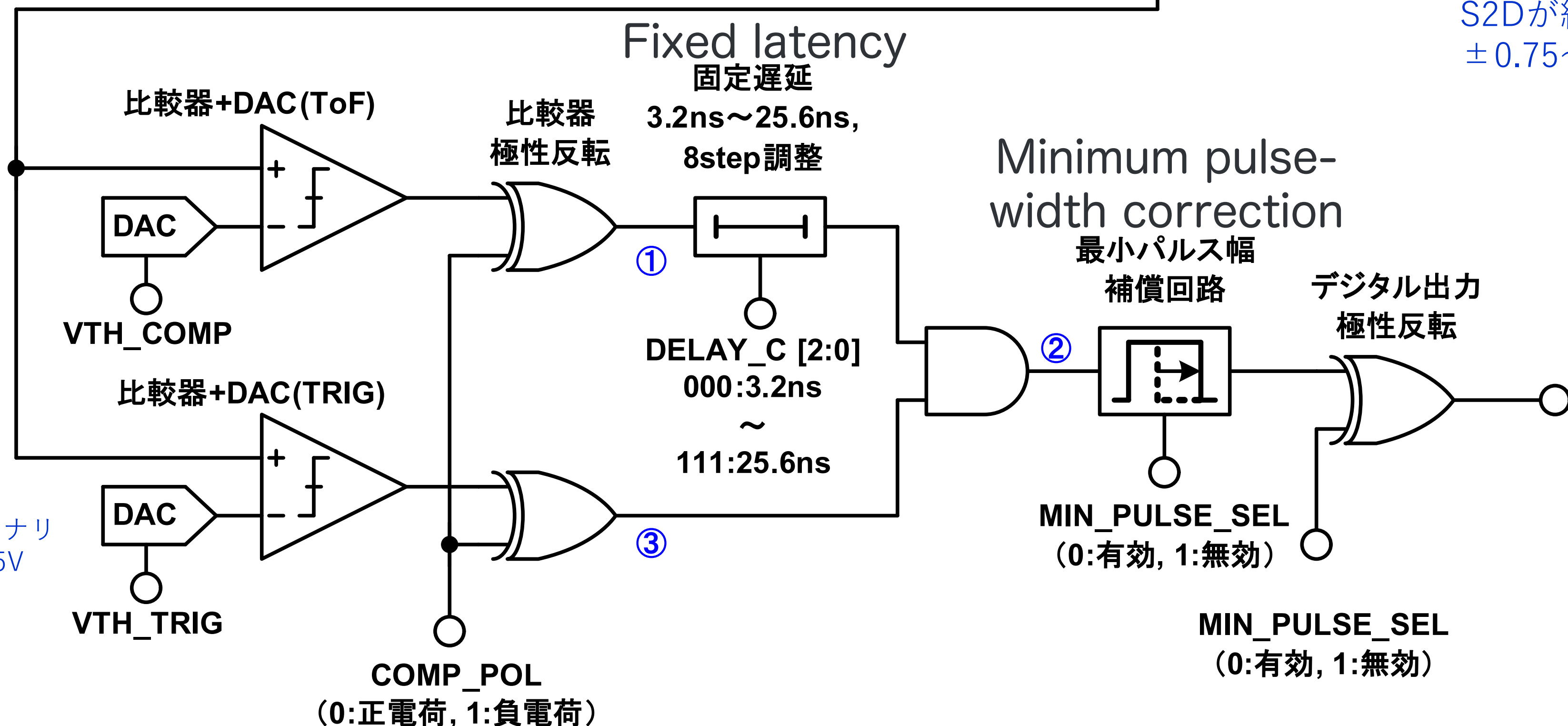
最小パルス幅
補償回路

デジタル出力
極性反転

デジタル
出力
DO#

Digital output

10bit 3.3V
ストレートバイナリ
d512の時に1.65V



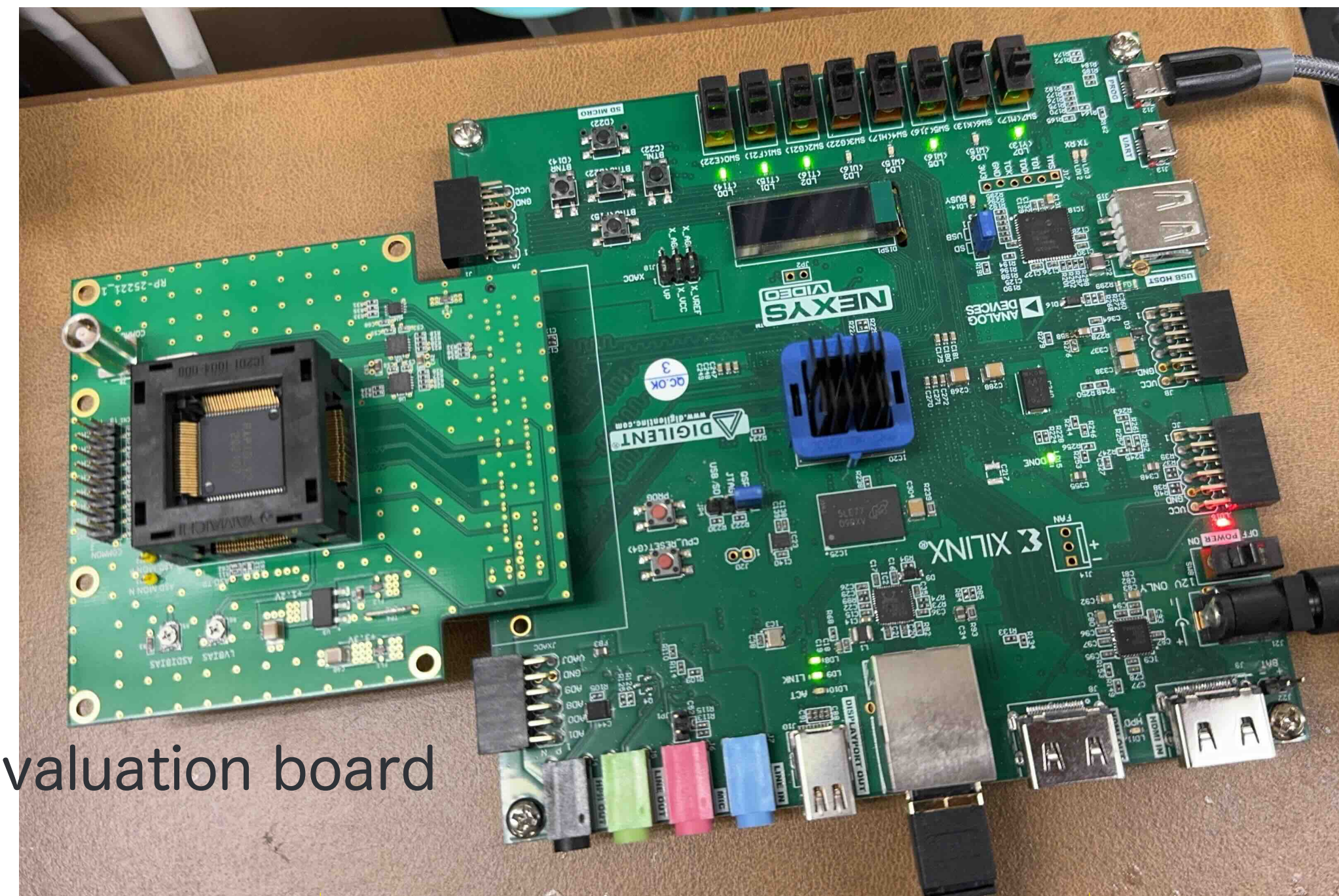
ASIC evaluation board

Current status

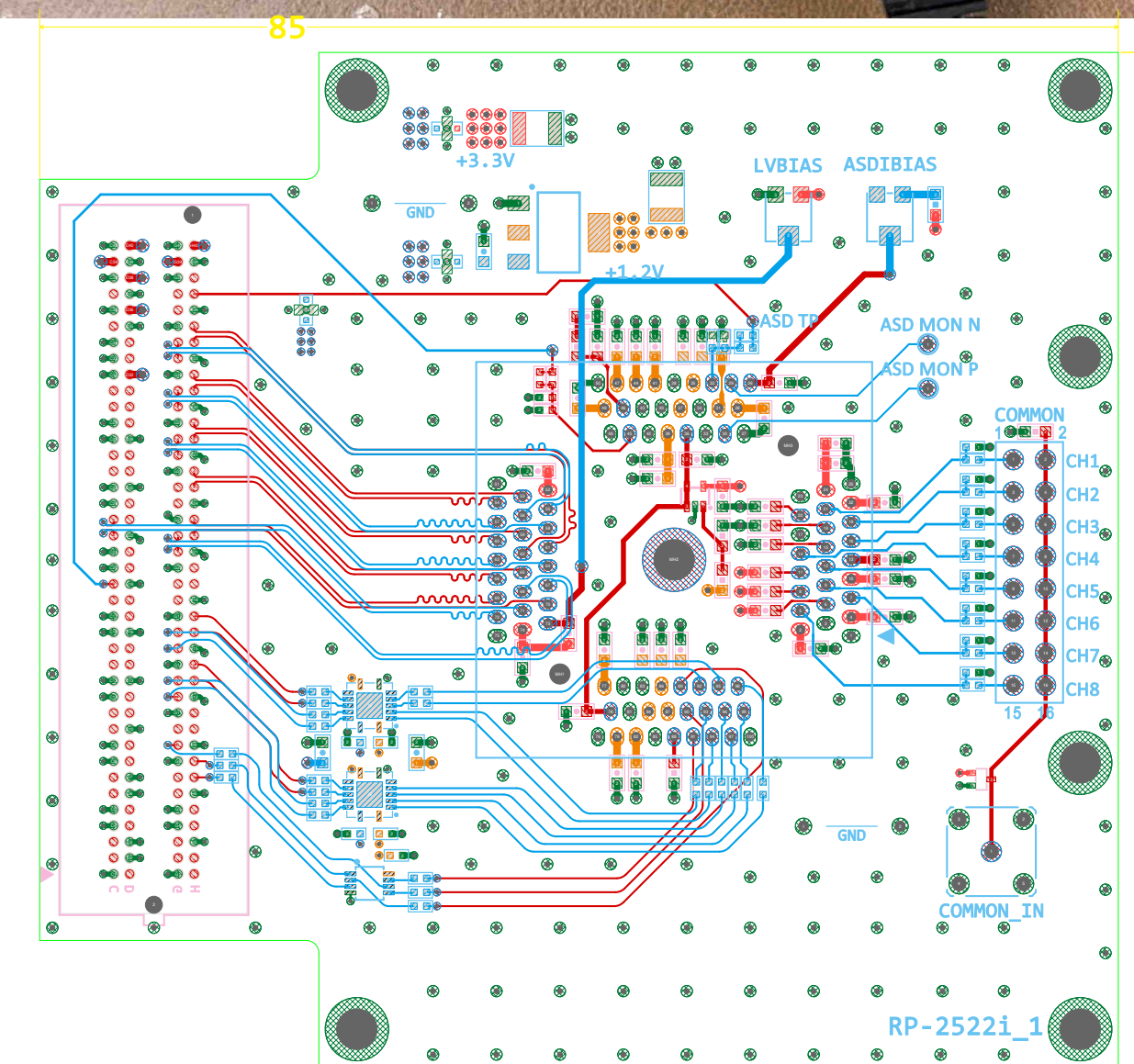
- Evaluation board has already been developed.
- ASIC configuration succeeded.
- [Issue] ADC readout is not stable.
 - The ADC output looks correct using an oscilloscope.
 - According to the developer of ASIC, it may be an ASIC issue rather than the evaluation board
 - It (PLLCTRL) may be sensitive to noise / ground fluctuation.
 - This could be a socket-mount issue on the board.
 - No problem about the ASIC soldered on the prototype module

Next step

- Reconsider whether this issue can be fixed.
- If not, we have to consider how to check the ASICs before mounting on modules.



evaluation board



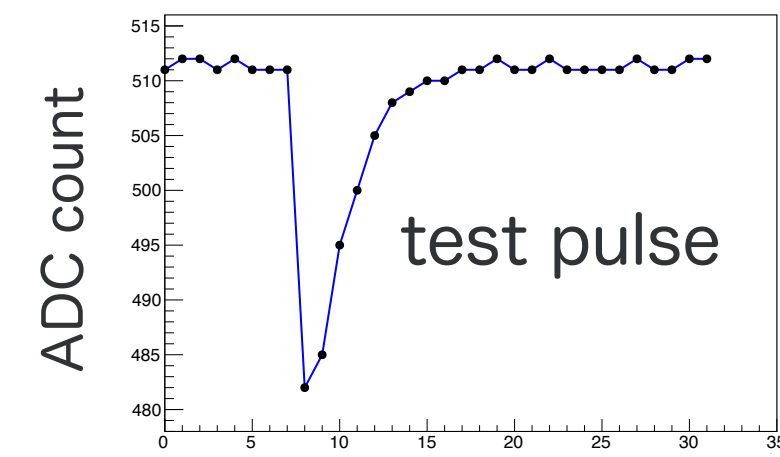
Performance test w/ test chamber

[Threshold scan]

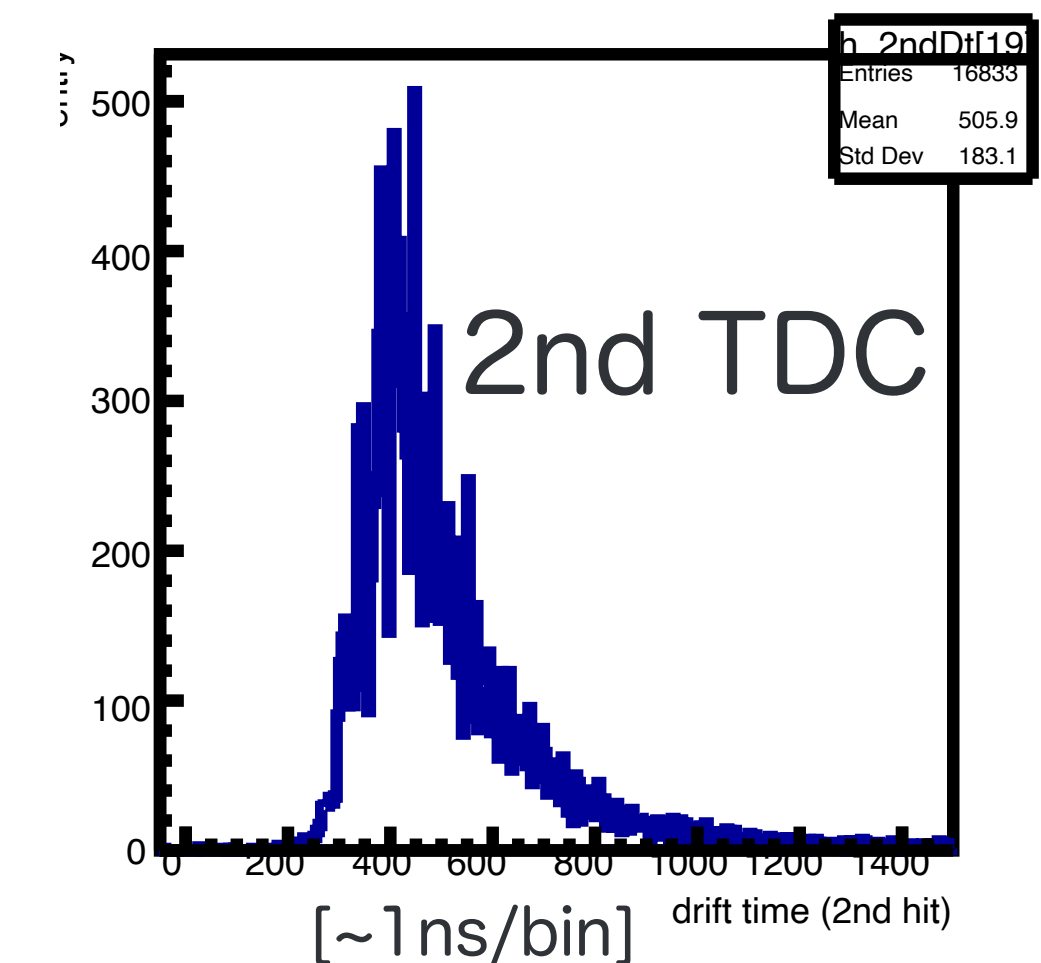
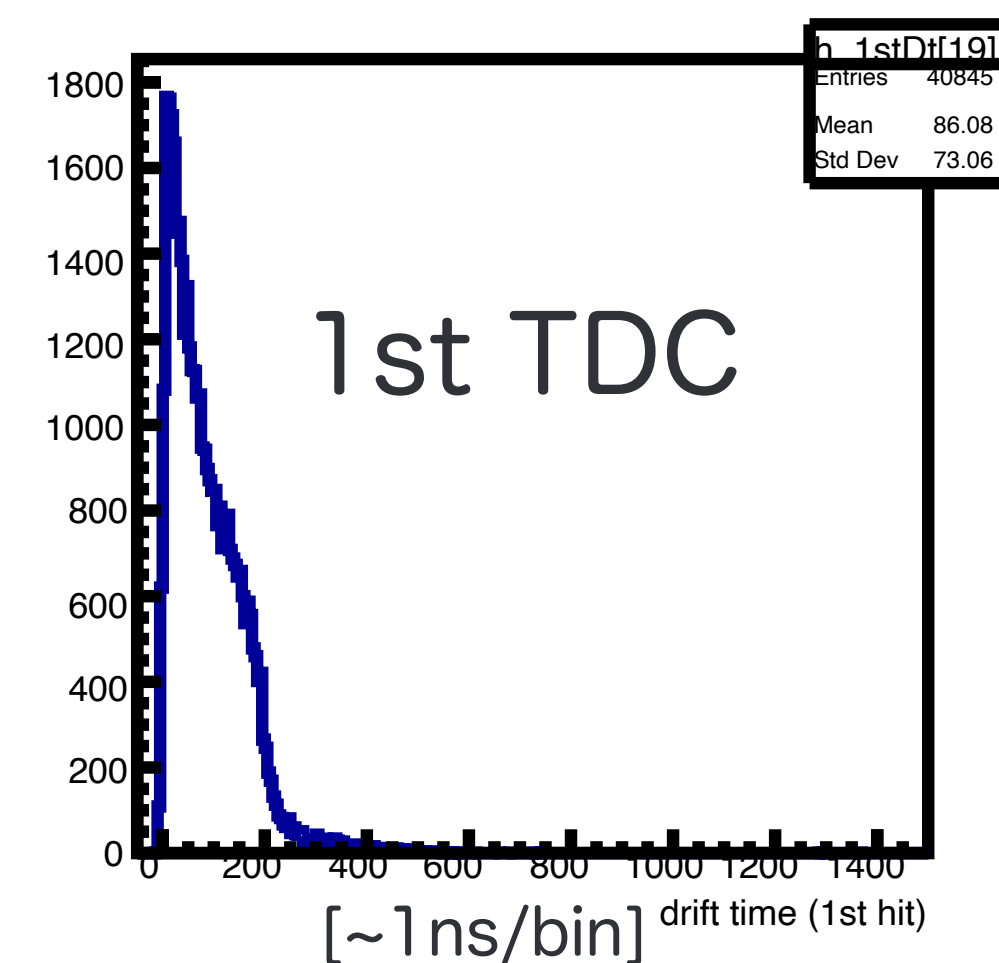
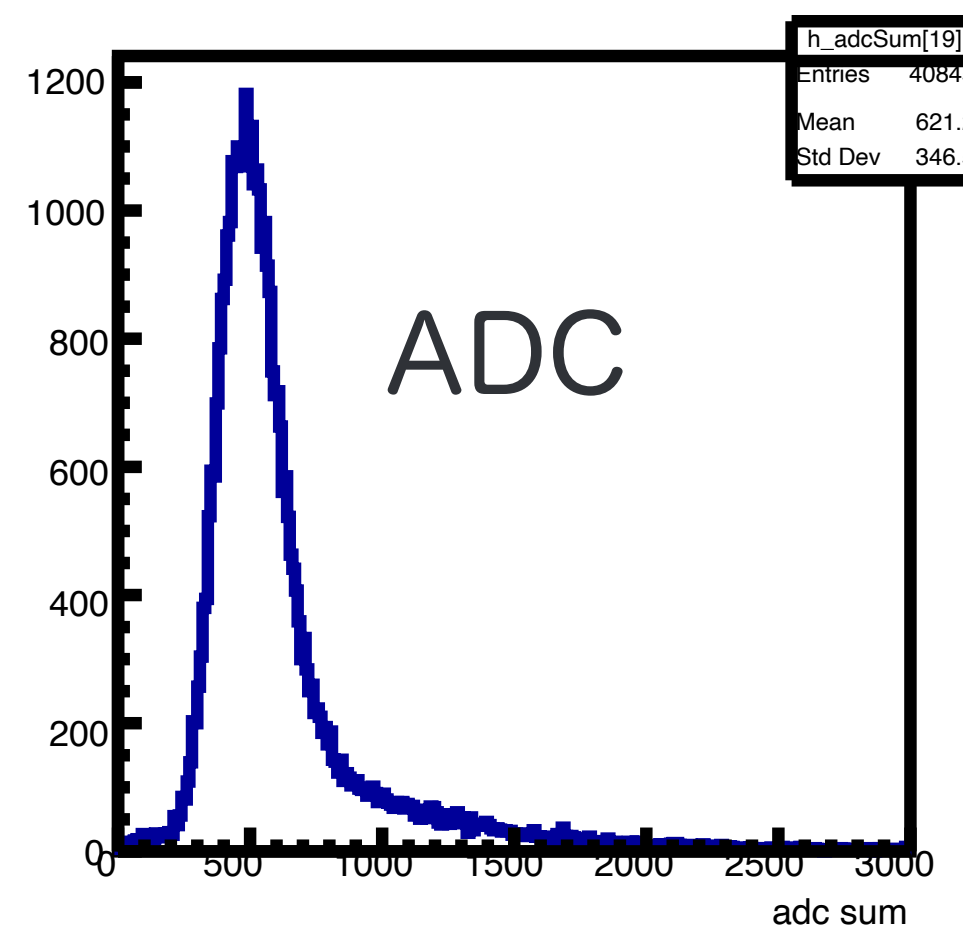
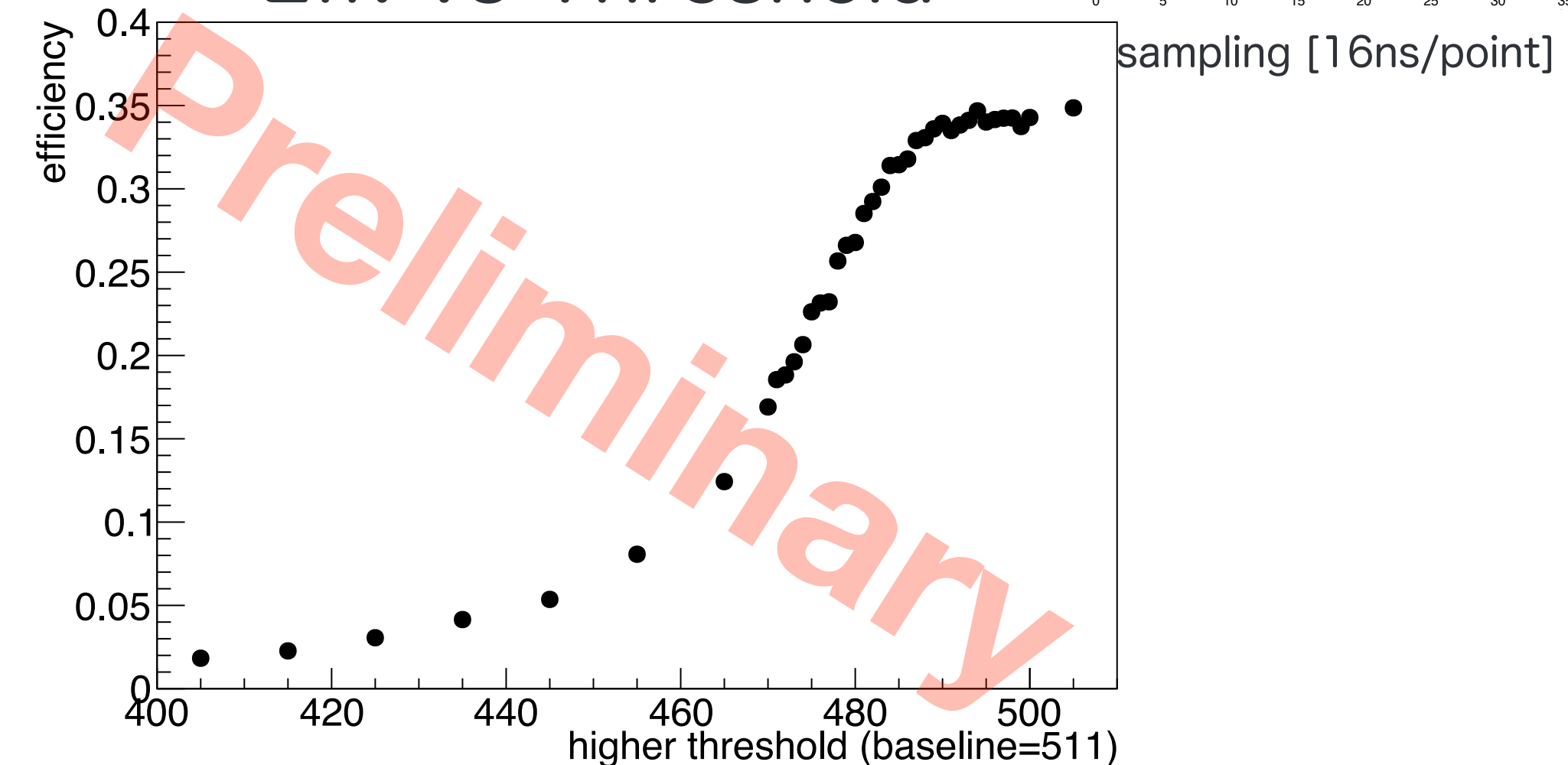
- The threshold for detection (not timing) was changed.
- $\text{eff.} = [\# \text{ of events w/ TDC}] / [\# \text{ of triggers}]$
- The detection efficiency also changes as the threshold value changes.
 $\Rightarrow$ Threshold works as expected.

[Check of general parameters used in analysis]

- No noise ADC peak thanks to the double-threshold scheme
- Reasonable 1st-TDC distribution
- Many 2nd-TDC hits
 $\Rightarrow$ under investigation..



Eff. vs Threshold



Performance test w/ test chamber

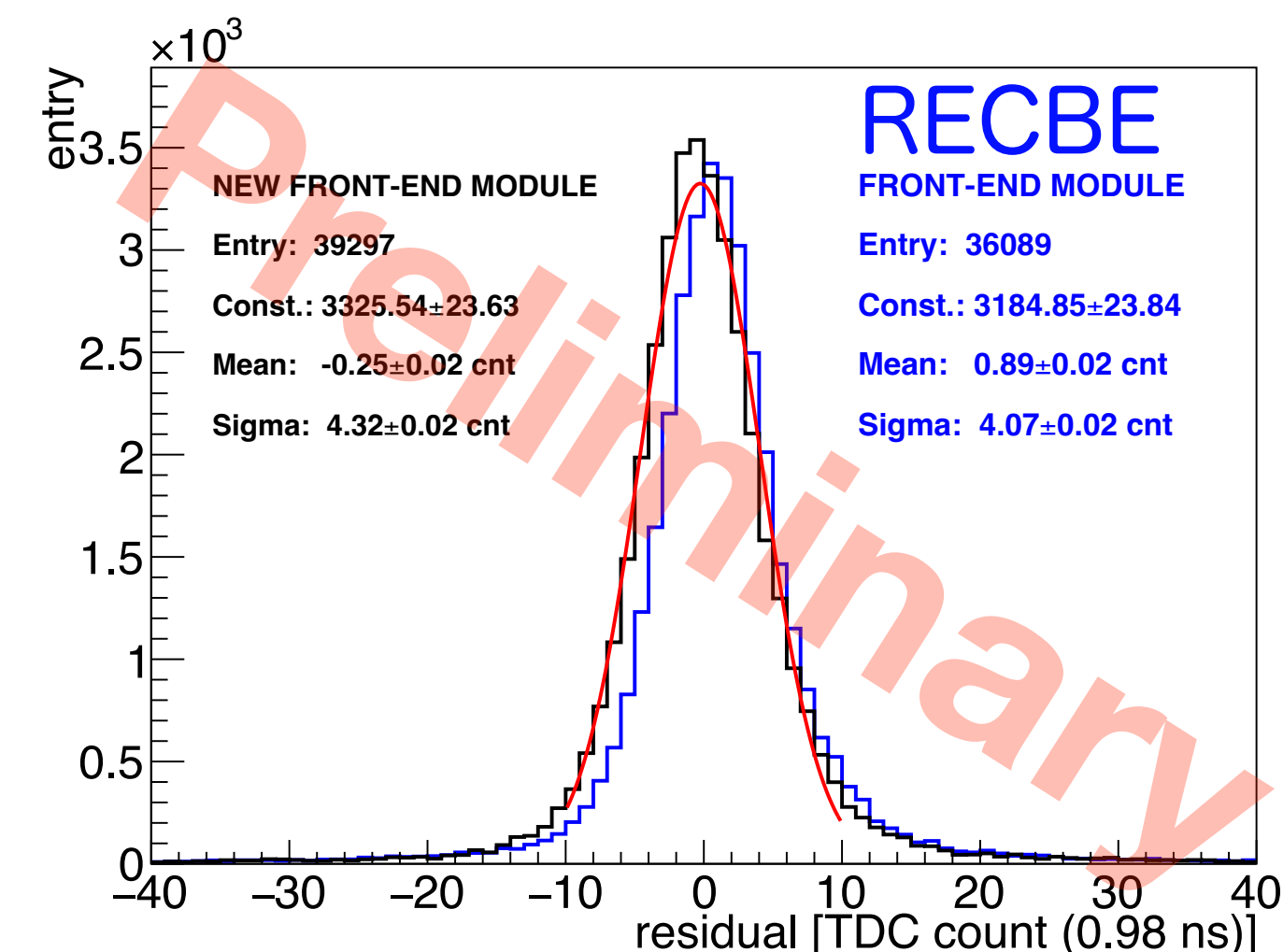
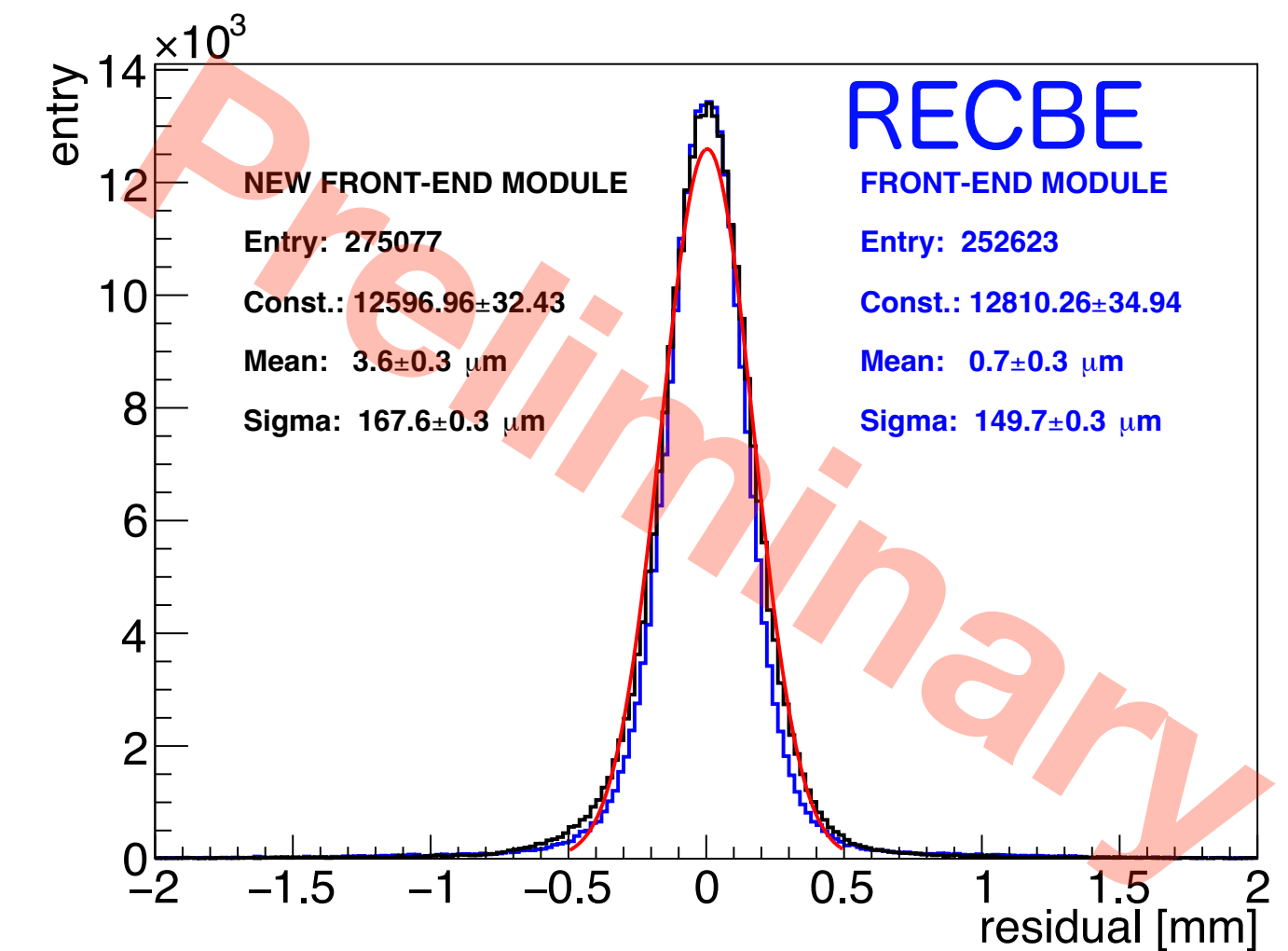
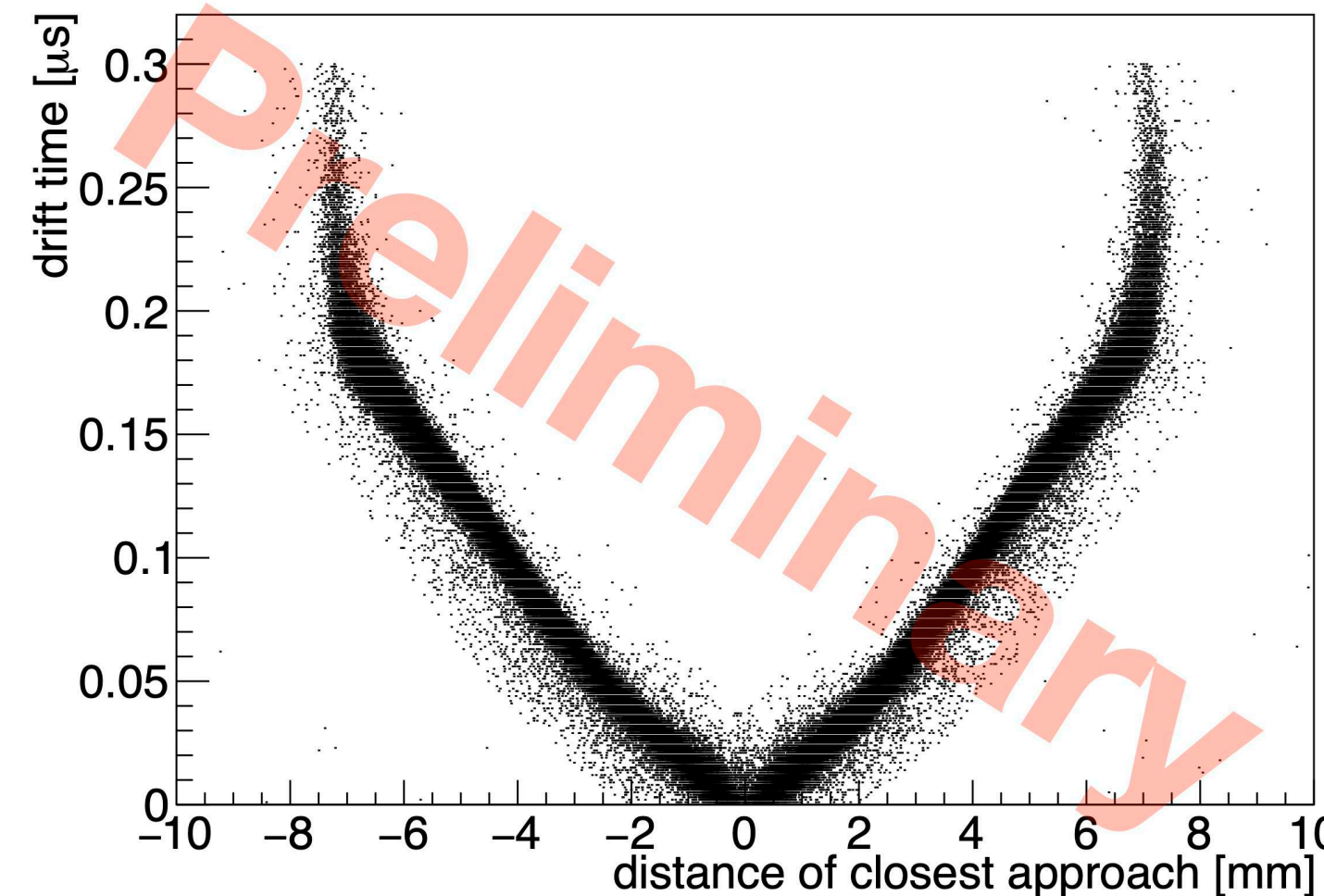
The same tracking code can be applied to RECBE and RECBE Mk-II data. These results are obtained after the 5th iteration of the tracking process.

[Spatial resolution]

- Normal shape of the XT relation
- Worse spatial resolution than RECBE's
 - RECBE Mk-II: $167.6 \mu\text{m}$, RECBE: $149.7 \mu\text{m}$

[Timing resolution]

- $\text{Residual} = (\text{TDC}_{\text{Layer0}} + \text{TDC}_{\text{Layer4}})/2 - \text{TDC}_{\text{Layer2}}$
- Negatively shifted mean value
- A little worse timing resolution than RECBE's
 - RECBE Mk-II: 4.32 cnt , RECBE: 4.07 cnt
 - due to the smaller amplitude for the comparators in ASIC
- I need comments from the tracking group on how much it will affect the physics.
- Parameter tuning for the ASIC amplifiers will be tried.



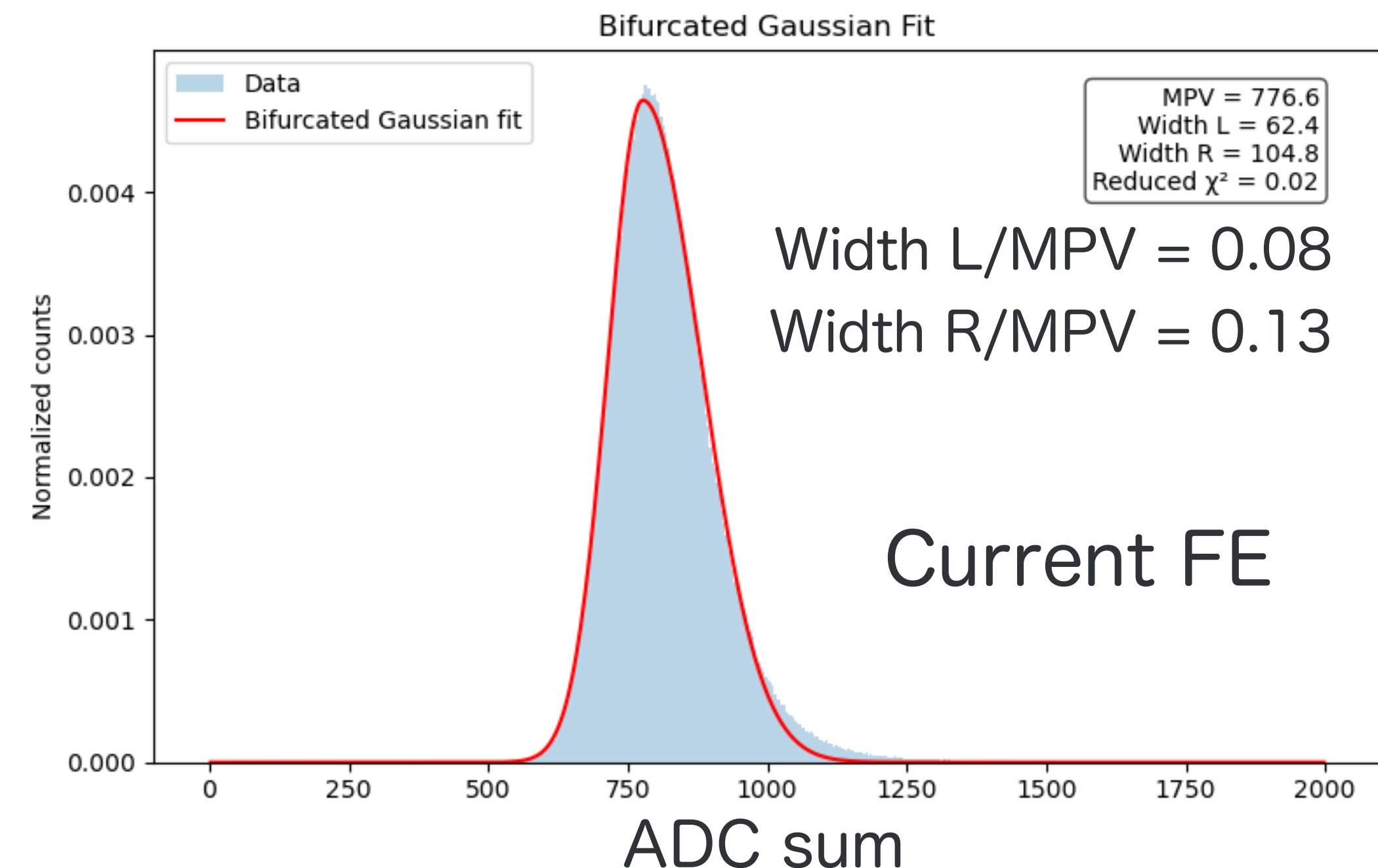
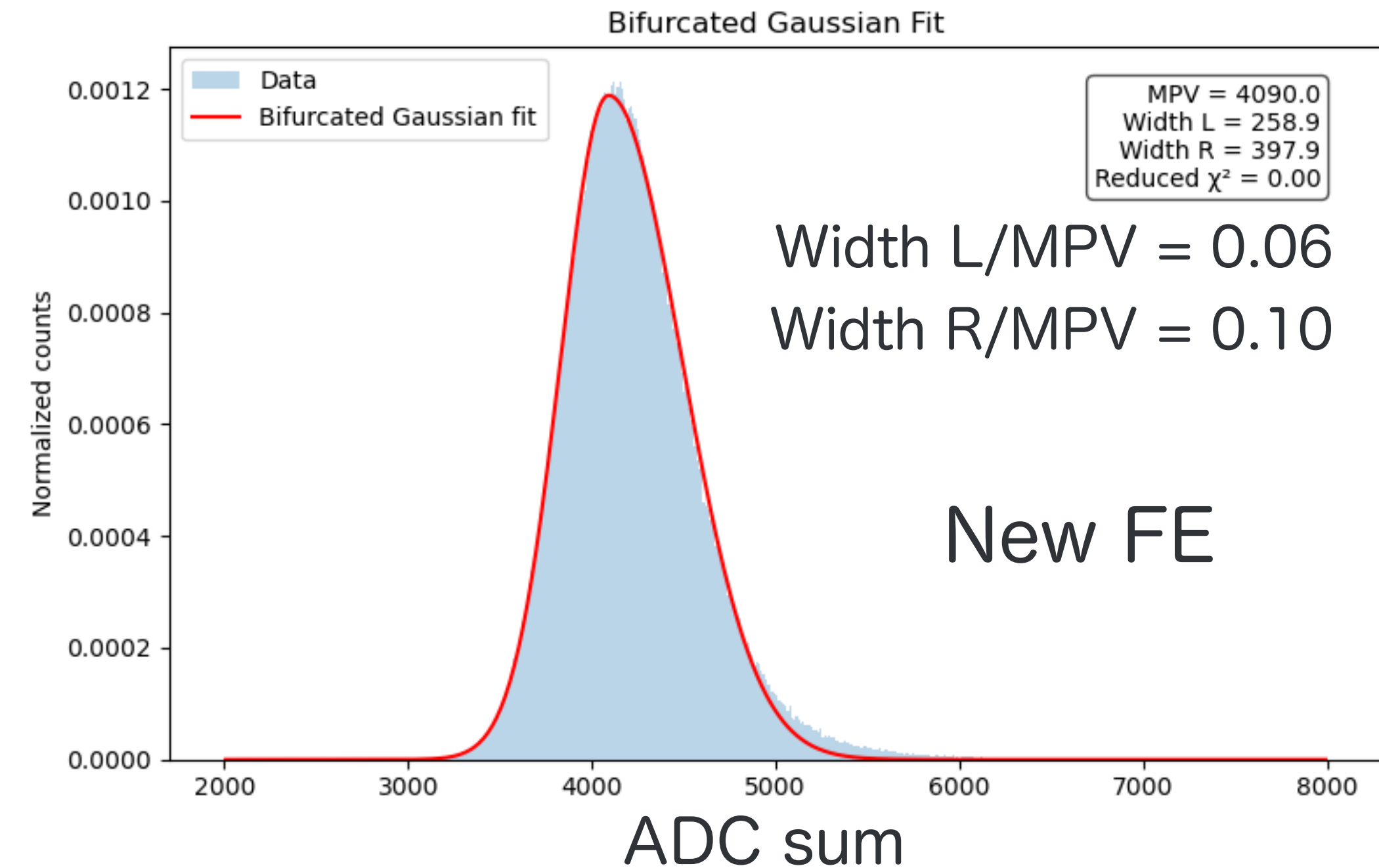
dE/dx resolution

Analysis workflow

- Select events with exactly one hit in each layer
- Compute the ADC sum over a 1-us window
 - Since RECBE records 1 us of data, it sets any samples below the baseline to zero (ignoring undershoot)
- Discard the highest and lowest ADC sums, then sum the remaining ADCs for six layers.
- Normalize the distribution width to its peak amplitude and compare with the current module.
 - Fit the spectrum using a bifurcated Gaussian

Result: new FE exhibits a 30% narrower width

- The reason is still unknown..
(Larger linearity region of ASIC??)



Remaining concerns

Worse spatial resolution than the current FE

- As discussed before

Performance at lower gas gain

- Since the ASIC was designed before the recent discussions on CDC performance, its gain is not taken into account.
- ASIC gain is smaller than the current ASD, so performance degradation is a concern.
- According to the developer, tuning R/C values in the amplifier/shaper may increase the gain by 5-10 times.

Study: evaluate spatial resolution in a tracking study using a test chamber

- [Pre-study] scan R/C and find the optimal settings.
- Check if spatial resolution improves.
- Run with lower HV to reduce gas gain, and then evaluate the performance (not only spatial resolution)
- Schedule: middle or late November if I have time to prepare.

Status of readiness

Circuit desing

- Only minor modifications remain.
- All known changes are listed.

Parts procurement

- All fixed chips have been purchased.
- Parts that might be unnecessary depending on the final FE design have not been ordered.
- ASICs: we need to test.
 - We are still working through issues with the evaluation board.
 - We use a replaceable socket for replacing chips, but with this socket the ADC readout is not stable.

FPGA Firmware development

- Signal-processing logic equivalent to the current firmware has been developed.
- We already tested the firmware running with the current DAQ and TRG (in PocketDAQ).
Once it is integrated, the firmware development will be completed.
- For deployment, we will need to prepare new scripts to configure the ASIC.
- [Task] After fixing the firmware, the power consumption needs to be measured.