CDCTRG Dataflow Upgrade

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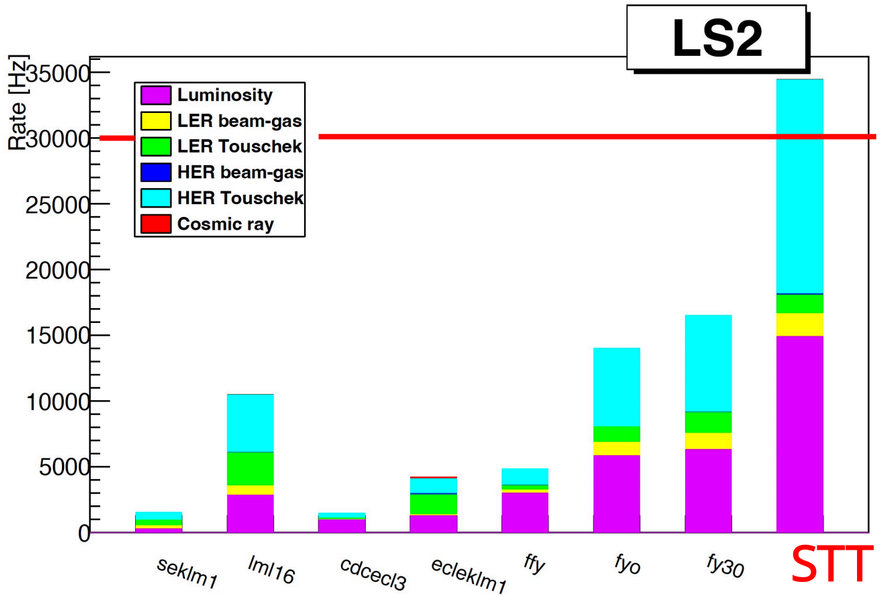
Trigger Rate due to the Beam Background

- Currently, the trigger rate is under the DAQ limit
  - Trigger rate: 5-8 kHz in 2024c
- In the target luminosity ($\mathcal{L} \sim 6\times10^{35}\mathrm{cm}^{-1}\mathrm{sec}^{-1}$), some of trigger bit may exceed the limit
  - i.e., the single-track trigger may be prescaled, which affect the efficiency of Dark Matter or τ events
- A large portion of the beam background (BG) induced CDCTRG rate in the future (~50%?)
  - If we can upgrade the CDCTRG to reduce the BG rate, we may save possible lost in the future!

Target	Trigger condition	Trigger rate ($\mathcal{L} \sim 4.0\times10^{34}$)
$B\bar{B}$ Events	N_{trk}^{2D} >= 2 & N_{trk}^{3D} >= 1	0.3 kHz
	N_{trk}^{2D} >= 2 & N_{trk}^{3D} >= 1 & $\Delta\phi_{2D} > 90°$	0.75 kHz
τ or Dark Matter	3D Neuro track w/ $\lvert\vec{p}\rvert > 0.7$ GeV	2 kHz



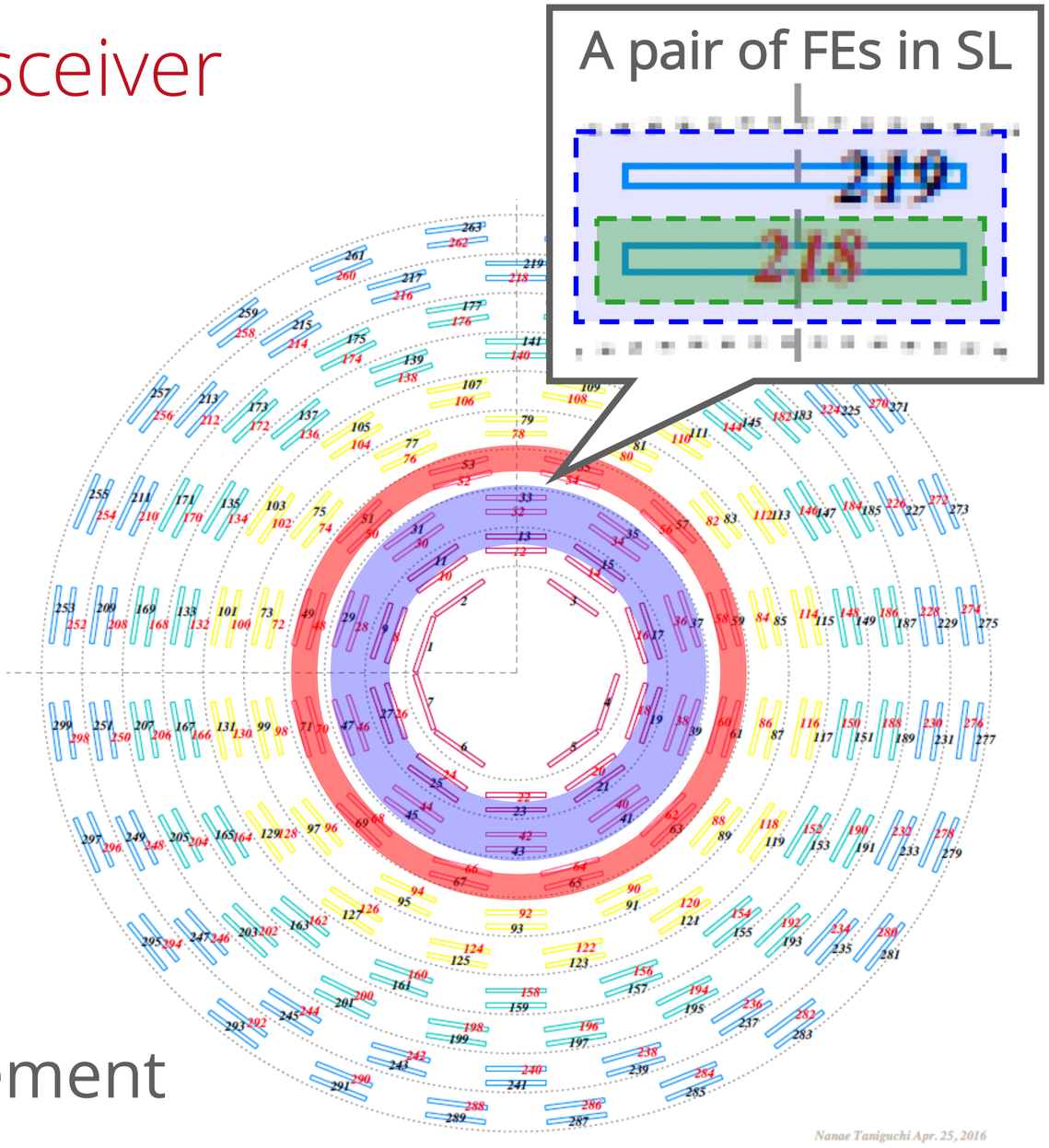
Radiation Damage of Optical Transceiver

- Optical transceiver in the current CDCFE may dead around 2026-2027 due to the radiation

- We suppose three scenarios:
  1. One of FEs in the pairs for SL0/1 is dead
  2. Both of FEs in the pairs for SL0/1 are dead
  3. FEs after SL2 is dead

- Impact in CDCTRG efficiency:
  1. Mitigatable by channel masking (Koga's slide)
  2. Degradation about 1% per one pair
  3. **Significant degradation may be present**

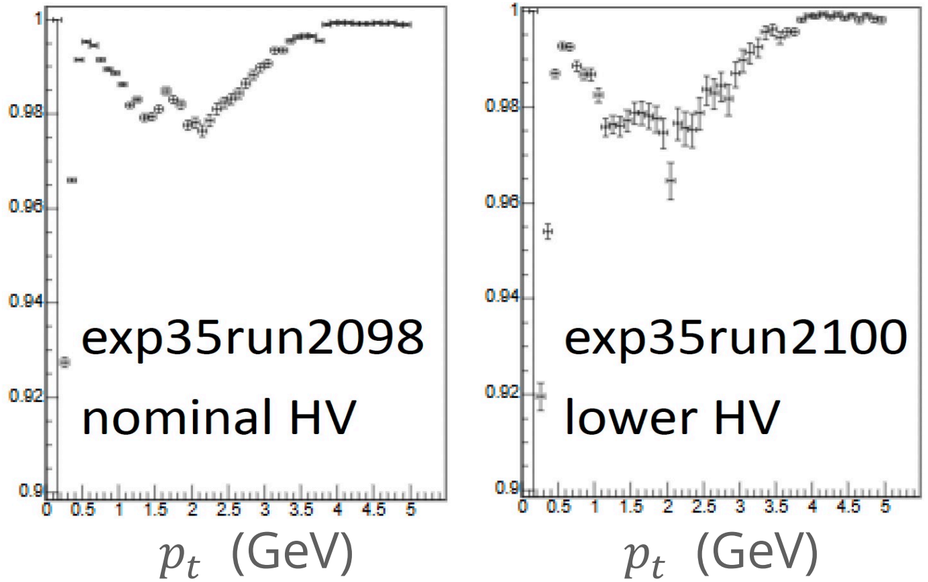
👉 First priority plan to implement



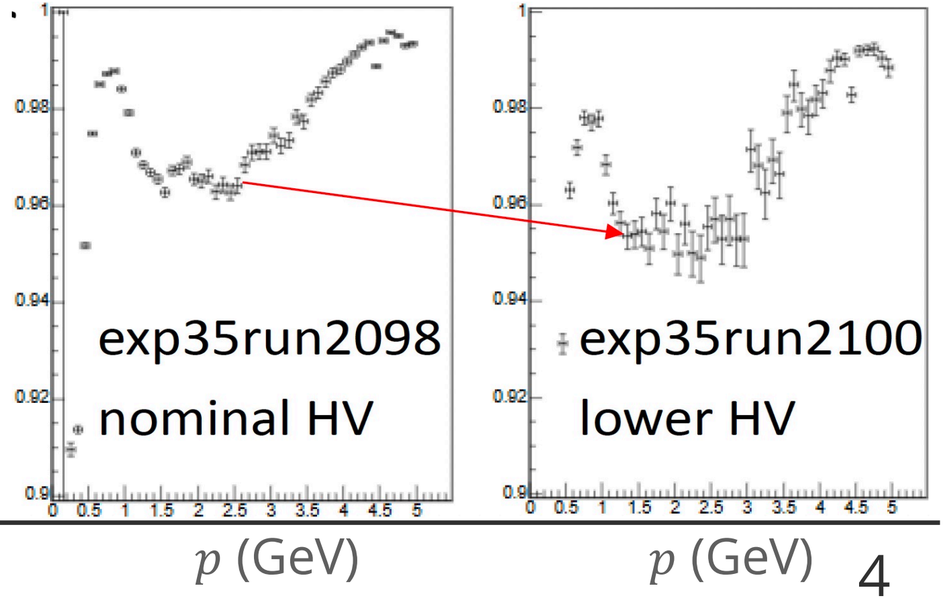
Trigger Efficiency with Lower CDC HV

- The CDC team tested the lower voltage for the CDC HV in 2024c (Y. Nakazawa's Slide)
- The rate of Track Segment detection from SL0 decreased by 30%
- No significant degradation (< 1%) in the 2D efficiency
- The 3D efficiency degraded by ~2%
- There are no critical effects of radiation damages for now, but the countermeasure may be needed

2D Track Efficiency

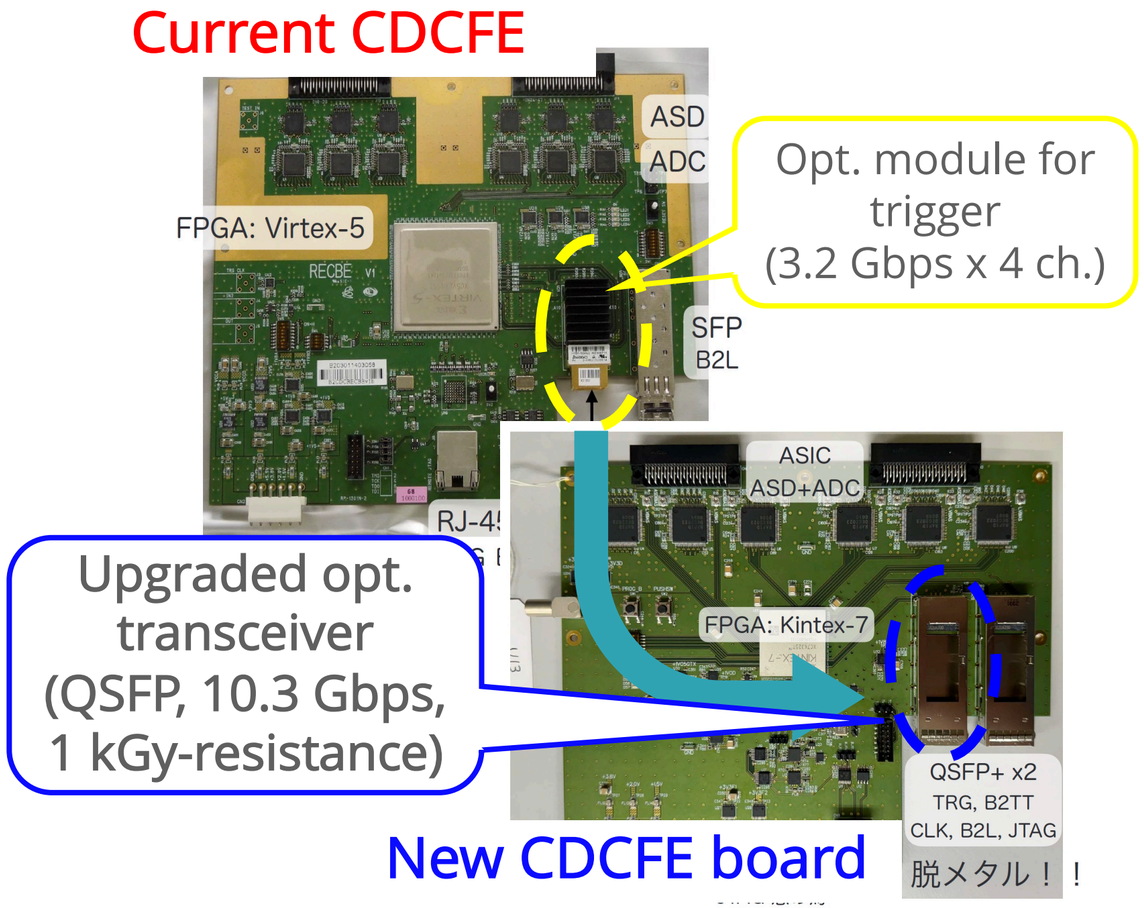


3D Track Efficiency



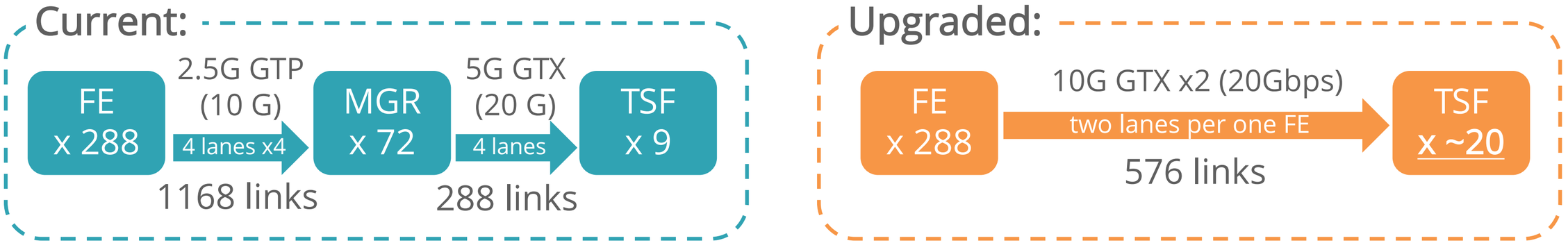
Upgrade of CDC Frontend Electronics

- RECBE-2 will have improved components
  - Optical transceivers and ASICs for ADC
- Improvements of the new QSFP modules:
  - Bandwidth for CDCTRG: **3.2 → 10.3 Gbps**
  - Discontinued product → **Common modules**
  - 1-kGy radiation hardness: **10-year** operation (Tested with gamma and neutron rays)
- Improved ASIC will provide ADC counts with shorter latency (300 ns reduced)
  - Latency budget for CDCTRG loosen
  - Double-threshold functionality: Reduce noise and time-walk jitters



Upgrade on Datapath of CDCTRG

- We will upgrade CDCTRG with the new datapath to utilize the high speed of new FE
  - Main plan: Remove Mergers (MGR) and connect FE ↔ Track Segment Finder (TSF) module directly



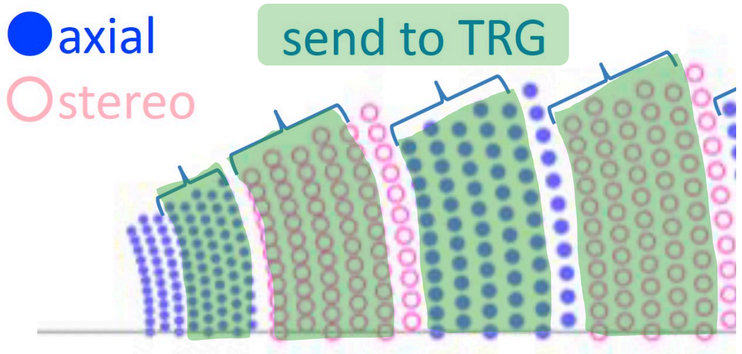
  - Number of the TSF modules: 9 → 18~20 modules (UT4 modules for those are ready)
  - Lane conf.: 4 lanes for CDCTRG → 2 lanes for CDCTRG and 1lane for B2L (1 lane for spare)

- Expected improvements:
  - The number of bits from one CDCFE per a 32-MHz clock: **320 bits → 512 bits**
  - Latency reduction: 600 ns expected

Current Inputs for CDCTRG

- Currently, only part of CDC hit information is sent to TSF

Hit existence



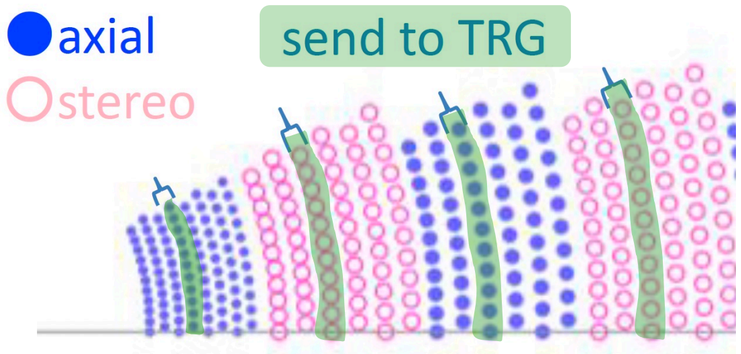
- Indicates hits in a wire
- Accounts 5 layers from 1 SL (covers only ~80%)

ADC

$$\sum_{i}^{i+3} \boldsymbol{ADC(i)} > threshold?$$

- Indicates exceeding the thresholds in frontend
- Summation of ADC of ~3 points for part of wires

TDC

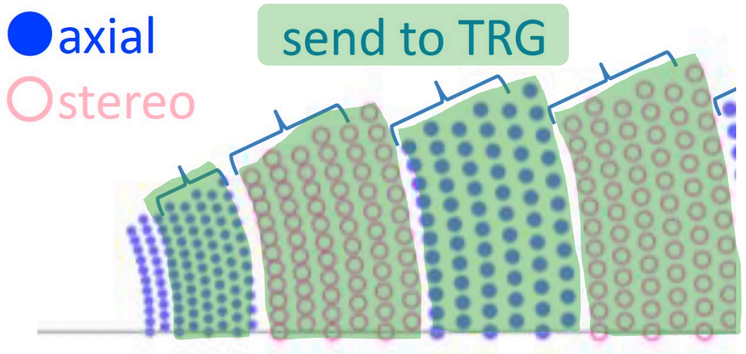


- Receives TDC with 2ns resolution from 2 layer (covers only ~30%)

Inputs with Improved Bandwidth

- If the bandwidth from CDCFE is doubled, we can upgrade the information as follows:

Hit existence



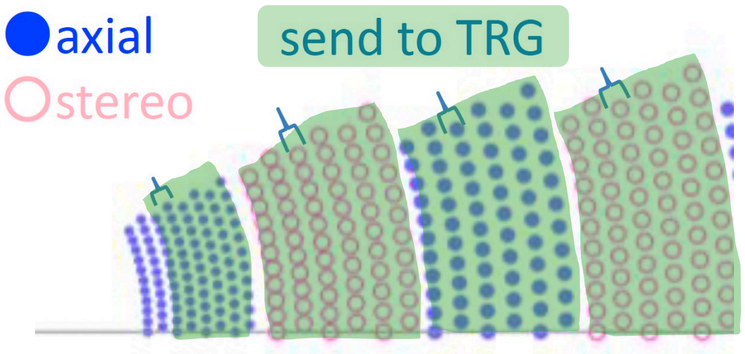
- Coverage: 5 → 6 layers
- Some innermost wires in SL0 is unclear

ADC

$$\sum_{i}^{i+n} \boldsymbol{ADC(i)} = \text{16-step values}$$

- Summation over all wires
- Window for summations may be enlarged
- Resolution: 4 bits

TDC



- Sending all wires with 2ns resolution

Tentative Bitmap Design

- The upgraded optical link can contain all the upgraded inputs

Figure 10: Part of CDC outer SL inside wire cell configuration [6].

Current

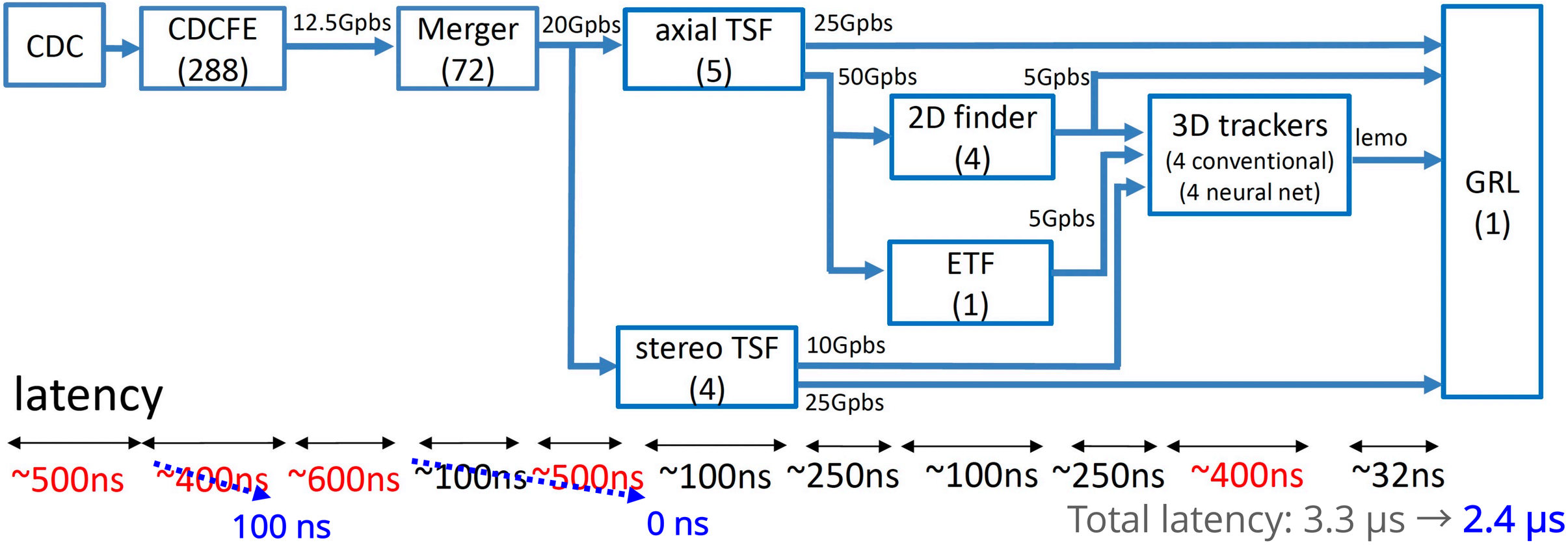
Input data	Bits from one CDCFE per 32-MHz clk.
Hit existence map (5 lyr.)	48 bits
ADC threshold flag	1 bit x 48 wires
TDC count of 1 layer	5 bits x 16 wires = 80
The fastest TDC count in the track segments	5 bits x 16 segments = 80
Edge information	10 bits
Clock counter	9 bits
Total number of bits	275 bits (< 320 bits)

Upgraded

Input data	Bits from one CDCFE per 32-MHz clk.
Hit existence map (all lyr.)	48 bits
TDC count of all layers	5 bits x 48 wires = 240
ADC sum. of all layers	4 bits x 48 wires = 192
Clock counter	9 bits
Total number of bits	489 bits (< 512 bits)

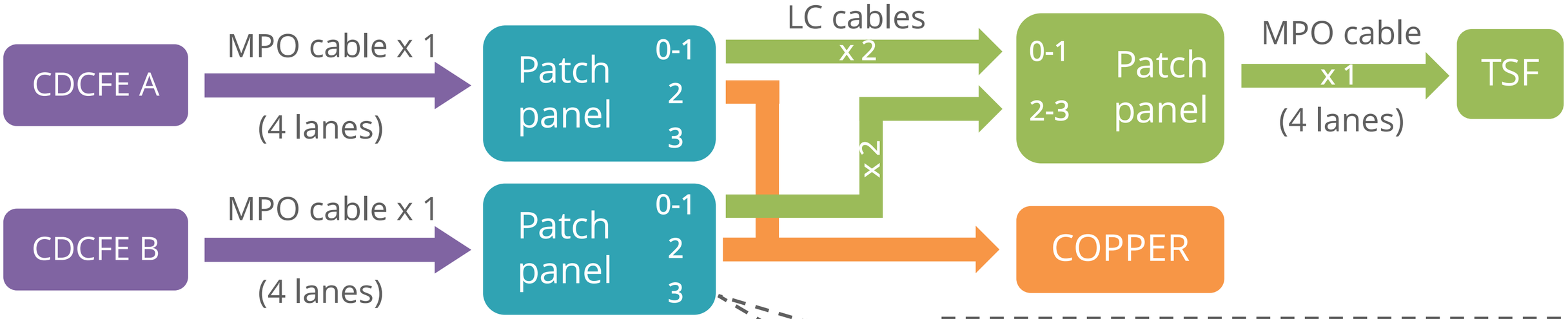
Latency Improvements

- We expect we can reduce CDCTRG latency by ~1 μs by the CDCFE upgrade
  - More accurate CDCTRG logic will be available (e.g., more complex NN or Hit cleaning w/ GNN)



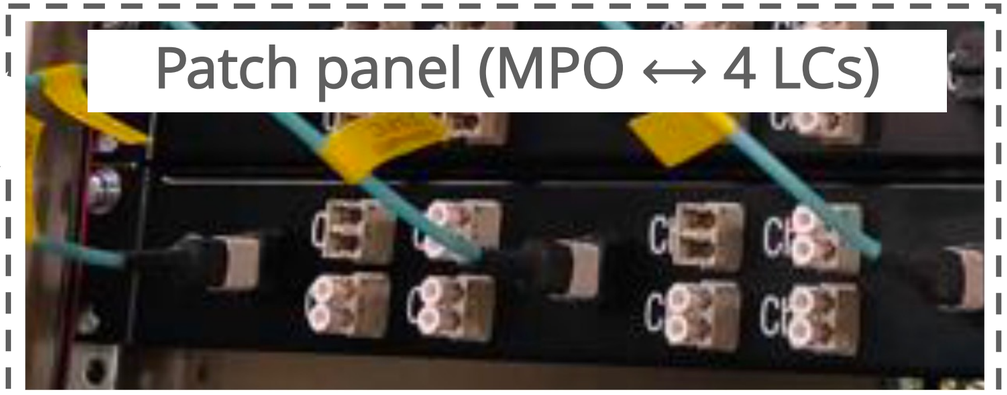
Cabling Design and Material Demands

- Example design for the cabling configuration for the upgraded CDCFE ↔ CDCTRG



- Cable and patch panel demends

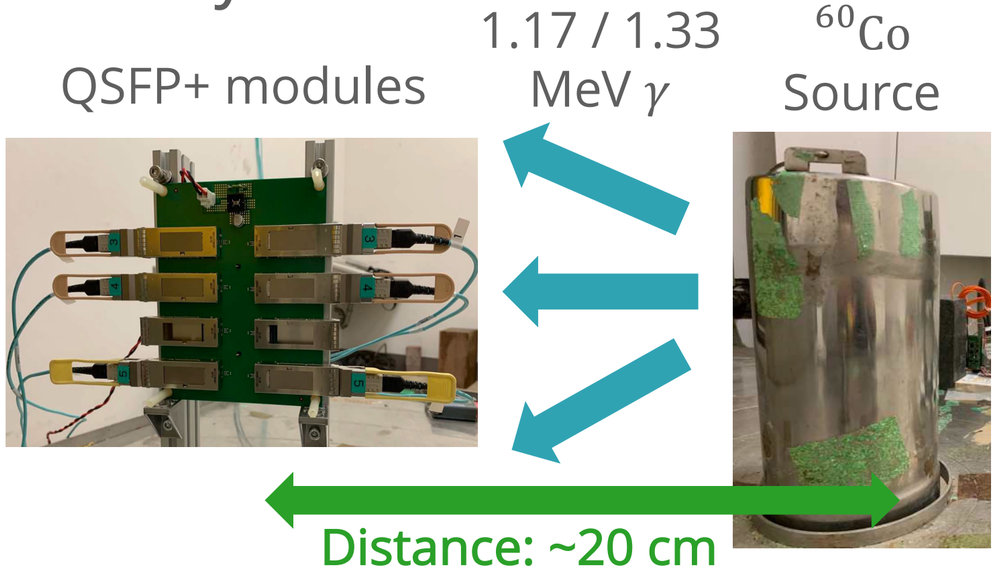
	CDCFE (MTP cables)	Patch panel (MTP to 4 LCs)	LC cables	Patch panel (4 LCs to MTP)	TSF modules (QSFP trans.)
Total #	288	288 ch.	864	288 ch.	~20
Remark	Length: $\mathcal{O}(10)$ m	4 MTP ch. in 1 panel	Length: $\mathcal{O}(1)$ m	4 MTP ch. in 1 panel	5-12 QSFPs in 1 module



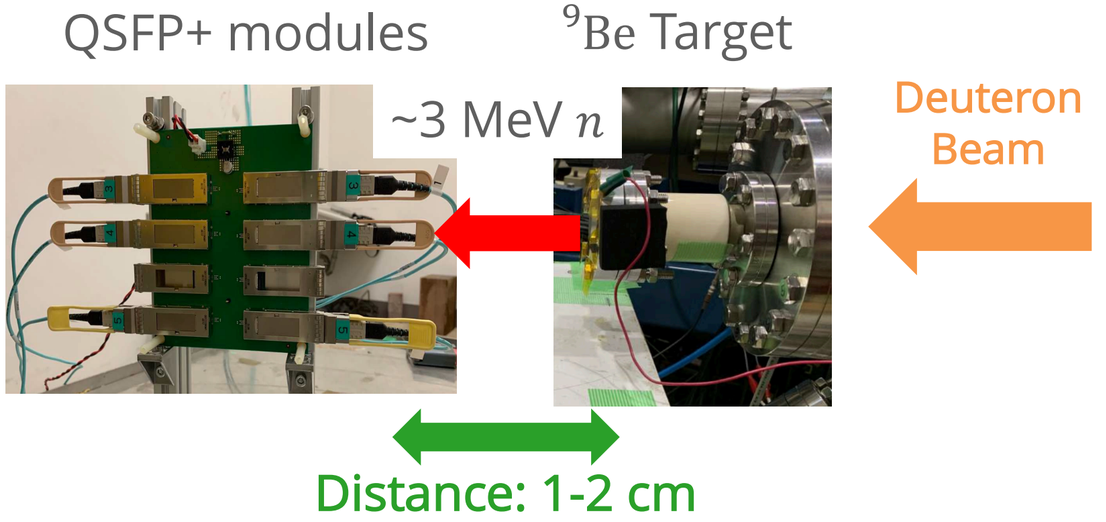
Radiation Hardness for New FE

- We tested the radiation resistance of the QSFP modules for the new CDCFE
- Target radiation: γ-rays from $^{60}\mathrm{Co}$, n-rays from $^{9}\mathrm{Be}(d,n)$ from a deuteron accelerator
- Test items: Radiation tolerance of products and the lot-number dependencies
- Selected item: Dell-compat. QSFP-SR4-40G
  - Dose: 1.2-1.5 kGy for γ and 10^{12} for 1 MeVeq.-n (equivalent for the 10-year operation)
  - 714 transceivers have been purchased (Goal stock: 700)

Gamma-ray tests



Neutron-ray tests



Long-term Schedule

- 2024 – Early 2025: Trigger rate analysis with the latest dataset
  - What does make Beam BG-induced trigger rates? fake tracks? off-IP tracks?
  - We use the result from this analysis to decide upgrade items for CDCTRG

- Mid 2025-2026: Preparation of the TSF firmware for new scheme
  - Confirming the bitmap from CDCFEs and upgrading TSFs
  - Goal: Make TRG ready against the optical transceiver breaking
    (If Belle II decided to change CDCFE to the new one, we should be able to deal with it)

- 2025-: Upgrading the CDCTRG logic (Adding Hit-filtering using GNN, DNN, etc...)
  - Based on the beam background study result, we will devise new logic or upgrades for CDCTRG
  - The design for the new TSF should be flexible for upgrades of later modules
    (Original author left Belle II, poor FW design for the high-speed transmission, etc...)

Summary

- Motivation:
  - The rate of some CDC trigger condition may exceed the 30 kHz limit in the future
  - The CDC will upgrade front-end electronics w/ improved opt. transceivers and ADC chips
  - Performance degradation due to the radiation damages must be considered

- Upgrade contents:
  - FE and dataflow upgrade will enable CDCTRG to utilize more large bits per clock (320 → 512 bits)
  - The inputs for CDCTRG can be improved a lot: Covering all layers, sending ADC sum, and so on…
  - Radiation hardness is enough to operate for 10 years with the Belle II radiation condition

- Plan:
  - I will investigate the source of CDC trigger rate, and upgrade TSF firmware to the new version
  - CDC Hit-filtering using GNN, Neural Network 3D-Trackers, and so on is ongoing
  - Retaining the efficiency in the future is the most important item, we will do our best for this

Backup Slides

Gamma Irradiation Test: Results by Models

- We tested various models for the modules. Two modules meet our requirements
  - Considering the selling agencies, we selected the **Dell-compatible model from FS.com**

Model & Manufacture	Sample pair number / Lethal dose					Resistance at least
	#1	#2	#3	#4	#5	
FiberJapan 8515	500 (PC)	650	1400 (PC)	1300 (PC)	1500 (PC)	> 400 Gy
FiberJapan 85-015	1400 (PC)	1300 (PC)	1100 (PC)	1256 (PC)	1200 (PC)	> 1000 Gy
FS.com FS compatible QSFP-SR4-40G	500 (PC)	400 (PC)	500 (PC)	400 (PC)	400 (PC)	> 300 Gy
FS.com Dell compatible QSFP-SR4-40G	1300 (PC)	1400 (PC)	1300 (PC)	1200 (PC)	1200 (PC)	> 1100 Gy
FS.com Cisco compatible QSFP-SR4-40G	1000 (PC)	1190 Survived	Not tested			> 900 Gy
FS.com Avago compatible QSFP-SR4-40G互換	1000 (PC)	1156 Survived	1300 (PC)	1200 (PC)	1300 (PC)	> 900 Gy

- Color of figures indicates the dose rate (100 Gy/h and 200 Gy/h)
- (PC) means the corresponding sample dead after the power-cycle
- In the (PC) case, we consider the dose in the previous successful power-cycle as the final resistance as a conservative approach

Gamma Irradiation Test: Results per Lot-Numbers

- We performed another test to check the dependency of the lot numbers.
  - The module model is “Dell compatible QSFP-SR4-40G” from FS.com
- Three module pairs from two different lot number has been tested
  - Dose rate and total dose: 40 Gy/hour for 32 hours: 1280 Gy

- Result: No significant variations and all pairs from the both lot numbers can meet our requirements.
  - Some pairs showed unstable link status during the test, but after power-cycling at the end of test, all modules established the stable link!

Lot. No. of Dell-compatible QSFP-SR4-40G modules	Sample pair number / Lethal doses			Resistance at least
	#1	#2	#3	
CG2409245468	> 1280 Gy	1200 Gy	1200 Gy	1200 Gy
CG2408268338	1200 Gy	1100 Gy	1200 Gy	1100 Gy

Neutron Irradiation Test: Results

- As we considered the optical transceiver is not affected much by the neutrons, we tested two pairs of the optical transceiver
  - The module model is “Dell compatible QSFP-SR4-40G” from FS.com

- We irradiated 10^{12} neutrons to the module, and there were **no optical link instability during the test**.
  - The module was normal after the irradiation test.

- The both modules **meet our requirements** for the resistance against the neutron rays