Belle II Trigger/DAQ Workshop 2025

Thursday 23 October 2025

Upgrade - □□□□□□ (Large seminar room) (16:15 - 19:05)

time	[id] title	presenter
16:15	[181] CDCFE upgrade	
16:45	[182] CDCTRG upgrade	
17:05	[183] CDCTRG logic upgrade	
17:25	[184] ECL shaper DSP upgrade	
17:55	[185] ECLTRG upgrade	
18:15	[186] ECLTRG logic upgrade	
18:35	[187] VTXTRG	

Friday 24 October 2025

Upgrade - □□□□□□ (Large seminar room) (10:15 - 12:15)

time	[id] title	presenter
10:15	[188] UT5	
10:35	[189] CEF, AI	
10:55	[190] Latency budget discussion	
11:15	[191] FTSW4	
11:45	[192] Level3 trigger	

Upgrade - □□□□□□ (Large seminar room) (13:15 - 15:45)

time	[id] title	presenter
13:15	[193] PCIe400	
13:45	[194] Haardware HLT: GPU	
14:15	[195] Hardware HLT: FPGA	
14:45	[196] Anomaly detection by machine learning	
15:15	[197] Discussion	