Benchmarking the FTSW4.1 Board

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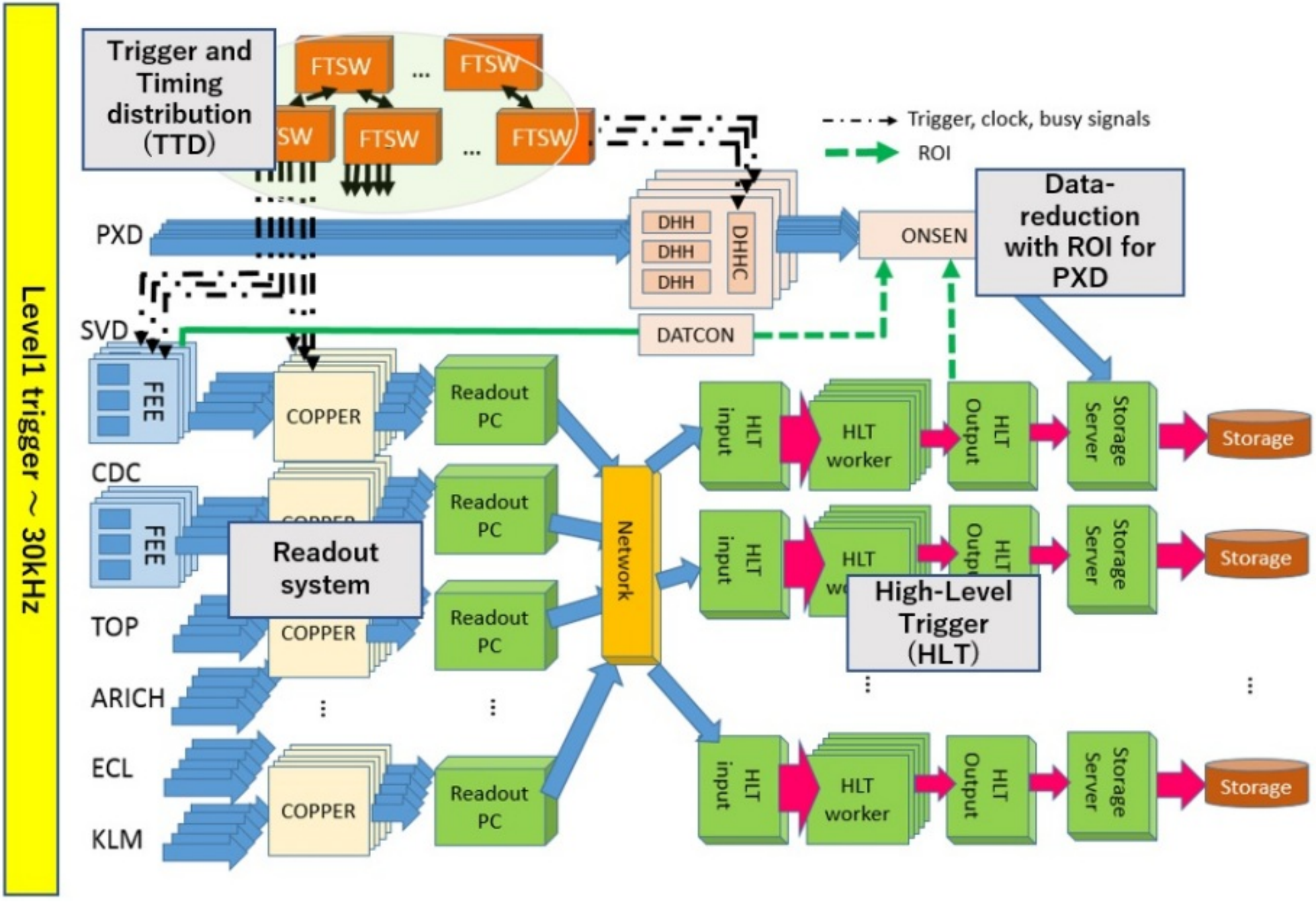
Project Introduction

- **Objective** – Develop firmware to benchmark, or rather, test the various functions of the FTSW4.1 boards to be implemented into the Belle2 experiment by 2027 (hopefully)
- **Duration** – July 1, 2025 to August 22, 2025
- **Software** – VHDL through ISE 14.7 Design Suite (including iMPACT), VSCode, PicoSample 4
- **Setup** – Initial attempts to setup ISE 14.7 on Linux (WSL) and dual boot ended disastrously, so ended up using Oracle Virtual Machine running Linux. Documentation on github.
- Key tools and hardware:
  - FTSW3 & FTSW4 boards
  - Tektronix TDS 3034B and PicoScope 9404-16 Oscilloscopes
  - Matsusada Power Supply
  - USB to JTAG cable
  - Optic fibre cables, QSFP modules (QSFP-SR4-40G)
  - CAT7 cables


Level1 trigger ~ 30kHz
Trigger and Timing distribution (TTD)
FTSW
FTSW
FTSW
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FTSW
Trigger, clock, busy signals
ROI
PXD
SVD
CDC
TOP
ARICH
ECL
KLM
DHH
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ONSEN
Data-reduction with ROI for PXD
DATCON
FEE
FEE
COPPER
COPPER
COPPER
Readout system
Readout PC
Readout PC
Readout PC
Readout PC
Network
HLT input
HLT worker
HLT Output
Storage Server
Storage
High-Level Trigger (HLT)

Trigger and Timing System Overview

Level-1 Trigger (L1):

- Hardware-based trigger system
- Reduces event rate to 30 kHz (aim, current rate is around 20 kHZ)

Need for Synchronization:

- Event-level correlation across subsystems
- Accurate distribution of trigger + time info

Trigger Timing Distribution (TDD):

- System-wide clock to FEE, readout (PCIe), trigger boards
- Run number, trigger type, event number, timestamp to FEE
- Injection veto and revolution signal broadcast

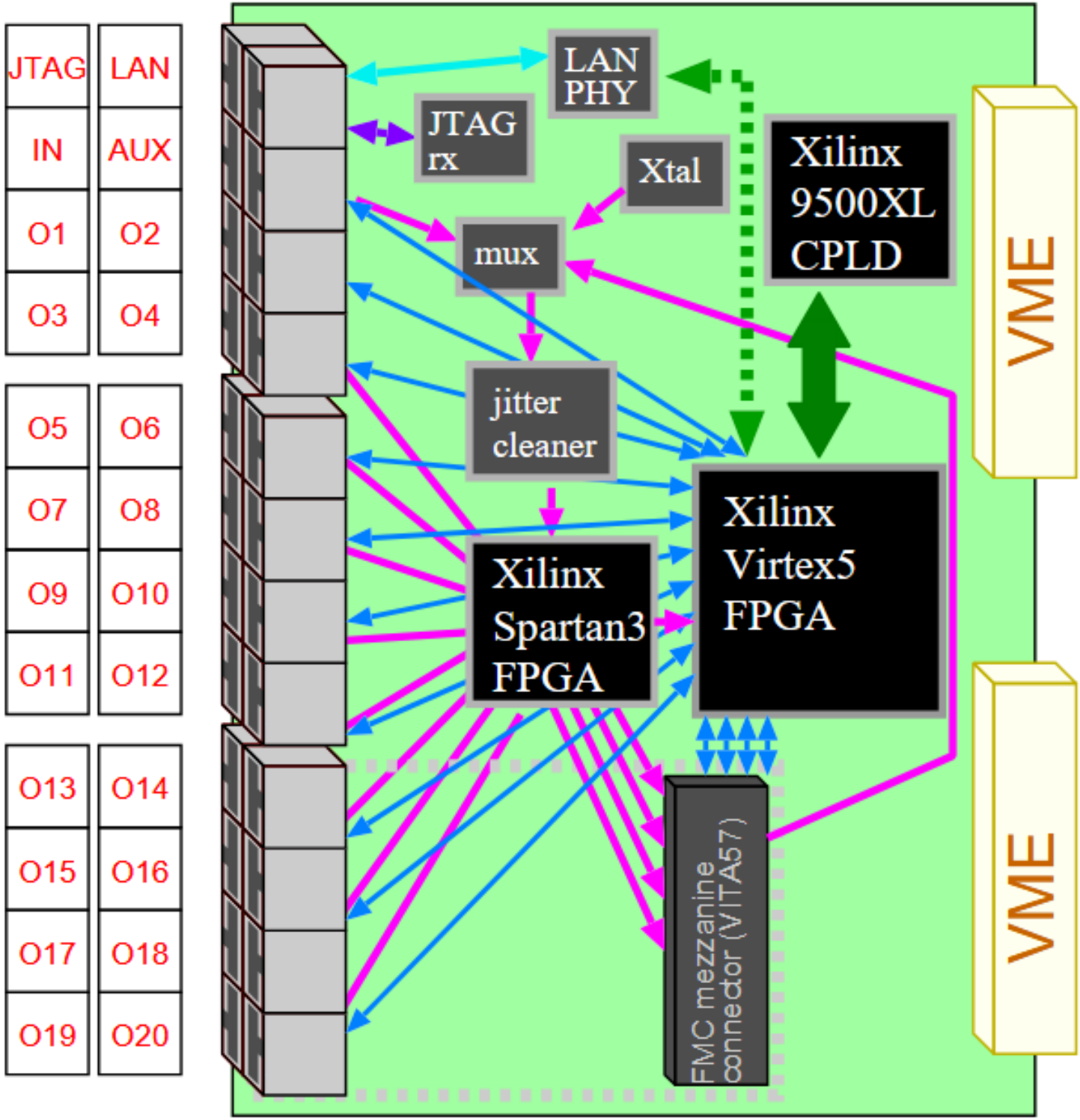
Clocking and FTSW Boards

Clock Synchronization:

- SuperKEKB RF clock at 508.9 MHz
- Divided by 4 $\rightarrow$ 127.16 MHz (used by FTSW)

FTSW – Frontend Timing Switch:

- FPGA-based boards
  - FTSW3 uses Virtex5 XC5VLX30-1FFG676
  - FTSW4 uses Artix7 XC7A200T-1FBG676
- Aggregate FEE data + trigger + timing
- Transmit using **b2tt protocol**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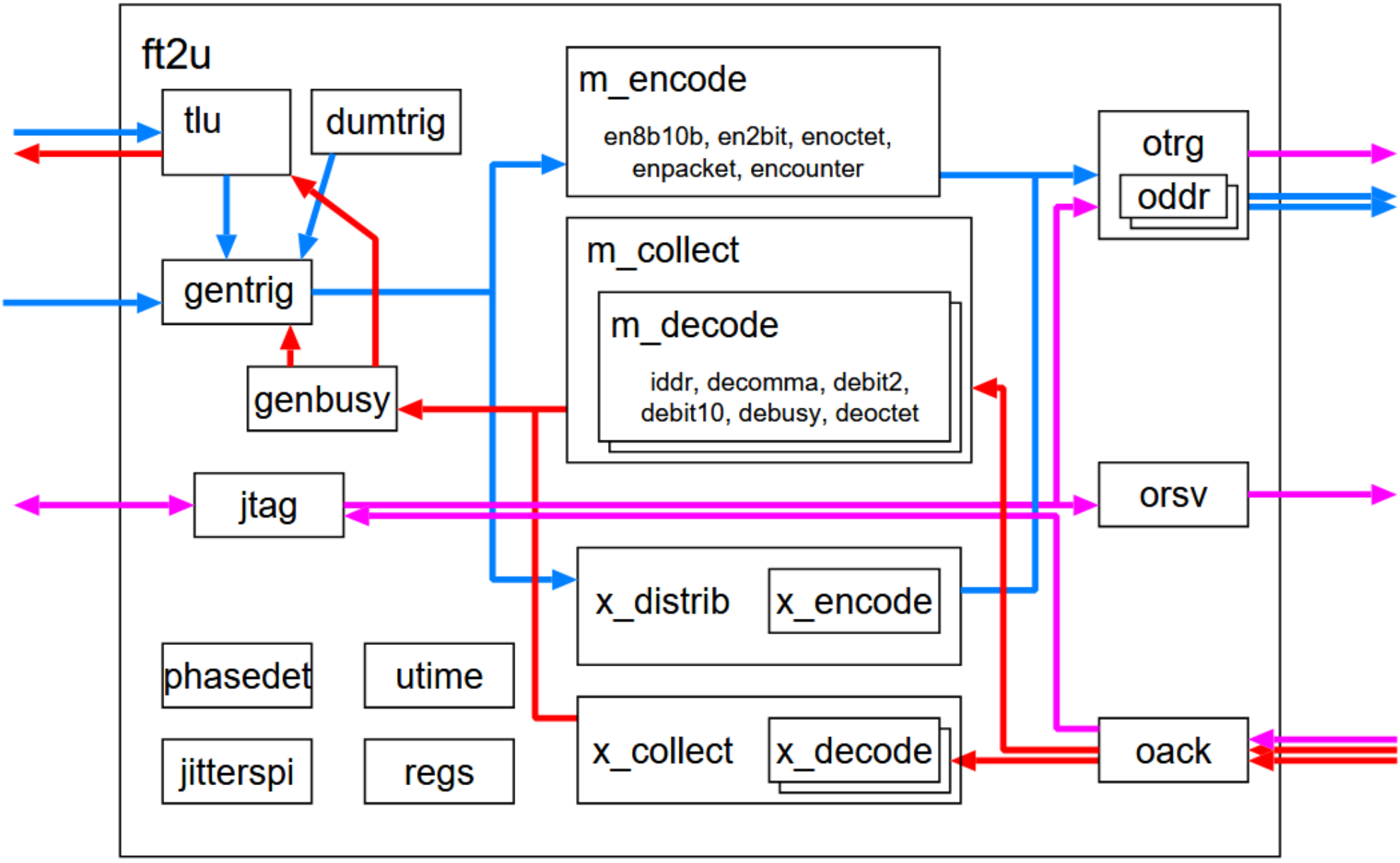
LAN PHY
JTAG rx
Xtal
mux
Xilinx 9500XL CPLD
VME
jitter cleaner
Xilinx Virtex5 FPGA
Xilinx Spartan3 FPGA
FMC mezzanine connector (VITA57)
VME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utime
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en8b10b, en2bit, enoctet,
enpacket, encounter
m_collect
m_decode
iddr, decomma, debit2,
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x_distrib
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FTSW4 board

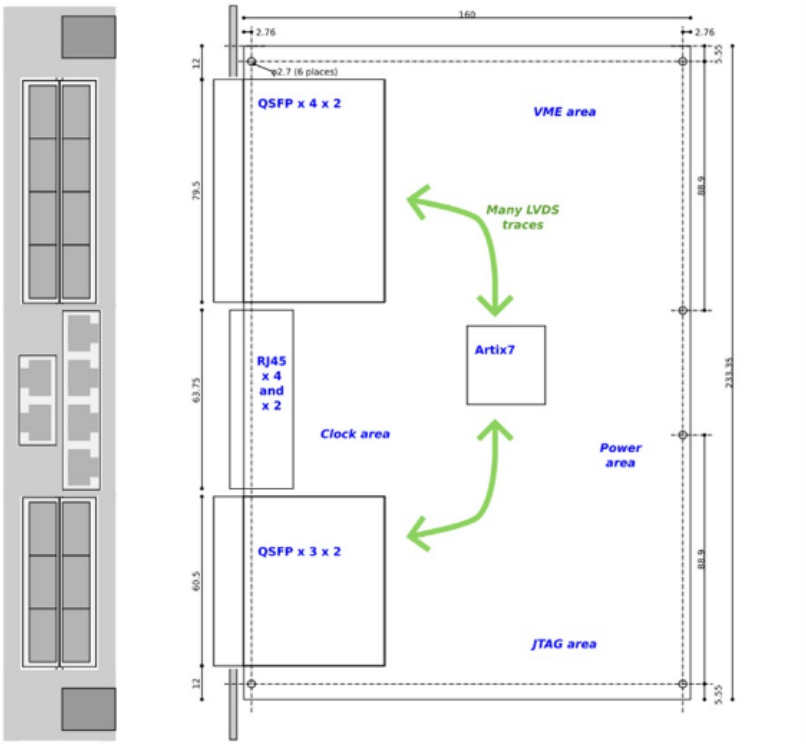


Figure: Schematic drawing of the FTSW4.1 board

Motivation for FTSW4 Upgrade at Belle II

- **Problem in FTSW3:**
  - Long distance b2tt links over CAT7 cables suffer occasional glitches, most likely due to electromagnetic interference.
  - Issue does not occur for short intra-crate connections or optical fibre connections
  - Loss of link $\Rightarrow$ DAQ stops until run restart.
  - Causes non-negligible efficiency loss in data taking.
- **Planned Solution:**
  - Transition from copper (CAT7) to optical fiber interconnects.
  - New module: **FTSW4**, 2-slot 6U VME with high-density optics.
- **Key Features of FTSW4:**
  - 12 QSFPs for trigger timing distribution + 2 QSFPs for uplink/other.
  - Supports up to 24 front-end/readout boards (2 fiber pairs per link).
  - Additional 6 RJ45 ports kept for legacy connections.
  - Controlled by cost-effective **Artix-7 FPGA**.

FPGA comparison

Spec	**Virtex-5 XC5VLX30 - 1FFG676**	**Artix-7 XC7A200T - 1FBG676**
Process node	65 nm	28 nm
Logic cells	30,720	215,360
Slices	4,800	33,650
Distributed RAM	320 Kb	2,888 Kb
Block RAM (36Kb)	32 ($\approx$1.15 Mb)	365 ($\approx$13.1 Mb)
DSP slices	32	740
Clock Mgmt Tiles	2	10
Total I/O banks	13	10
Transceivers	None (LX = no MGTs)	8 GTPs @ 6.6 Gb/s (FBG676 pkg)
Max user I/O	400	400

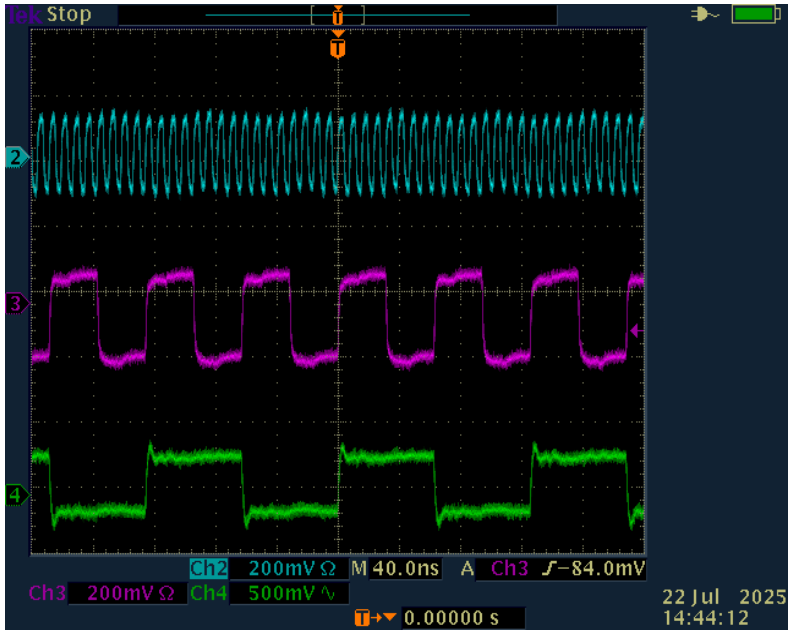
- **Resources:** FPGA on FTSW4 has $\sim$7$\times$ BRAM and $>$20$\times$ DSP vs FTSW3.
- **MGTs:** Virtex-5 has none; A200T (FBG676) has 8 GTPs (6.6 Gb/s).

LED Pattern Experiments (Jul 2025)

Update	**Key Points**
01-led (08/07)	▪ All LEDs on (static). ▪ Bug: ‘one_sec‘ in sensitivity list but unused.
02-cycle-led (10/07)	▪ Achieved cycling patterns via LUT. ▪ Downside: Explicitly typing all patterns. ▪ Next: streamline using logic.
03-led-cycle-proc (10/07)	▪ Split into 2 processes: counter + output. ▪ Learned rising edge sync. ▪ Issue: Cycle duration doubled.

Fast Pattern Generation (Jul 2025)

Update	**Key Points**
04-fast-pattern (15/07)	▪ Generated signals every clock cycle (4 cycles @127 MHz). ▪ Output only on TRG. ▪ Patterns: x up/x down ($x = 1$–4). ▪ Learned UCF, IOBUFDS, differential signaling.
05-fast-pattern-lut (16/07)	▪ Added RSV output, used LUT for multiple sequences. ▪ Each starts with ”00” marker. ▪ LUT modularized into external file. ▪ Next: test on FTSW-3.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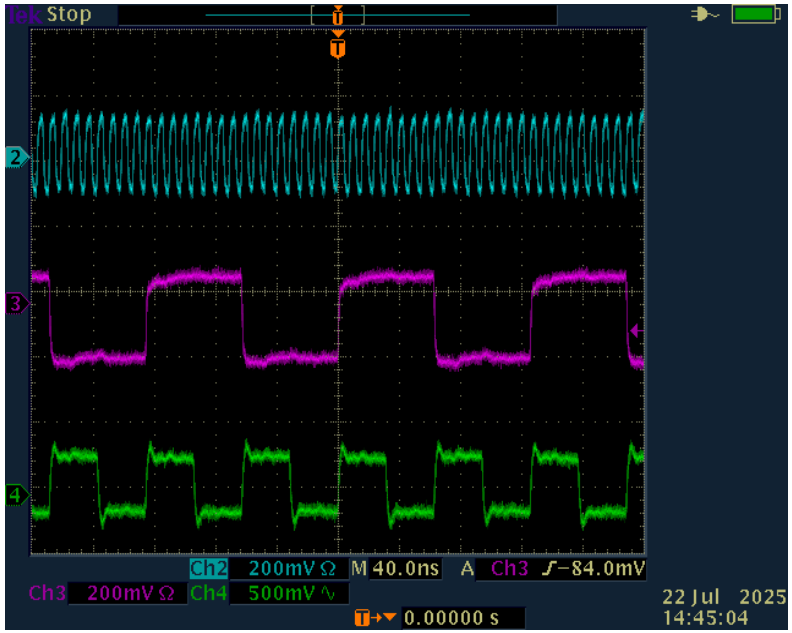
Ch2 200mV Ω M 40.0ns A Ch3 ∫−84.0mV
Ch3 200mV Ω Ch4 500mV ∿
0.00000 s
22 Jul 2025
14:44:12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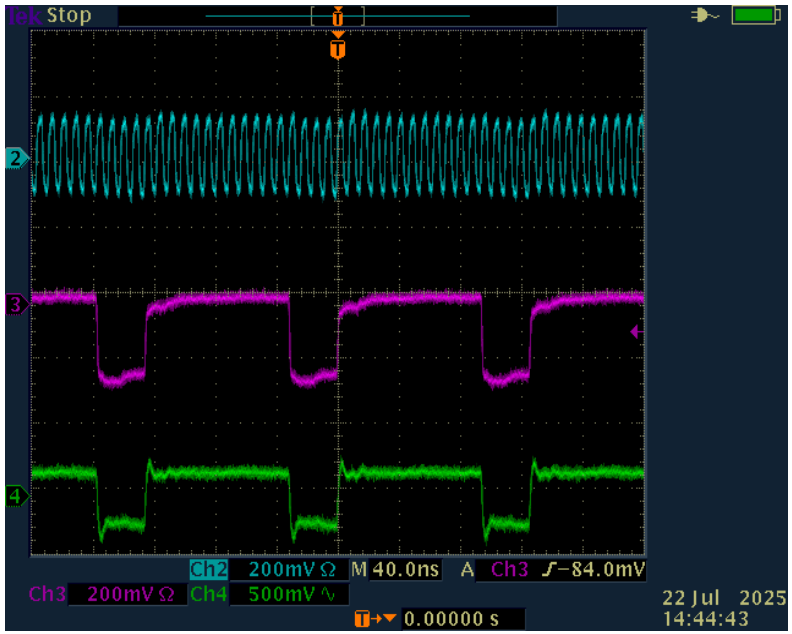
14:45:04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Ch3 200mV Ω Ch4 500mV ∿
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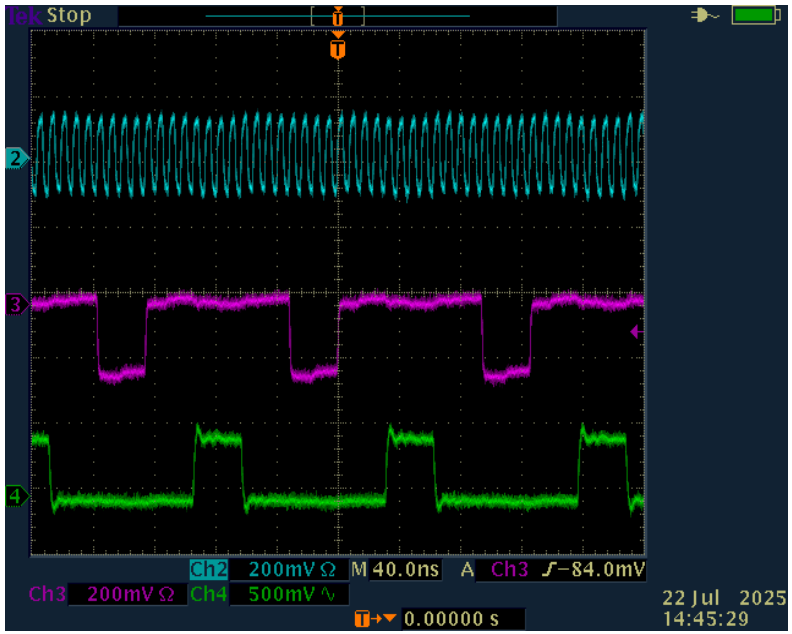
14:44:43


Stop
Ch2 200mV Ω M 40.0ns A Ch3 ∫−84.0mV
Ch3 200mV Ω Ch4 500mV ∿
0.00000 s
22 Jul 2025
14:45:29

Signal Testing (Jul 2025)

Update	**Key Points**
06-signal-testing(22/07)	▪ Based on LUT design, tested OUT-1..20. ▪ Used CLK, RSV, TRG, ACK channels. ▪ ‘obufds$_{m}$*odule*‘ + ‘*generate*‘*usedfordiff* .*signals*. ▪ LEDs verified shifting every 0.5s. ▪ Result: odd-port CLKs ok, even-port CLKs failed.
07-even-out-ports (25/07)	- Issue: CLK on even ports controlled by secondary Spartan FPGA. ▪ Fix: updated UCF, disabled ‘usejtag‘, tied ‘entck_o‘ to low. Result: CLKs work on even ports also.

Odd vs Even ports

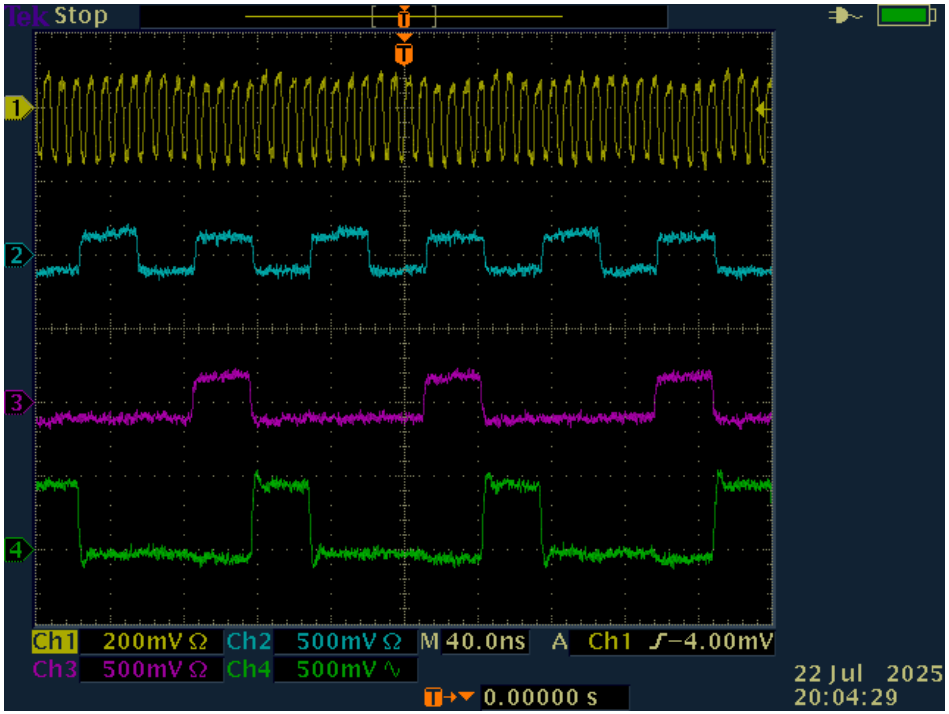


Figure: Output from odd ports

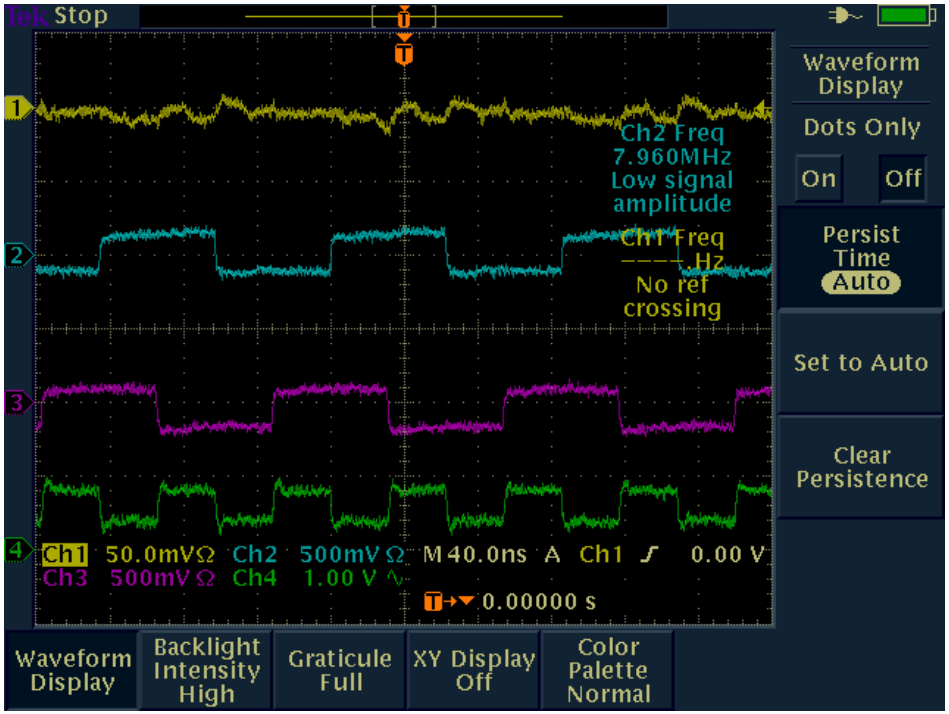


Figure: Even outputs

FTSW-4 Power Testing (Jul 2025)

08-ftsw4-current-testing (31/07)

- Test code derived from Prof. Nakao's code.
- Distributed fast clock 254 MHz across RJ45 ports.
- Goal: measure maximum possible current consumption.
- Observed ≈ 0.9 A consumption (same at 31 MHz and 127 MHz).

09 – ftsw4-qsfp-current-testing (04/08/2025)

Overview:

- Based heavily on `ftsw4.0-test/02-2v5`, with minor modifications.
- Tested current draw across different clock frequencies and output port combinations.

Clock Frequencies Tested: 254 MHz, 127 MHz, 31 MHz

Test Combinations:

Case	Description
1.1	Programmed, no QSFP modules: only RJ45 ports
1.2	Programmed, no QSFP modules: only QSFP ports
1.3	Programmed, no QSFP modules: both RJ45 + QSFP ports
2.1	Programmed, 1 QSFP module plugged in: only QSFP ports
2.2	Programmed, 1 QSFP module plugged in: QSFP + RJ45 ports
3.1	No program: QSFP plugged in
3.2	No program: QSFP not plugged in

Result: Power consumption recorded in *ftsw405-test-report.org* for all combinations.

Power Tree: 1-e. Current and Temperature (FLIR ONE)

Conditions:

- FTSW405 horizontally on the desk
- Matsusada power supply (current reading)
- 5.0V power supply at J17 5V0IN
- `f401c_drv31.bit`: 31 MHz clock output to all LVDS ports
- `f401b_drv127.bit`: 127 MHz clock output to all LVDS ports
- `f401d_drv254.bit`: 254 MHz clock output to all LVDS ports
- 127 MHz from oscillator, choice by SW3=00
- 254 MHz is generated by MMCM
- 254 MHz clock confirmed by Tektronix oscilloscope

Issues:

- FLIR ONE camera inconsistent with distance/ambient conditions.
- Devices were touched during run, affecting dissipation.

Readings:

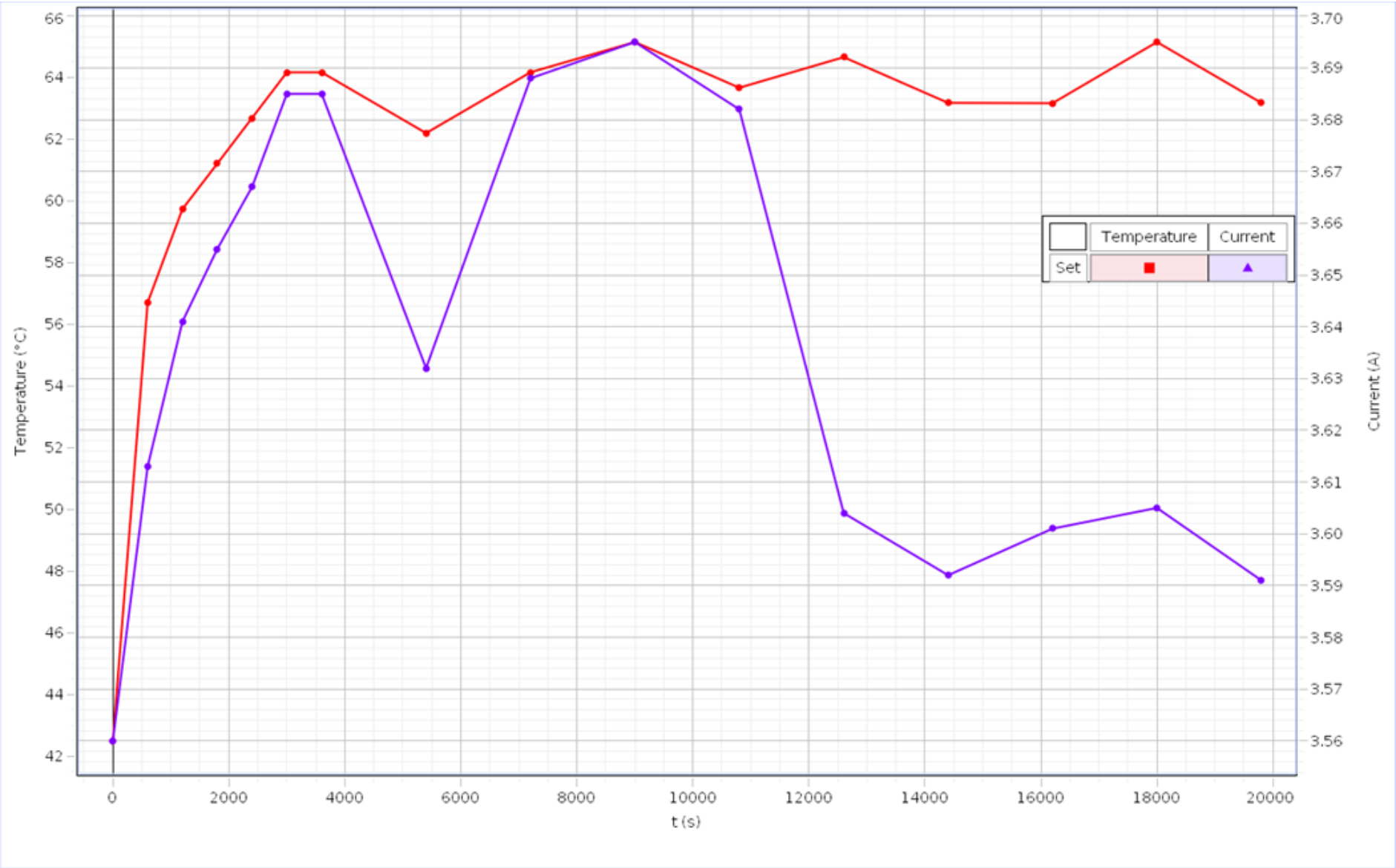
Current(A)	Temp(°C)	Time(min)
3.562	41	0.00
3.615	48	9.58
3.632	52	15.43
3.652	54	25.50
3.676	58	44.75
3.698	62	77.25
3.654	64.16	353.00
3.648	62.68	393.00

Power Tree: 1-e. Current and Temperature (ISE iMPACT)

- Conditions: Same as above. Readings taken using `Get Device ID` command in ISE iMPACT. Does not hamper code execution.
- Readings: for the FPGA running f401d_drv254.bit. Max Temp = 66.13 °C (QSFP x14, 1 connected to oscilloscope, 1 RJ45, 1 JTAG)

Current (A)	Temp (°C)	Time (min)
3.560	42.5	0.00
3.613	56.7	10.00
3.641	59.73	20.00
3.655	61.20	30.00
3.667	62.68	40.00
3.685	64.16	50.00
3.685	64.16	60.00
3.632	62.19	90.00
3.688	64.16	120.00
3.695	65.14	150.00
3.682	63.66	180.00
3.604	64.65	210.00
3.592	63.17	240.00
3.601	63.16	270.00
3.605	65.14	300.00
3.591	63.17	330.00

Plot of Temp and Current vs Time



Temperature and current fluctuations need to be studied further as it may affect component performance (e.g. clock)

10 – ftsw4-3v3en (05/08/2025)

Objective:

- Test ability to disable/reset board via 3V3EN signal connected to U14.18 (power module, enable pin) after 4 s.

Implementation:

- Code drives `3v3en = '0'` after 4 s to disable power module.

Observations:

- Early attempts: 0 was sent for only one clock cycle (31 ns), then reverted back to 1. Since the `EN` signal of the device has a long stabilization period (100 μs), the disable signal is ignored.
- Persistent '0' successfully disabled 3V3EN.
- LED D8 (DONE indicator) turned off permanently after 4 s.

11 – ftsw4-out-spikes (07/08/2025)

Objective:

- Verify that each of the 51 QSFP output channels ($4 \times 12 + 3$) receives a unique signal, confirming mapping and reach.

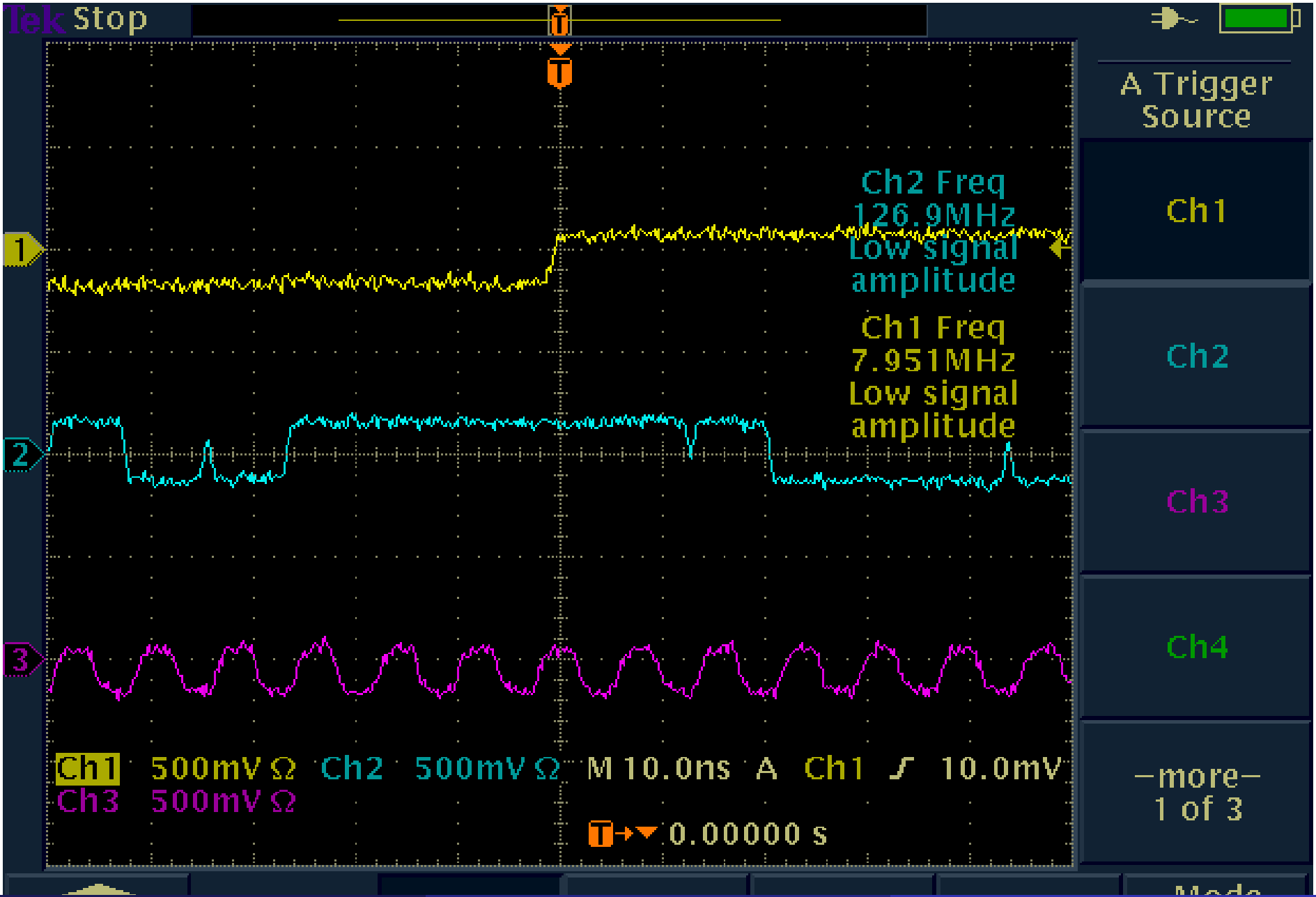
Implementation:

- 7×8 LUT assigns distinct 16-bit pattern to each port.
- Pattern formula: `'1'` + *6-bit binary(num)* + NOT(*6-bit binary(num)*) + `'010'`, where num $= 8 \times$ row + col.
- NOT + `'010'` maintain DC balance.
- Leading `'1'` and `'010'` give pattern boundary.
- 127 MHz clock used for bit output timing.
- Slow clock: 127.216 / 16 = 7.951 MHz used as Picoscope trigger.
- LUT entries mapped to QSFP ports via UCF file.
- FOR...GENERATE loops used to instantiate OBUFDS modules

Observations:

- Unique patterns observed on all outputs.
- Random voltage spikes/dips appeared in Picoscope readings.
- Spikes significant enough to risk misinterpretation.

11 – ftsw4-out-spikes (07/08/2025)



12 – ftsw4-qsfp-out (14/08/2025)

Objective:

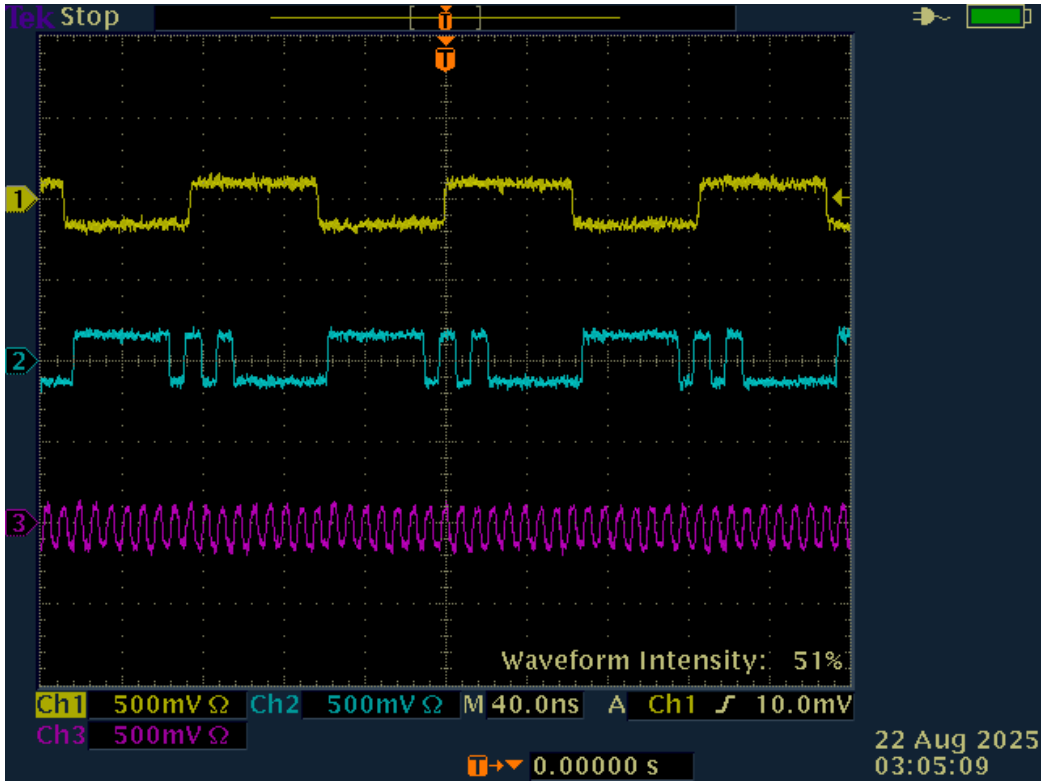
- Eliminate voltage spikes/dips seen in QSFP outputs during test 11.

Implementation:

- Cause: `bit_cnt` transitions through undefined intermediate states.
- Fix: Introduced buffer signal `temp`.
  - `temp` captures stabilized LUT value after `bit_cnt` changes.
  - QSFP outputs driven from `temp`.

Observations:

- Spikes/dips no longer present.
- Output patterns clean and correctly mapped.
- Phase difference between each output and trigger signal measured



Output Phase Table

Phase difference may occur between signals produced and received by FTSW board due to different signal paths, placement of I/O pins, etc.

Table for time lag (ns) between oscilloscope trigger and start of bit patterns. Signals 4-7 correspond to signals 0-4 of the ports on the B side.

Signal	Port 0	Port 1	Port 2	Port 3	Port 4	Port 5
0	***2320***	1722.5	482.5	402.5	362.5	482.5
1	642	402.5	1522.5	162.5	602.5	2002.5
2	1082.5	722.5	802.5	922.5	482.5	762.5
3	762	1282.5	482.5	1202.5	562.5	282.5
4	1282.5	602.5	1122.5	282.5	482.5	362.5
5	482.5	602.5	962.5	***37.5***	802.5	722.5
6	802.5	602.5	2242.5	562.5	682.5	722.5
7	402.5	602.5	962.5	1522.5	682.5	922.5

13 – ftsw-single-in (15/08/2025)

Objective:

- Verify reception of a QSFP signal pair and forwarding through FPGA.
- Test out implementation methods of signal reception and forwarding using OBUFDS and IBUFDS modules

Implementation:

- QSFP port 2: generates 127.216 MHz clock.
- QSFP port 1: one differential pair serves as input.
- FPGA forwards received signal from port 1 to port 0 using `mid_1_0`.
- QSFP port 0 outputs signal to Picoscope.

Observations:

- Forwarded signal matched input.
- Confirmed correct input reception and forwarding path.

14 – ftsw-in-drops (15/08/2025)

Objective:

- Verify simultaneous input reception from all signal pairs in 4 QSFP ports.

Implementation:

- Based on previous test, extended to multi-port capture.
- Used intermediate `temp` signal to suppress spikes.
- Introduced `std_logic8_vector dead` with modules `dso`, `dsi` to map unused ports to '0'.
- Required because unused differential signals cannot remain unconnected.

Observations:

- Expected signals observed for most tested ports.
- Significant noise when signal='1' in patterns from ports (which ports depend on firmware).
- Noise absent when oscilloscope connected directly to generating ports.
- Root cause unresolved.

Input Signal Comparison

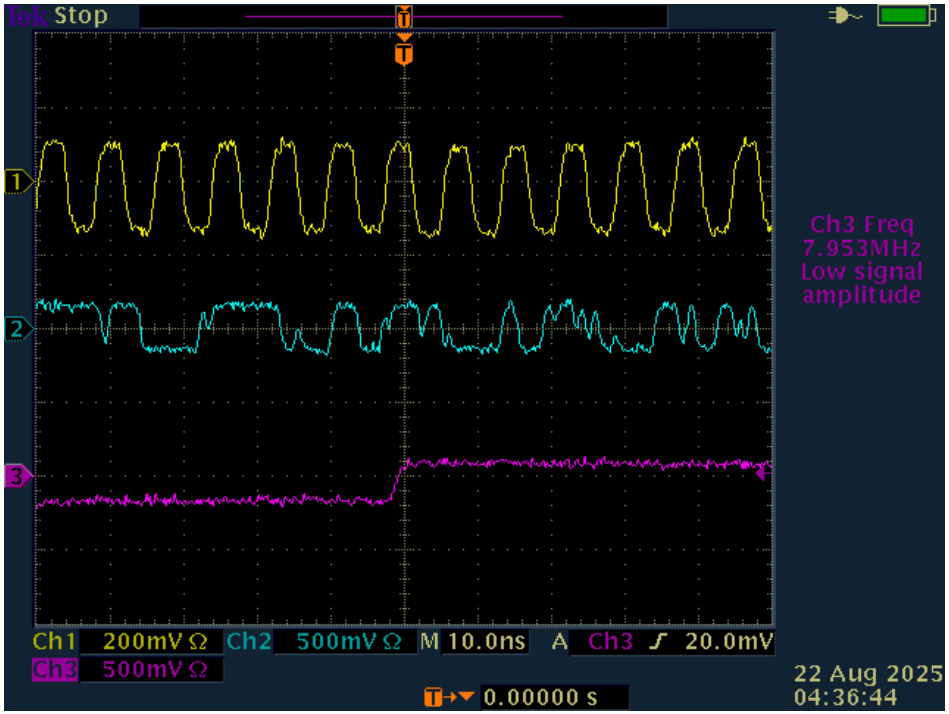


Figure: Signal from Output port

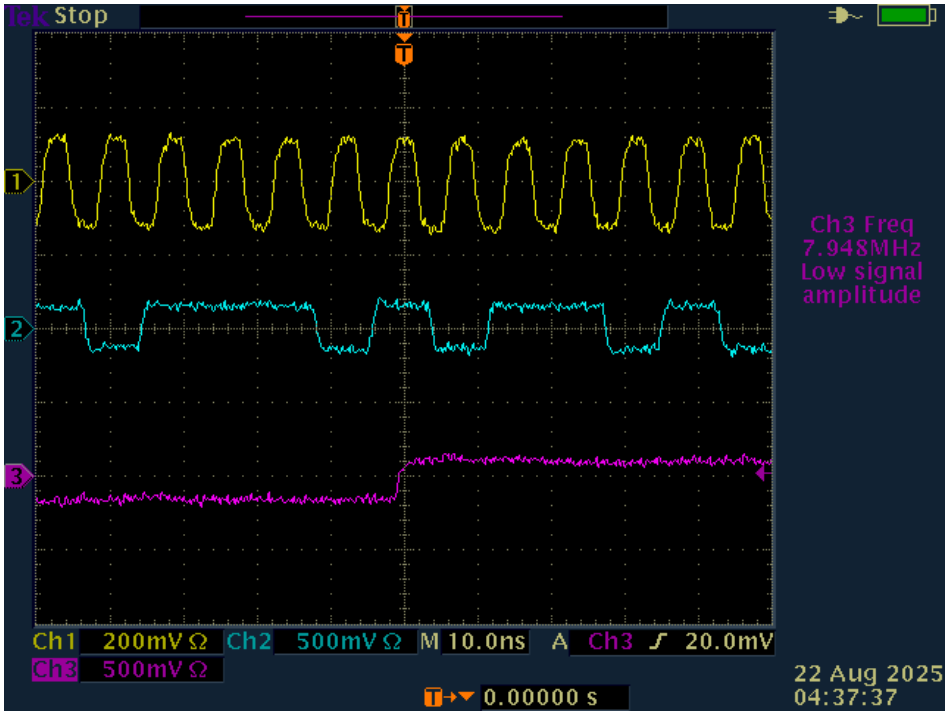


Figure: Signal from Generating Port

Noise Issues in FTSW Board

- Excessive noise during signal reception and forwarding is undesirable for the FTSW board due to TTD role
- Magnitude is sufficient to trigger false negatives and false positives
- This could be disastrous during DAQ operation
- Issue was reported to Prof. Nakao
- Over the last week, multiple hypotheses, checks, and solutions were tested by Prof. Nakao
- My work: shadowing Prof. Nakao and replicating his proposed solutions on board #405

Hypotheses and Checks (1/2)

1. **Timing constraints not implemented correctly**
   - Added constraints for time period in UCF file corresponding to the clock signal driving the logic (7.9 ns for 127.216 MHz)
   - Noise persists
2. **Logic to receive/transfer signals flawed**
   - Tested by programming board with two independently developed firmware versions
   - Bit pattern generation mechanism different in both cases
   - Noise persists
3. **Unused output signals improperly terminated (set to 0)**
   - Made unused output lines produce clock signals
   - Noise persists
4. **Signal corruption inside FPGA or at ports**
   - Probed FPGA pins / QSFP ports with LeCroy oscilloscope
   - Signals clean entering and leaving FPGA

15 – high-speed-in (20/08/2025)

Objective:

- Investigate whether spikes/drops from test 14 are caused by sub-1 Gbps bitrate.

Implementation:

- Repeated multi-port input test at higher speeds.
- Used MMCM module `f4_mmcm.vhd` to generate 254 MHz, 339 MHz, 508 MHz clocks.
- Updated timing constraints in `f4-clk.ucf`.
- At 508 MHz, 1.965 ns clock constraint unmet: compiled but outputs incorrect.

Observations:

- Spikes/drops persisted at higher frequencies.
- Issue unrelated to bitrate.
- Anomalies remain unresolved.

Hypotheses and Checks (2/2)

5. **Insufficient power supply to QSFP ports**
   - Programed board with firmware utilizing only 3 ports (vs 12 ports)
   - Current consumption read 1.3A at 5.0V (vs. 3.7A max)
   - Noise persists
6. **Incorrect capacitor/inductor connections**
   - Capacitors for quick current discharge were connected before inductor used to filter incoming 3.3V signal. Effectively rendered useless
   - Electrical patches done by Prof. Nakao on 3 ports of board #402
   - Though a valid diagnosis, noise persisted
7. **QSFP transmission bitrate too low**
   - Tested with 127 MHz, 254 MHz, 339 MHz and 508 MHz clock signals
   - Respective timing constraints were declared in .UCF files
   - Firmware using 508 MHz clock signal failed to compile due to 1.9 ns timing constraint.
   - On successfully compiled firmware noise persisted.
   - However, this led to final set of tests

Crisis Averted?

- Firmware written by Prof. Nakao to transmit signals using the **b2tt protocol**
- 12 QSFP ports were paired (*up* + *down*) into 6 communicating pairs
- **LED indicators:** used to indicate
  - Successful connection (transmission + reception)
  - Number of connection failures (individual pair + total)
- **On-board switches** used to monitor each individual pair

Results and Verification

- Stable signals observed for all 6 pairs after a few initial connection failures
- **Oscilloscope measurements:** confirmed integrity of transmitted signals
- **LEDs and switches functionality:** validated by hot-swapping QSFP modules
  - LEDs correctly reflected connection status
  - Switches responded as expected

b2tt signal

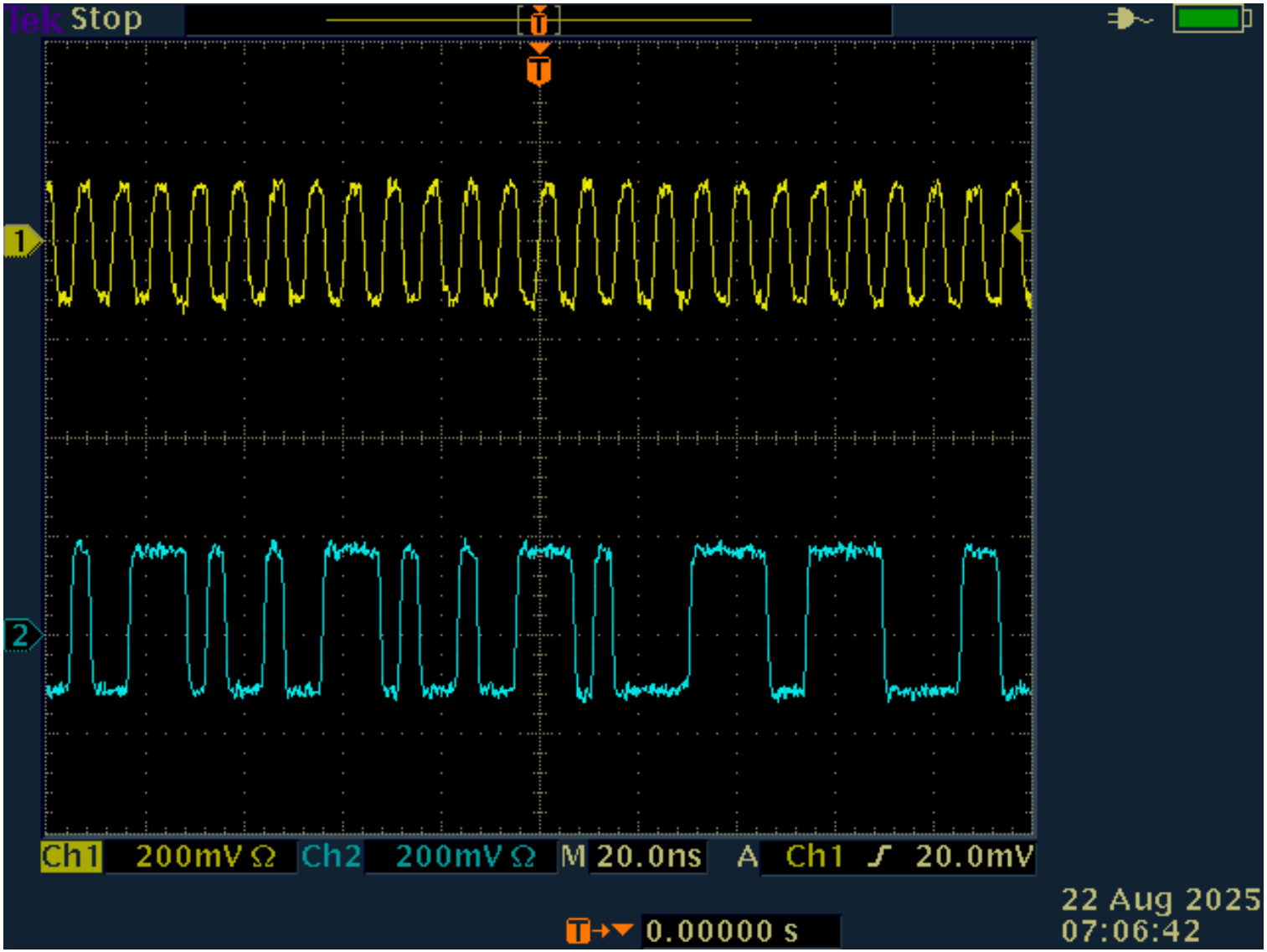


Figure: Signal captured after flashing f405j_b2tt.bit

Power Tree: 1-a. Resistance between power lines (2025-07-31)

- Resistance (Ohm) measured between GND(J13) and power points, using HIOKI 3245-60
- A: GND/black probe at GND
- B: GND/black probe at power
- (*2) does not stabilize, jumps between 100k and 10k

	5V0	3V3	2V5	1V8	1V2	1V1	1V0INT	1V0MGT
Testing Pt	TP3	J13	TP9	TP11	TP12	TP10	TP4	TP5
A	13.8k	200.8	(*2)	1.045k	2.323k	398	90.3	690
B	3835	222.2	1.941k	881	1.593k	520	183.1	755

Power Tree: 1-b. Test by applying 3.3V at J3 (2025-07-31)

- 3V3 supplied at J3 pin header, voltages at power points measured (mV).
- (*1) Regulators for 1V0INT, 1V0MGT activate as low as 2V.

Supply (V)	Current (mA)	3V3	2V5	1V8	1V2	1V1	1V0INT	1V0MGT
1.0	19	999	825	328.2	341.6	32	0	0
1.5	119	1492	1487	1456	824	161	0.7	7.5
2.0*	839	1932	1917	1795	1215	1061	984	997
2.3	872	2231	2207	1802	1216	1100	998	1003
2.4	948	2325	2294	1802	1216	1100	997	1003
2.5	959	2423	2379	1802	1216	1099	997	1003
2.8	982	2722	2484	1802	1216	1099	997	1003
2.9	990	2822	2485	1802	1216	1099	997	1003
3.0	998	2922	2485	1802	1216	1099	997	1003
3.3	1023	3222	2485	1802	1216	1099	997	1003

Power Tree: 1-c. Test by applying 5V at J17 (2025-07-31)

- 5V0IN supplied from J17 (VME connector).
- Voltages of 3V3 and 3V3_EN measured (mV).
- (*1) below 4.663V: 3V3_EN stays at $<$0.04 V.
- (*2) At 4.663V: 3V3_EN jumps to 3.3 V.
- (*3) At $>$4.675V: immediate 3V3_EN.

Supply(V)	I(A)	5V0	3V3	3V3_EN
2	0.006	2.002	0.017	0.684
3	0.010	3.004	0.022	0.888
4	0.014	4.006	0.031	1.089
4.2	0.016	4.200	0.033	1.129
4.4	0.02	4.400	0.035	1.168
4.6(*1)	0.031	4.600	0.036	1.208
4.663(*2)	0.800	4.600	3.322	3.292
4.675(*3)	0.800	4.610	3.323	3.298
5	0.790	4.940	3.324	3.458

JTAG & Clock

- Initialize chain OK: FPGA (XC7A200T) + CPLD (XC95288XL).
- JTAG programming of FPGA works via RJ45, flat cable and optic fibre cable (QSFP module unchecked).
- CPLD + SPI flash programming not fully tested.
- Automatic Input Selection: flat cable prioritized.
- Clock signal verified using oscilloscope probe at clock pins.

Concluding Remarks

Key Takeaways:

- Developed a solid understanding of hardware design and development.
- Gained skills in concurrent programming and signal manipulation, applicable to other physics software avenues such as parallel processing.
- Learned to appreciate the interplay between practical engineering and theoretical physics.
- Benefited from interactions with top experts in the fields of DAQ and analysis.

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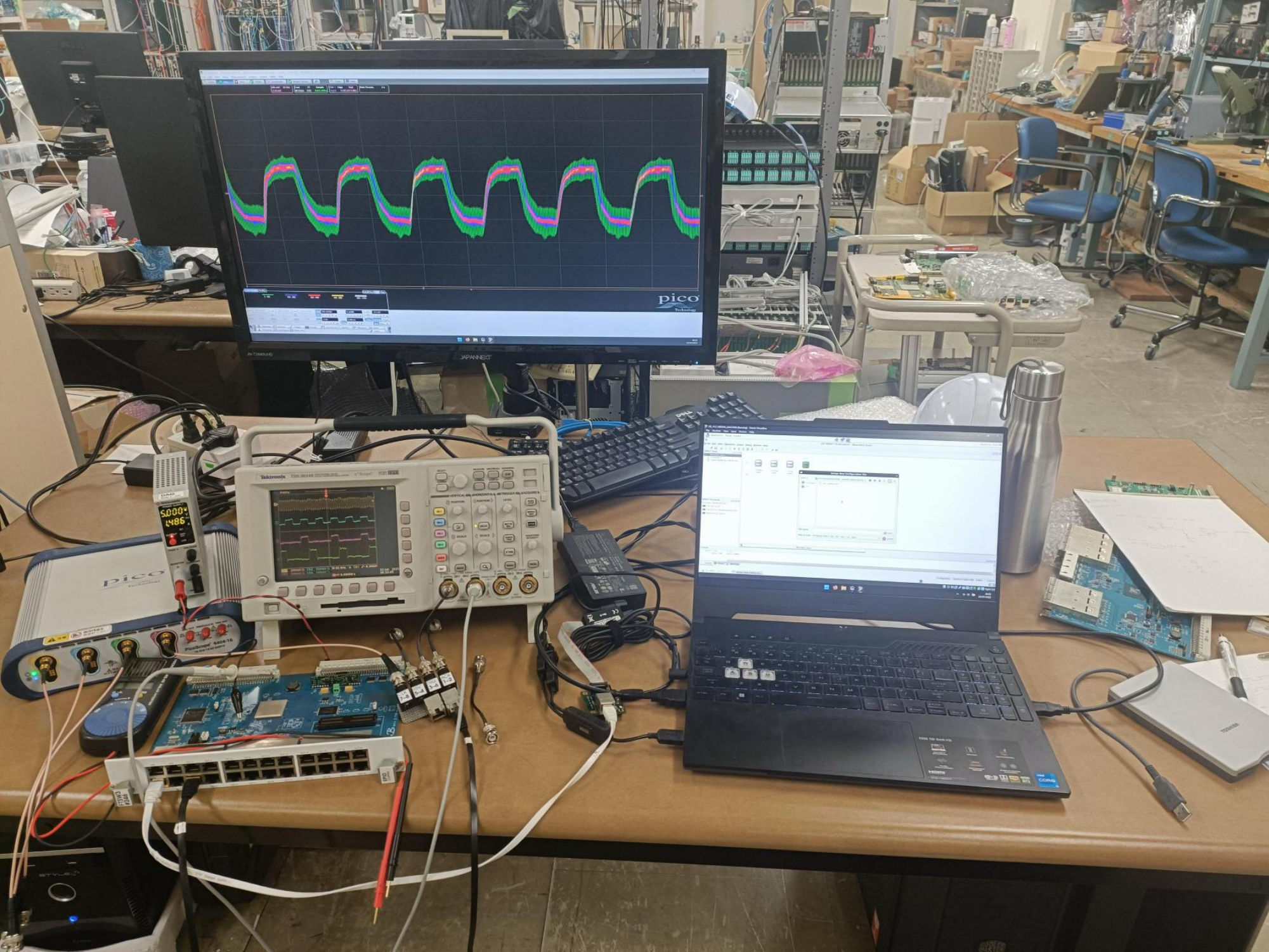
- **Prof. Satoru Yamada**: Project point of contact
- **Sokendai and KEK**: Sponsor and host of the KEK Summer Student Program

Thank You!

Questions and Discussion Welcome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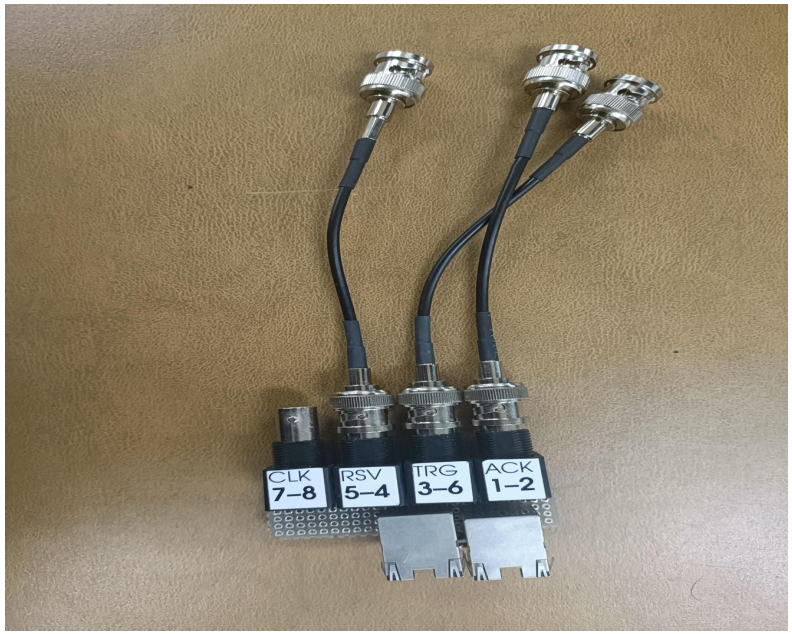
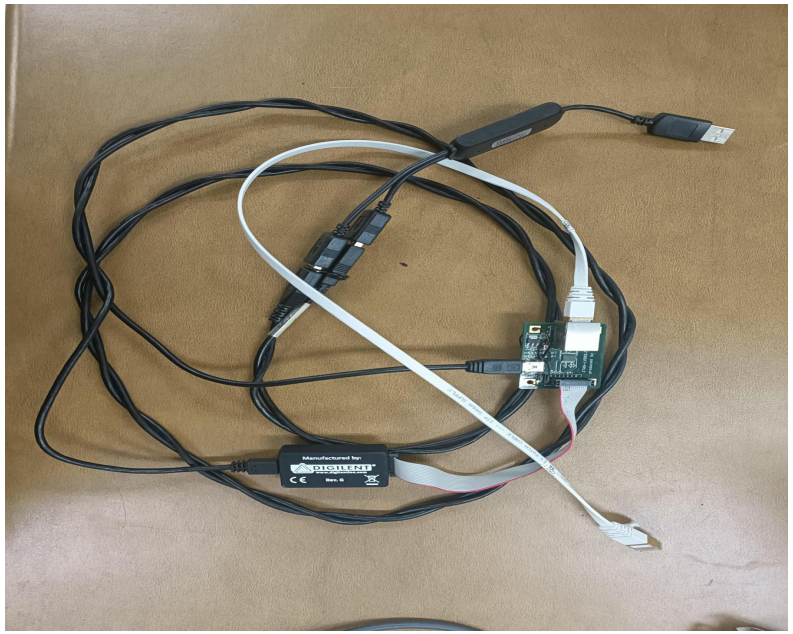
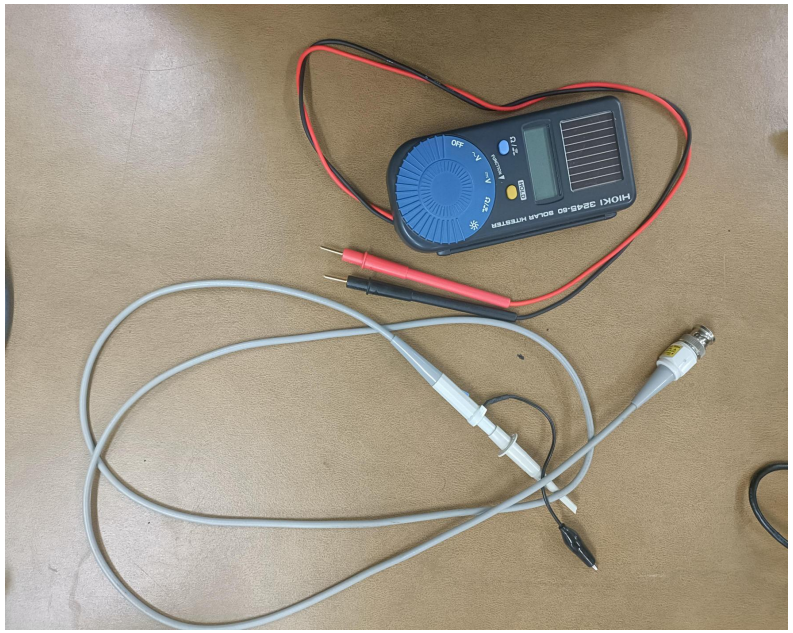
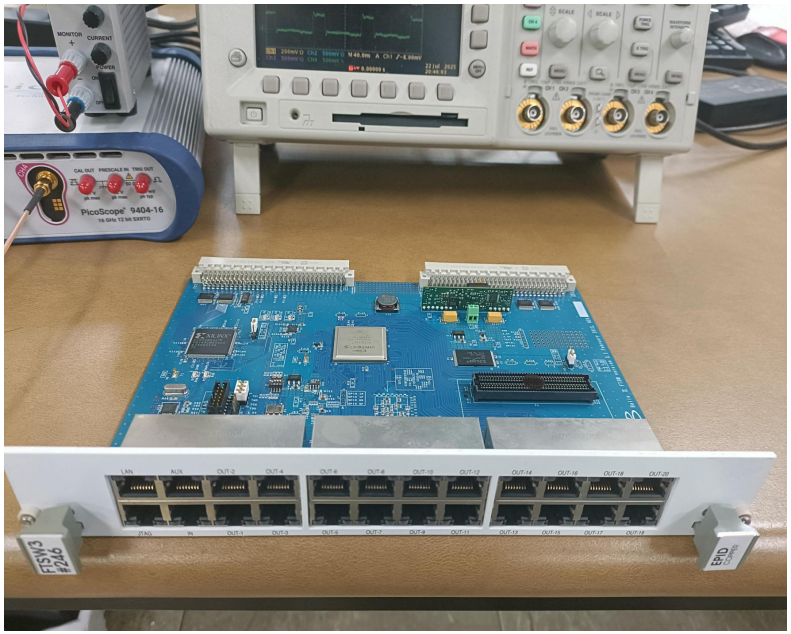
Cable Equipment

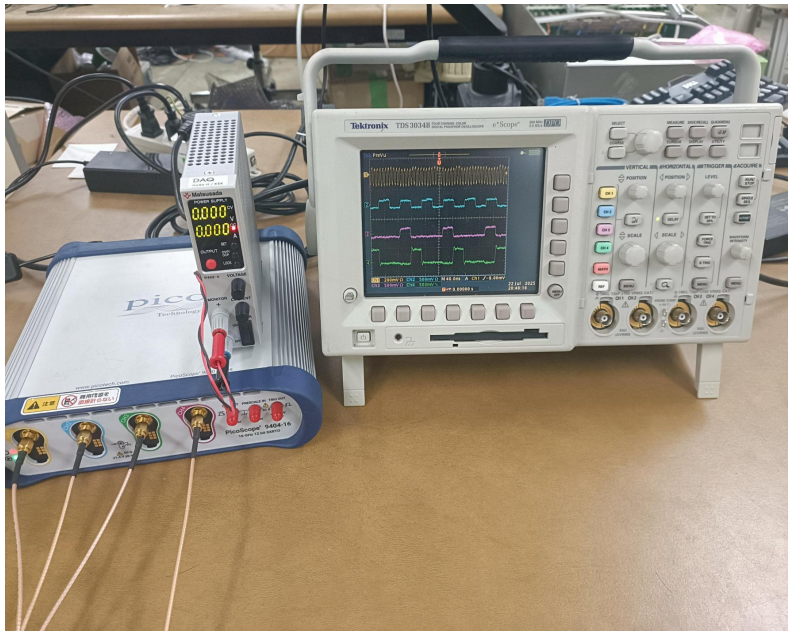






Cable Equipment






Clear
Run
Stop
Single
Autoscale..
Default Setup..
Copy..
Help
100 mV/ 16 GHz
-3.14 mV
5 ns/ ET Sample
40 GSa/s 2 KS 15.76 kWfm
Ch4 / Edge High
Trig'd f=127.217 2 MHz
Dots Persist. 2 s
C4
T
Color Grade
Scales
Auto
Max
Mid
Min
1 - 185
186 - 371
372 - 742
743 - 1484
1485 - 2969
pico
Technology
Ch1
100 mV/div
Ch2
100 mV/div
Ch3
100 mV/div
Ch4
100 mV/div
0 div
5 ns/div
5.325 ns
-3.1 mV
Freerun
Trig'd
Pos
Neg
Bi
Channels
Acquire
Trigger
Display
Save/Recall
Marker
Measure
Math
Histogram
Eye Diagram
Mask Test
Utility