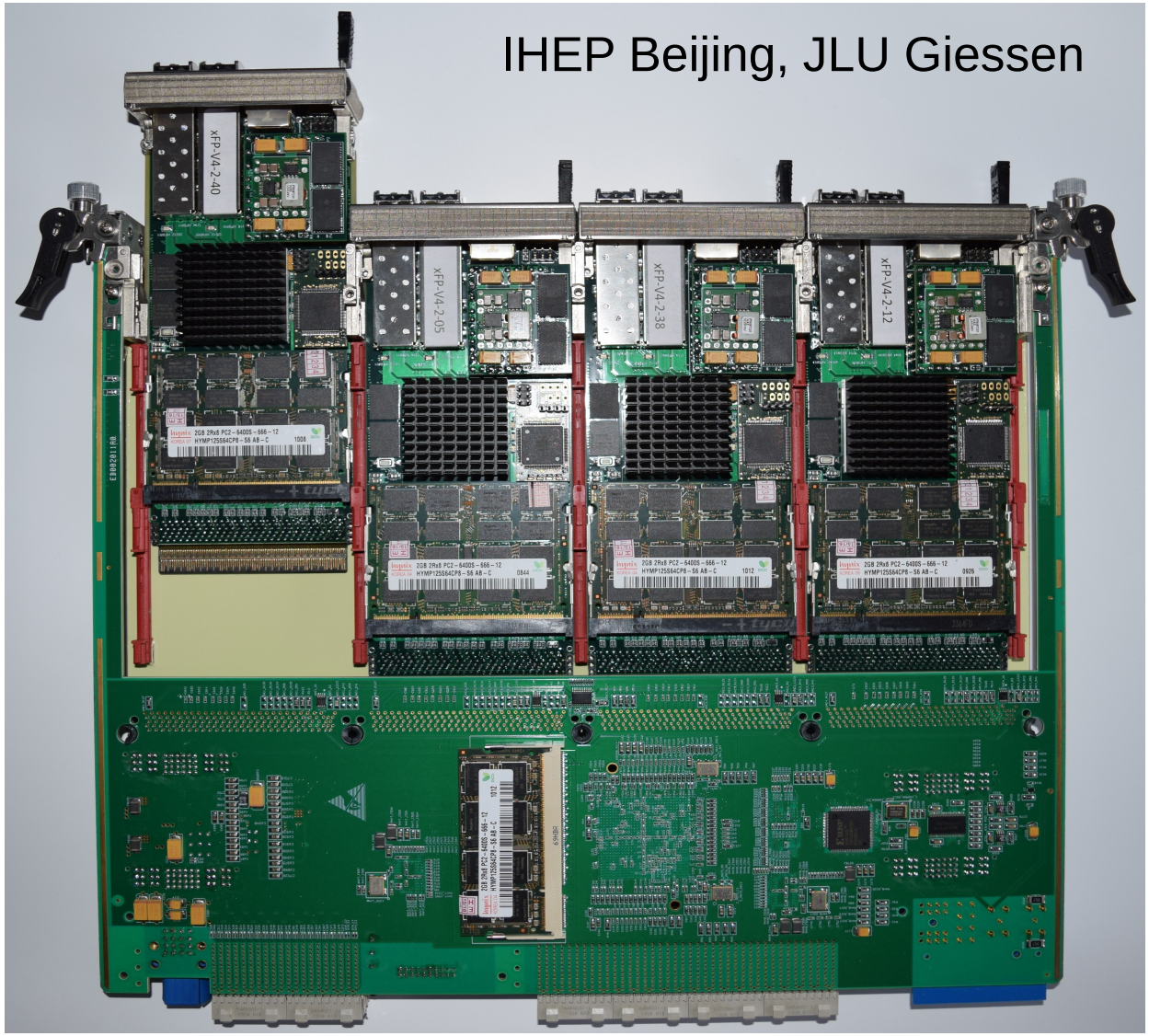
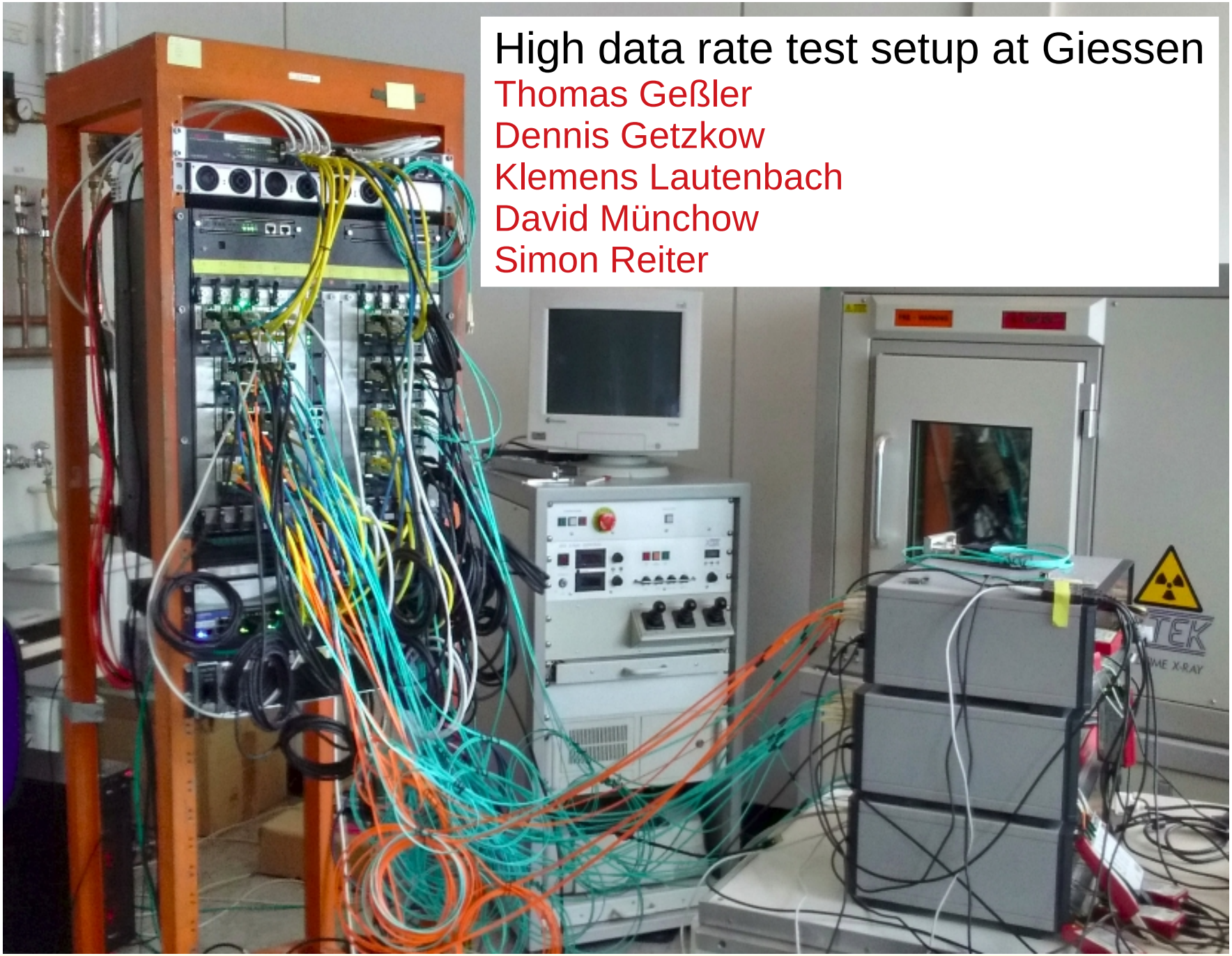
FPGA Hardware (XILINX Virtex–4 FX60, Virtex-5 FX70T)



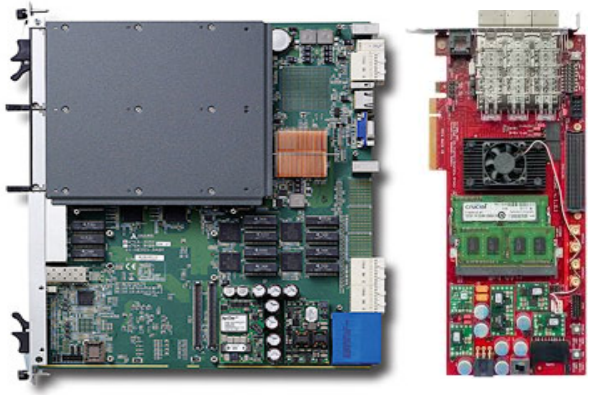
Final PXD readout hardware, mass production (IHEP, Giessen)

High data rate test setup at Giessen

Thomas Geßler
Dennis Getzkow
Klemens Lautenbach
David Münchow
Simon Reiter



Additional FPGA Hardware



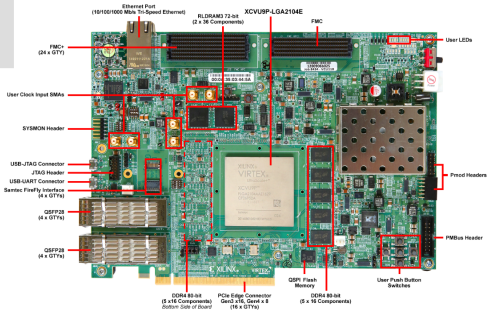
ALICE C-RORC, Virtex-6 LX240T
Optical 12 x 6G (optical), PCIe

Intel 40G (optical)

New Carrier Board (IHEP Beijing, Giessen)
Kintex UltraScale 060, 16 Gb DDR4
Optical 32 x 16.3G

ATCA ADLINK aTCA-3150
10G Uplink

ATCA ADLINK aTCA-3710
40G Uplink



Virtex UltraScale+ Board
Optical 8–32 x 28G

Two NN approaches for FPGA

1.) DSP Slices (matrix multiplication in hardware)
Falk Zorn

2.) High Level Synthesis („C program translated into bitstream“)
Peter Lehnhard

Small GPU

Quelle: techpowerup.com

8 processors
clock 1.06 Ghz
28 nm process (2012)

Programming: Marvin Peter
CUDA
Keras & TensorFlow

Large GPU (not tested yet)

Quelle: nvidia.com

nVidia p5000
2560 processors
clock 1.6 Ghz
16 nm process (2016)

16 GB GDDR5X, 256 bit wide, 288 GB/s
PCIe 3.0, x16