

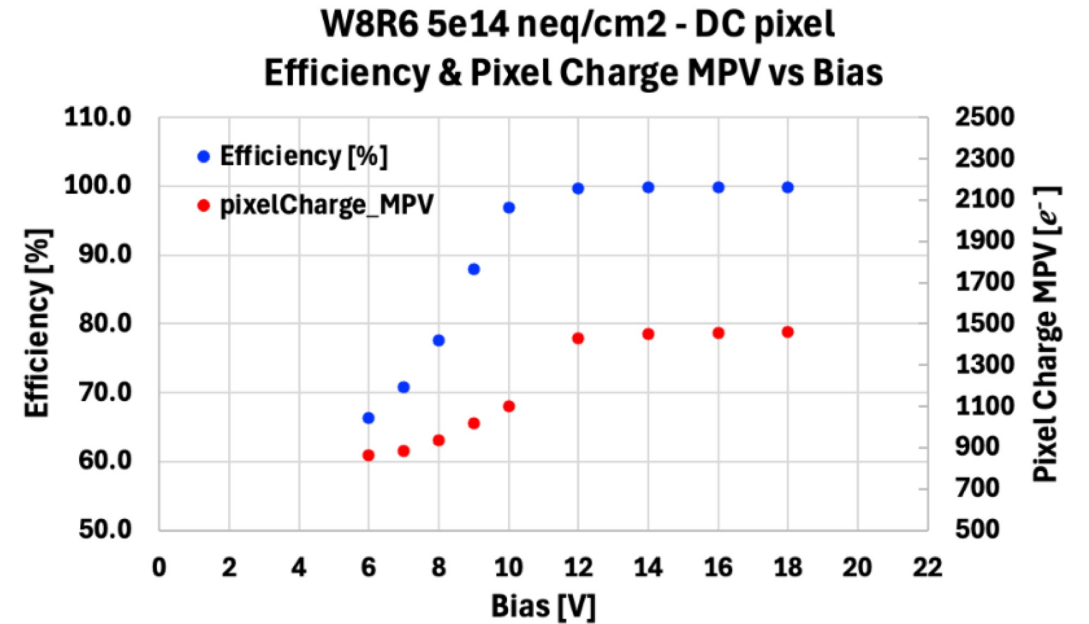
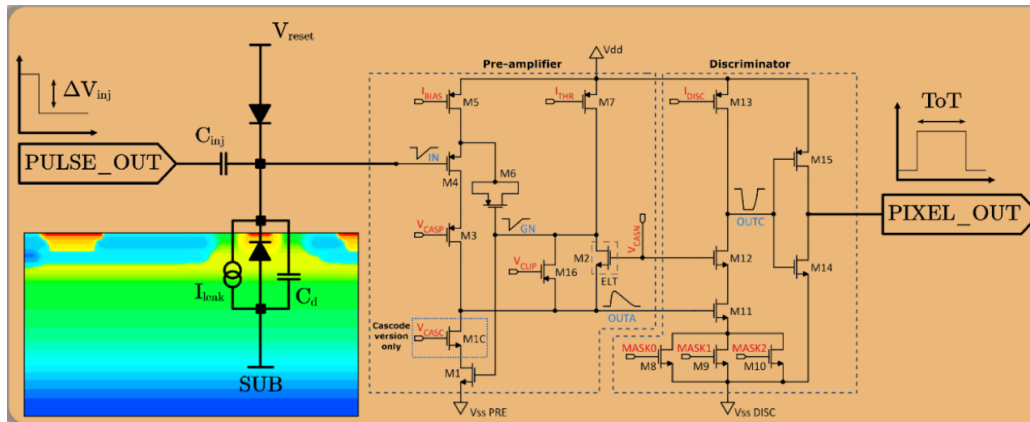
WG3 STATUS REPORT

C. Bepin on behalf of WG3

2nd VTX General Workshop – 20.04.2026

- TJ-Monopix2 testing activities slowing down
- Preparations for OBELIX-1 testing ramping up
 - Identifying participating institutes
 - Training on TJ-Monopix2 testing
 - Development of OBELIX-1 lab test DAQ system

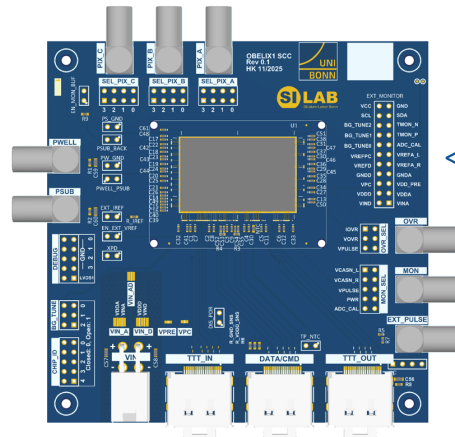
- Wrapping up test beam results of irradiated TJ-Monopix2
- Inconsistency between MPV charge and efficiency
- Leakage / discharge effect?
- Charge calibration depending on injection speed?
- Investigate with TCAD + FE sim



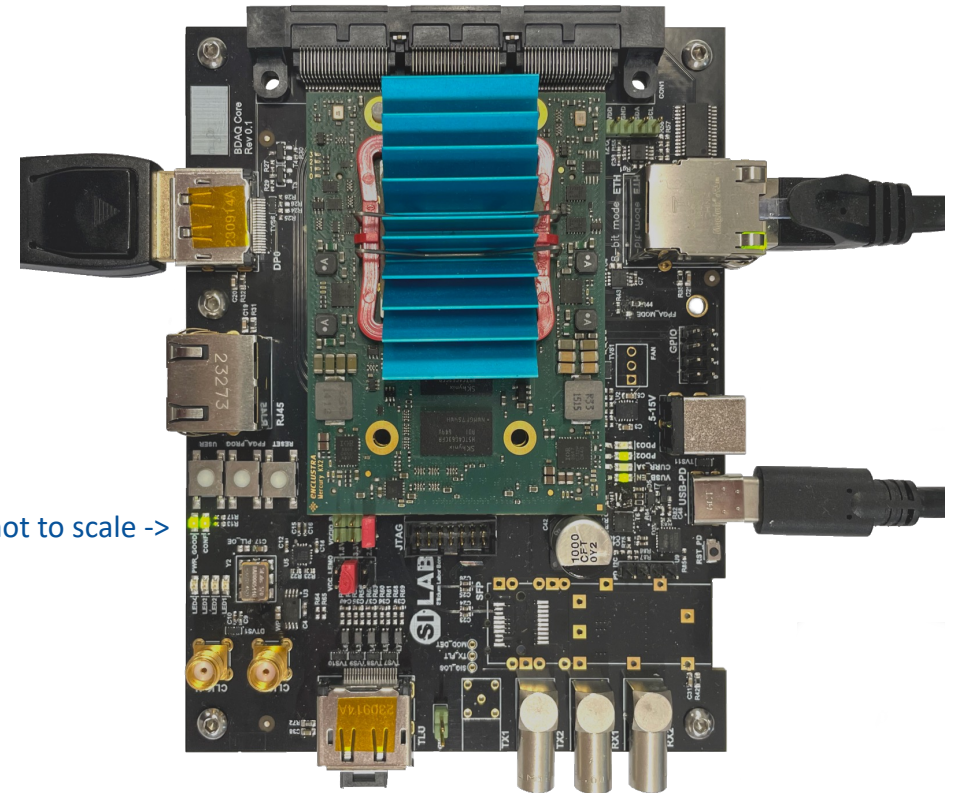
- Workshop on TJ-Monopix2 testing as preparation for OBELIX testing
- April 13 - 15 hosted in Pisa by local team (thanks!)
 - Participants from MBI, CPPM, IPHC, and IFIC
 - Hands-on lab work with DAQ board, chip, software
 - Fruitful round-table on last day with remote participants
 - Lots of ideas about test procedures, “wish list”, ...
 - Valuable input for DAQ development workshop



- Hardware ongoing:
 - BDAQcore board: next prototype iteration in production
 - After successful tests: survey to get estimate for # of boards
- Single chip carrier board:
 - No update since last workshop; design basically ready, wait for final OBELIX-1 design

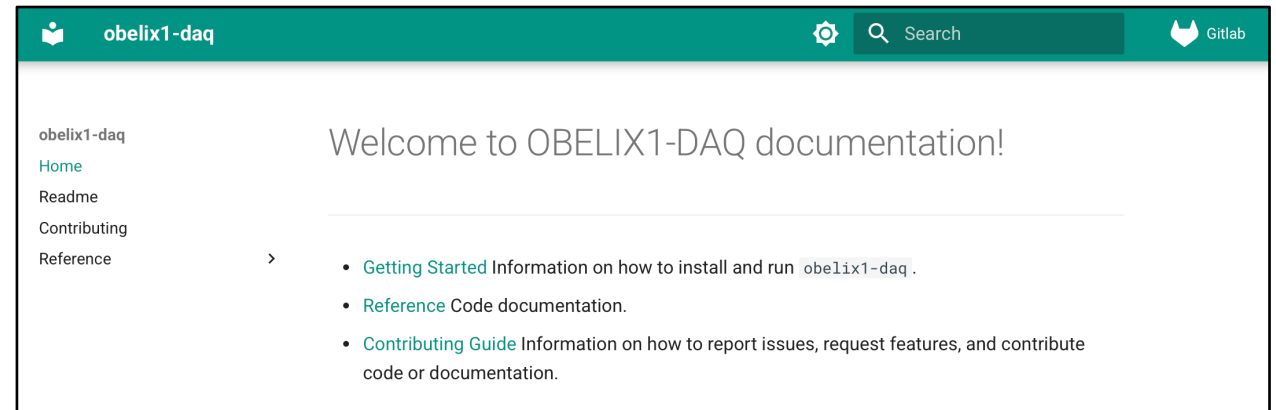


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N.b.: BDAQ53 still fully supported, no need to get BDAQcore board

- Software and firmware
 - Development started, reusing most blocks from TJ-Monopix2
 - same interface and usage (e.g. register access, pixel masking, scan implementation)
- Support multi-chip readout from the start
- Automated testing in CI (currently 72 % of software code covered in tests)
- Write documentation (usage and API) in parallel



- Software/firmware:
 - DAQ development meeting in Bonn (May 04 – 06) with OBELIX designers and experts
 - Discussions and planning for defining tasks, responsibilities, organisation, etc (following the TJ-Monopix2 testing workshop in Pisa)
- Gitlab access being figured out, currently no VTX user group

- Later (but before chip arrives): follow-up workshop for OBELIX lab DAQ system (usage, structure, how to contribute, open tasks, and more)

Id	Activity	Bonn	MBI (HEPHY)	Pisa	IPHC Strasbourg	CPPM Marseille	KEK	Pavia/Bergamo	DESY	Goettingen	Valencia
1	OBELIX single PCB chip design	x	x								
2	PCB adapter for multi-chip/flex/lpGBT design	x		?							
3	OBELIX single PCB chip production	x	x								
4	OBELIX single PCB chip assembly	x	x		x						
5	Bonding	x	x	x	x						
6	BDAQ core board (new)	x									
7	Firmware development (modules for OBELIX communication...)	x	x		?						
8	Software development (python modules, chip object registers/masking ...)	x	x	x	?						
9	Specific test scripts development Triggered operation	x	x	x	?						
10	Specific test scripts development TTT	x	x	x	?						
11	Specific test scripts development PTD	x	x		?						
12	DAQ for testbeam	x	?						x		
13	Telescope preparation (for TB in KEK)				x		x		?		
14	Temperature control setup for lab/testbeam		x	x							
15	Irradiation TID/NIEL	x		x	x						
16	Test SEU	x									
17	Test irradiation spikes (SBL)										
18	Post irradiation characterization			x							
19	Lab test	x	x	x	x	x	x	x	x	x	x
20	Testbeam preparation/operation	x	x	x	x		x		x	x	
21	Testbeam analysis			x						x	
22	wafer/dies management				x						
23	wafer testing				x						
24	BDAQ53 board for TJMP2 test available	x	x	x	x	x	x		x	x	x

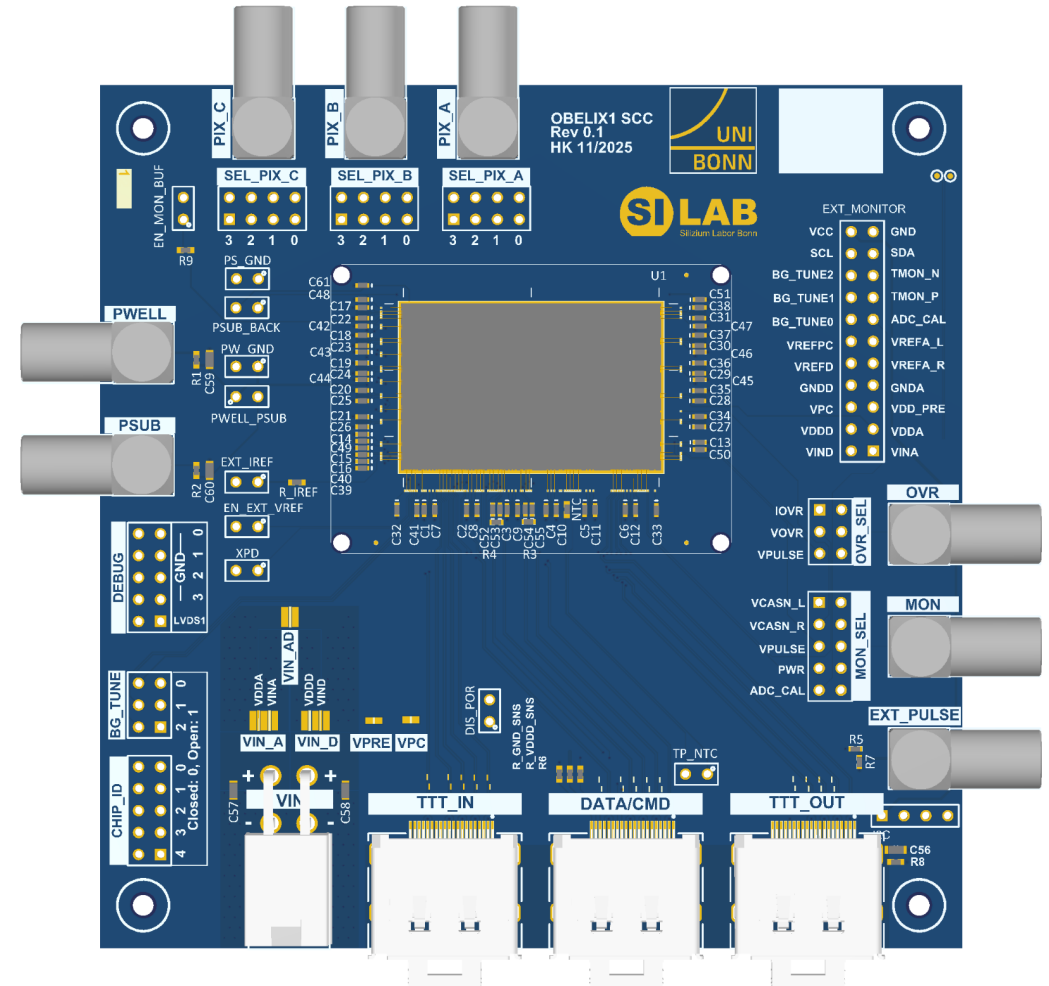
To be updated

- Shifting from TJ-Monopix2 testing towards OBELIX testing
- Preparations in full swing
 - User training for familiarity with tests, test setup, chip basics (Pisa workshop with TJ-Monopix2)
 - Lab DAQ planning (Bonn workshop)
 - Future: lab DAQ user workshop

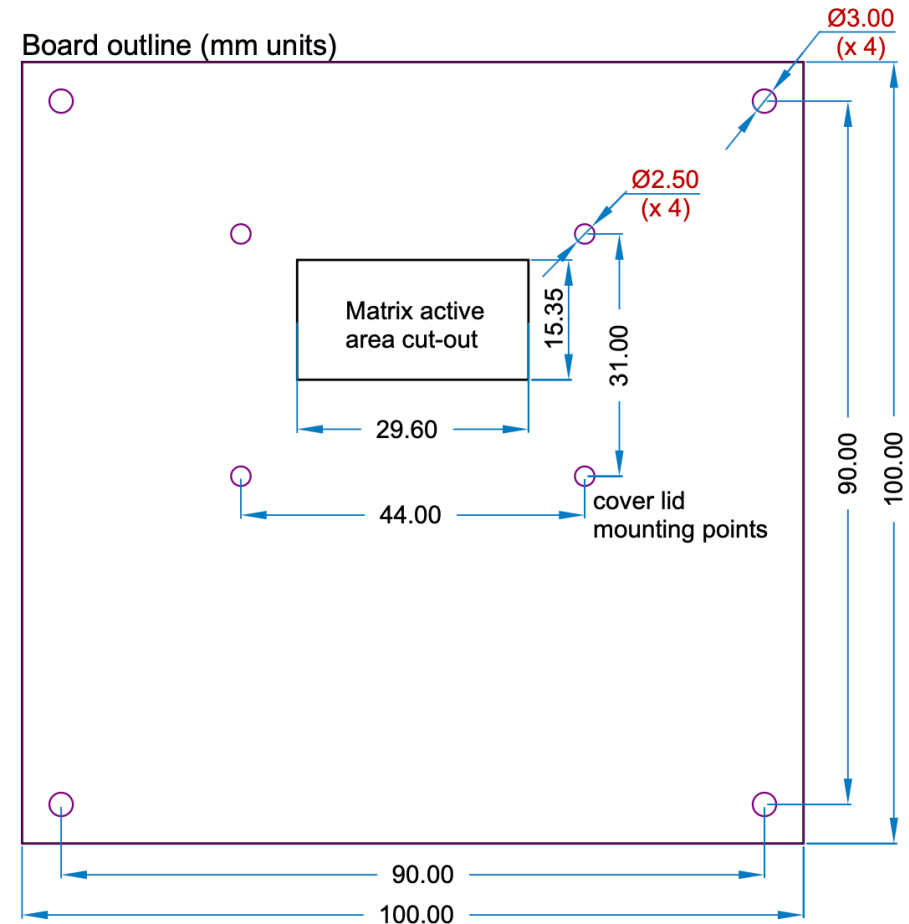
BACKUP

SINGLE-CHIP CARRIER BOARD

- Reviewed in OBELIX technical designer meeting
- Wire-bonding of one OBELIX-1
- TTT in, TTT out, DATA/CMD via DisplayPort
- No active components (beneficial for irradiation tests)
- Analog pixel output
- Overwrite / monitor currents and voltages

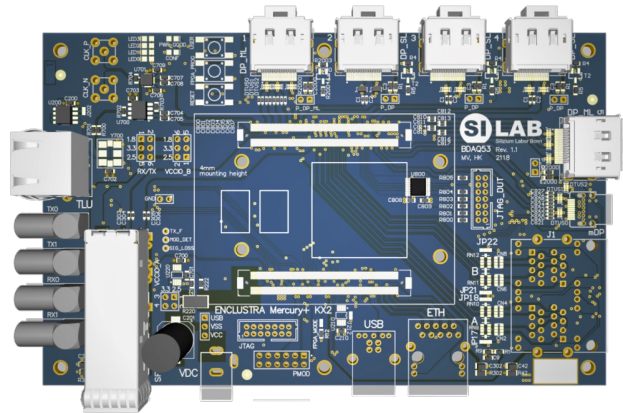


- Same PCB size, mounting points and chip position as TJ-Monopix2 board
- Cut-out for active matrix area
- Mounting holes for chip cover
- Documentation (and later production files) available in DAQ repository on git:
<https://gitlab.desy.de/vtxupgrade/obelix1-daq>



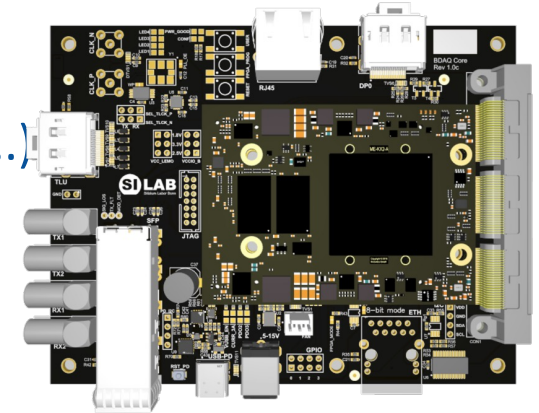
BDAQ53

- Developed for RD53 testing
- 1 DP (or up to 4 RJ45) connectors usable for Monopix/OBELIX
- 1 GbE / 10 GbE to user PC



BDAQ CORE

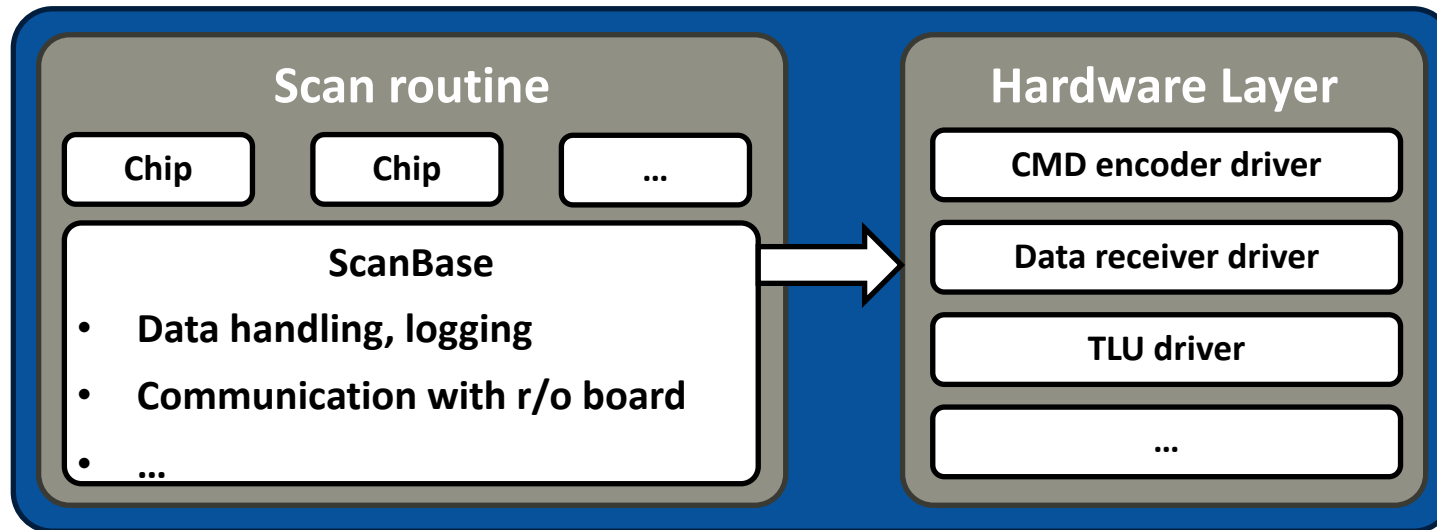
- Multi-purpose readout board
- 1 DP and 1 RJ45 for quick testing
- 1 GbE / 10 GbE to user PC
- 150-pin connector for adapter boards (more DP, flex, VTRx+, ..)



- Development started and ongoing
- Familiar structure
 - Code documentation
 - PCB design files (see before)
 - Unit tests
 - Pre-commit (code style / checks)
 - Contribution guide (getting started)

Name	Last commit	Last update
docs	ci: deploy docs to Gitlab pages	1 month ago
etc	sty: remove syntax error from veribl...	2 months ago
firmware	fix: adjust port names on higher level	2 months ago
obelix1	New tt injection pattern.	3 weeks ago
pcb	Upload New File	2 weeks ago
.gitignore	Update gitignore with typical python ...	10 months ago
.gitlab-ci.yml	ci: deploy docs to Gitlab pages	1 month ago
.pre-commit-config.yaml	sty: ruff format in pre-commit	2 months ago
CONTRIBUTING.md	DOC: fix typos	2 months ago
LICENSE	proj: add license	4 months ago
README.md	sty: ruff format in pre-commit	2 months ago
mkdocs.yml	ci: deploy docs to Gitlab pages	1 month ago
pyproject.toml	ci: fix conflicting pre-commit settings	2 months ago

- Re-use (and improve) a lot of existing code from TJ-Monopix2 testing
- Object-oriented approach



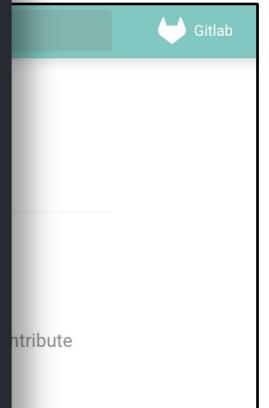
- Instantiation of multiple individual chips (module) not different than one
 - Same scan routines and interface for user

- Software a
- Develop
- same
- Support m
- Automate
- of softwar
- Write docu
- in parallel

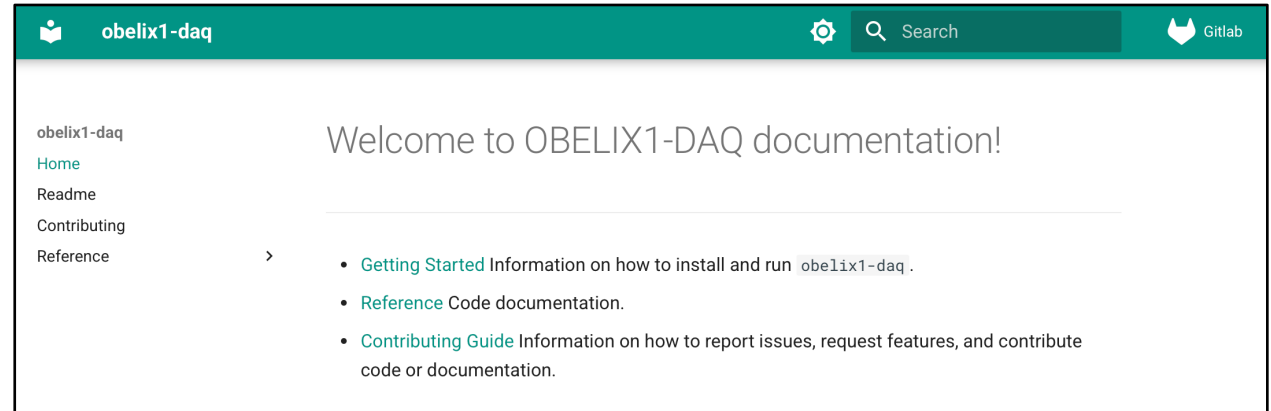
```

1  def get_write_command(self, value: int | str = None) -> list:
2      """Get list of commands to write `value` to the given register.
3
4      Args:
5          value (int | str, optional): Value to be written. Defaults to None.
6
7      Returns:
8          list: Command list
9      """
10     if value is not None:
11         self.set(value)
12
13     if self["size"] <= 16:
14         wr_value = 0x0000
15         for reg in self.chip.registers.get_all_at_address(self["address"]):
16             wr_value |= reg["value"] << reg["offset"]
17
18         return self.chip._write_register(self["address"], wr_value, write=False)
19     wr_value = eval("0b" + "0" * self["size"])
20     indata = []
21     for i in range(0, self["size"], 16):
22         reg_value = (self["value"] & (0xFF << i)) >> i
23         indata += self.chip._write_register(self["address"] + self["size"] // 16 - 1, reg_value, write=False)
24     return indata

```



- Online documentation (Gitlab Pages) set up
 - Code reference and usage guide
- Documentation in code itself
 - docstrings / type hints



- **Crucial for reliability** and (mostly) included in Gitlab
- Automated testing at every change of code, immediate feedback
- Current pipelines: code style check, running tests with simulated OBELIX, deploying docs

