UNIVERSITÄT BONN

SiLAB Silizium Labor Bonn

FTD

# All-Silicon Modules

VTX Workshop
April 2026 at Desy

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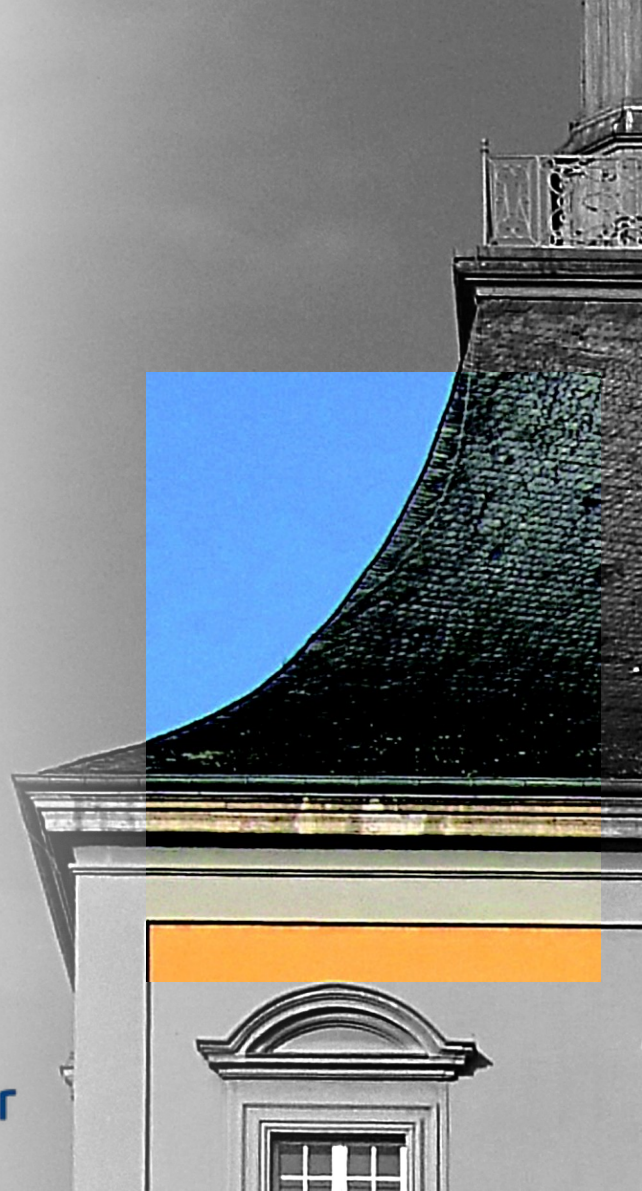
Physikalisches Institut der Universität Bonn

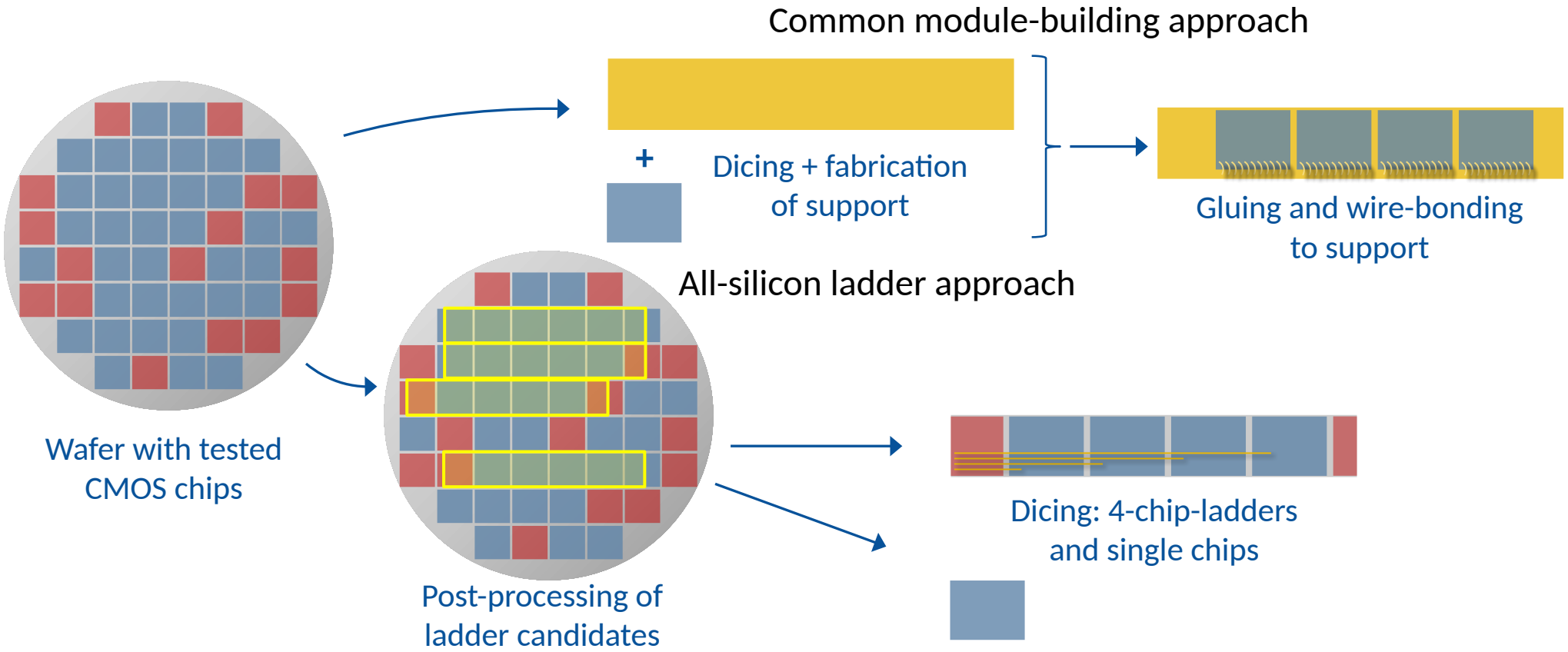


Bundesministerium
für Forschung, Technologie
und Raumfahrt

Belle II VTX

color meets flavor

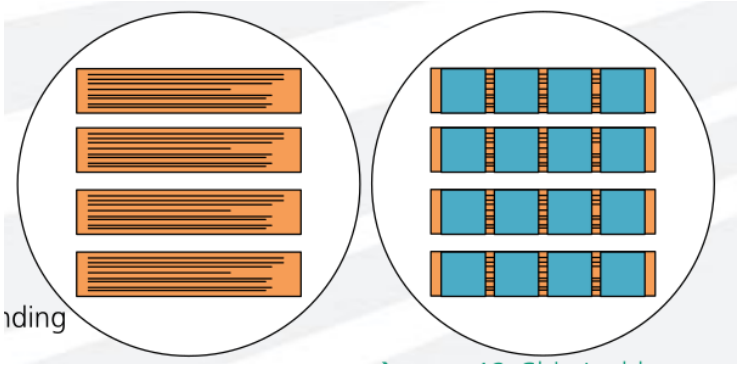
# All-Silicon Modules concept

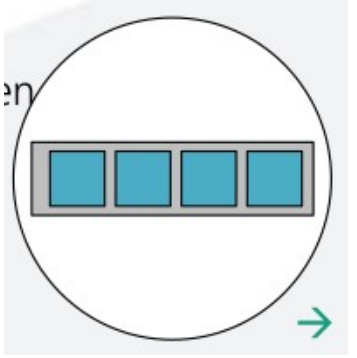


# IZM manufacturing options

Two Options how to produce All-Silicon Modules

- RDL first approach:
  - Build RDL layers on carrier wafer
  - Dice all chips
  - Bond chips on carrier and glue everything together
  - Thinning and carrier removal
- Ladder first approach:
  - Dice ladders (and remaining chips) from wafer
  - Process ladders in a “chip”-process on carrier wafer with RDL layers
  - Thinning and carrier removal





- Wafer level processing not feasible

# IZM manufacturing options: RDL first

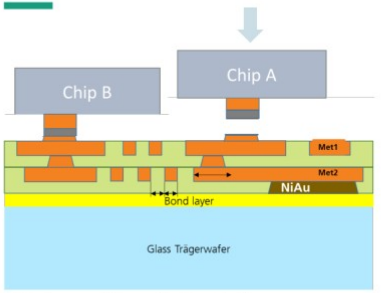
## RDL First Ansatz

Open question:

- What material for mold
- Mechanical properties
- Thermal properties
- Material budget
- RLD thickness

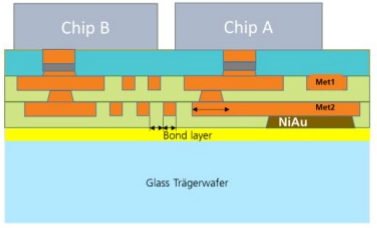
Currently not preferred but possible backup if ladder first approach not working

1



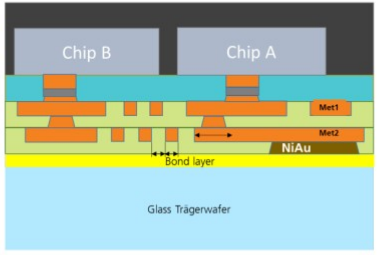

FC Assembly mit CuSnAg

2



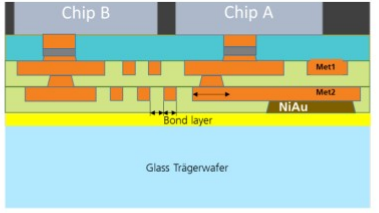

Underfill

3



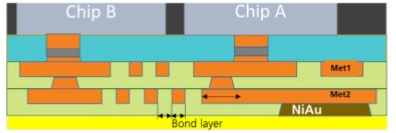

Molding

4



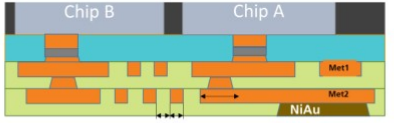

Auf gewünschte Zieldicke Grinden
Sägen

5




Debonden des Trägerwafers

6



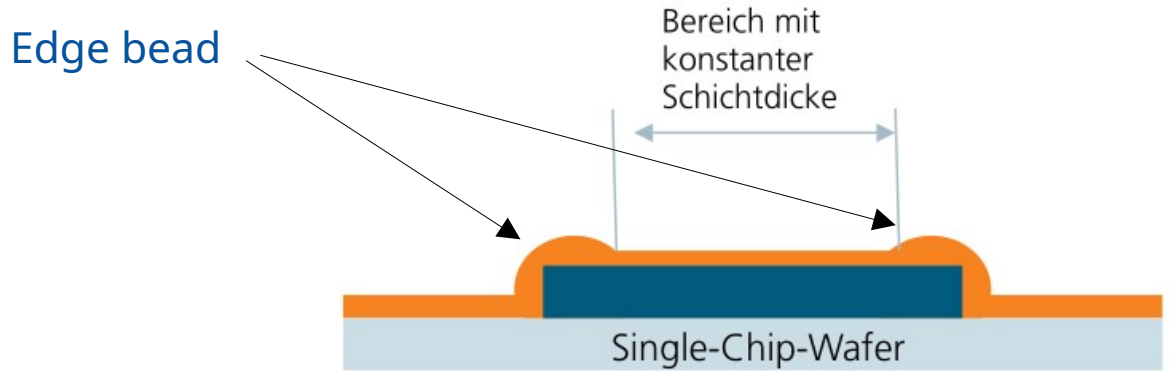

Rückseite:

- Plasmareinigung
- Ätzen der TiW und Au Schicht

# IZM manufacturing options: Ladder first

For ladder first to work:

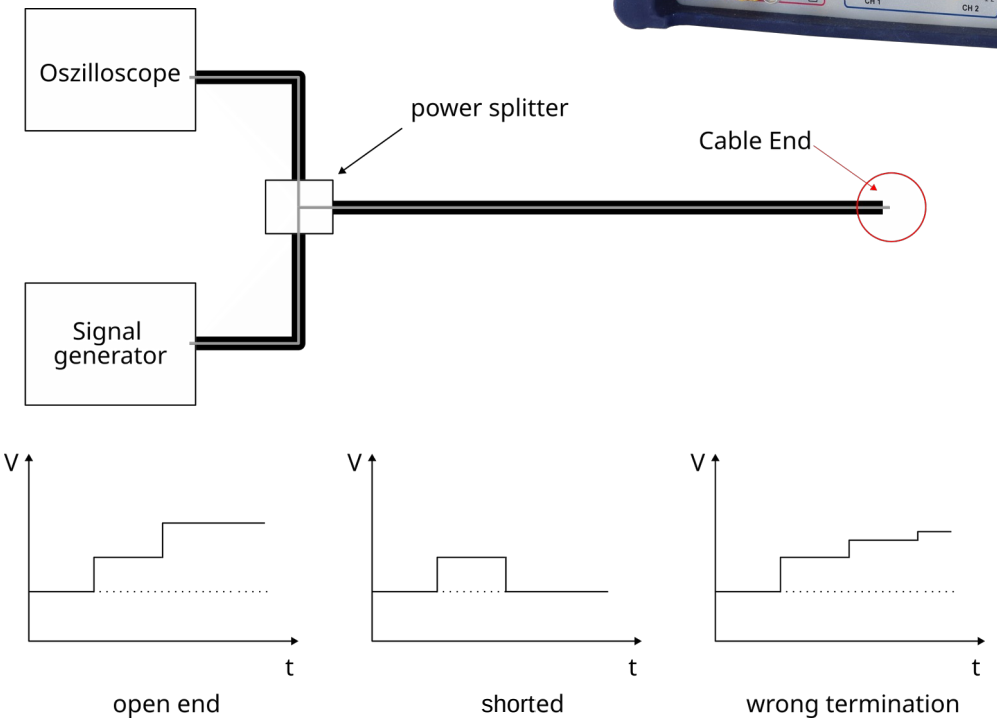
- Need chip structure to each side of the ladder for alignment
- Investgation ongoing reguarding layer thickness on edges and suppression of edge bead
- Cost unclear
  - Process development
  - Obelix prototype
  - Obelix production




Structural chips need chip/pad structures to align on

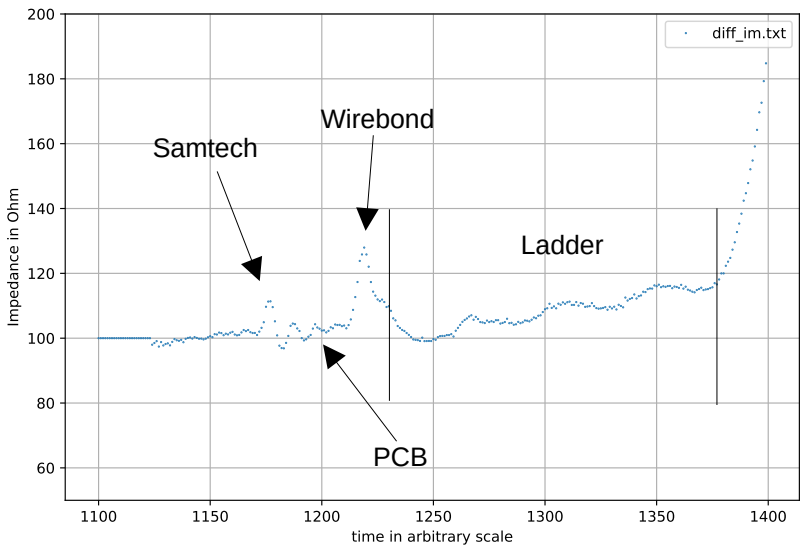
# TDR - Time domain reflectometry

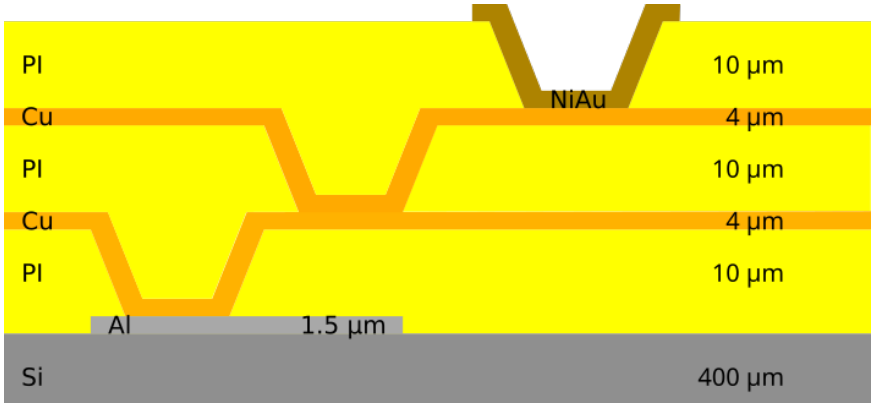

- Send electrical pulse and measure reflection
- Important is sharp edge at the beginning
- Method used to measure
  - Cable length
  - Defects
  - Shorts
  - Changes of impedance
  - Etc.

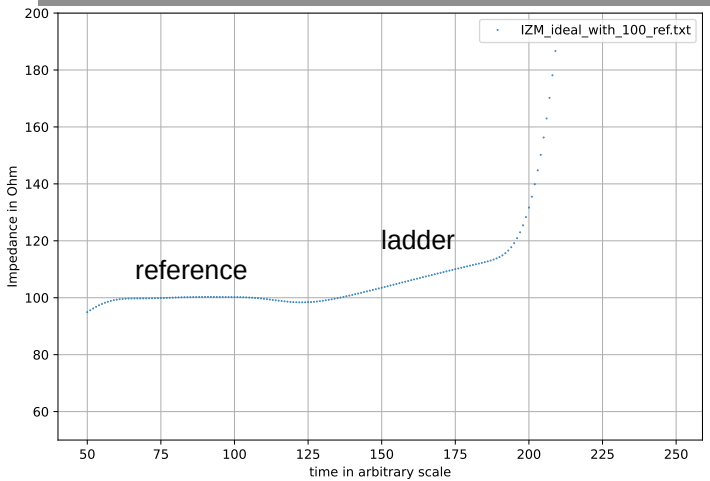


# Layer Stack-up IZM ordered

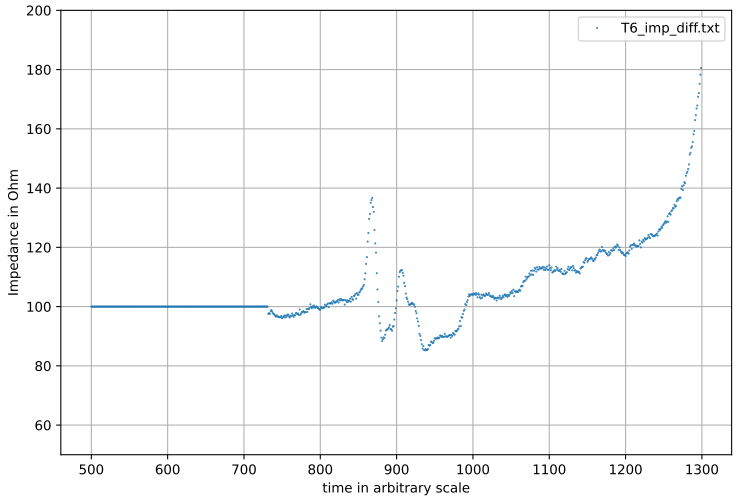
- width/gap: 40/40
- Simulation: $Z_0 = 99.4\Omega$

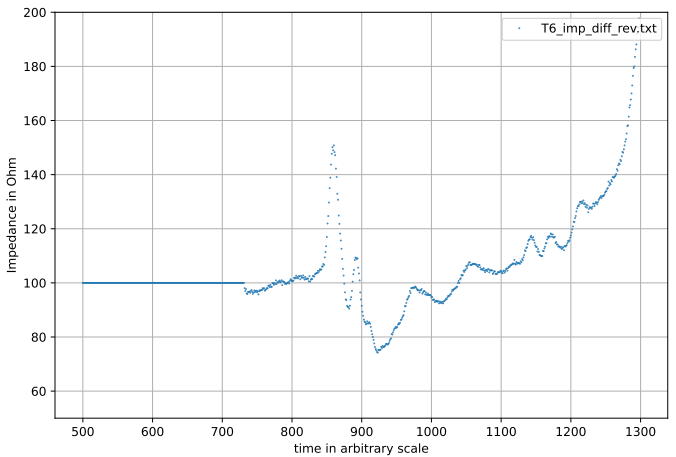


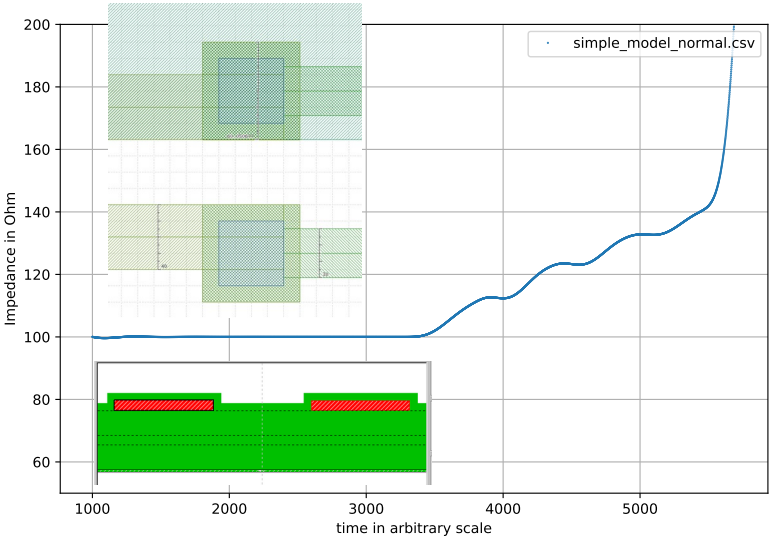



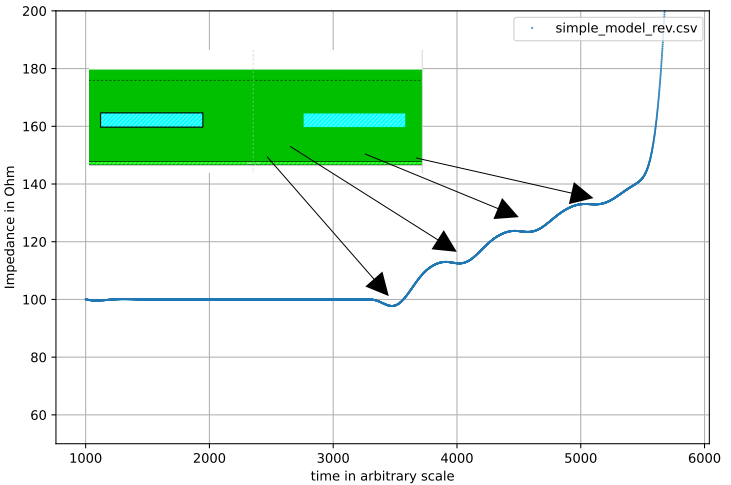



# Layer Stack-up IZM ordered



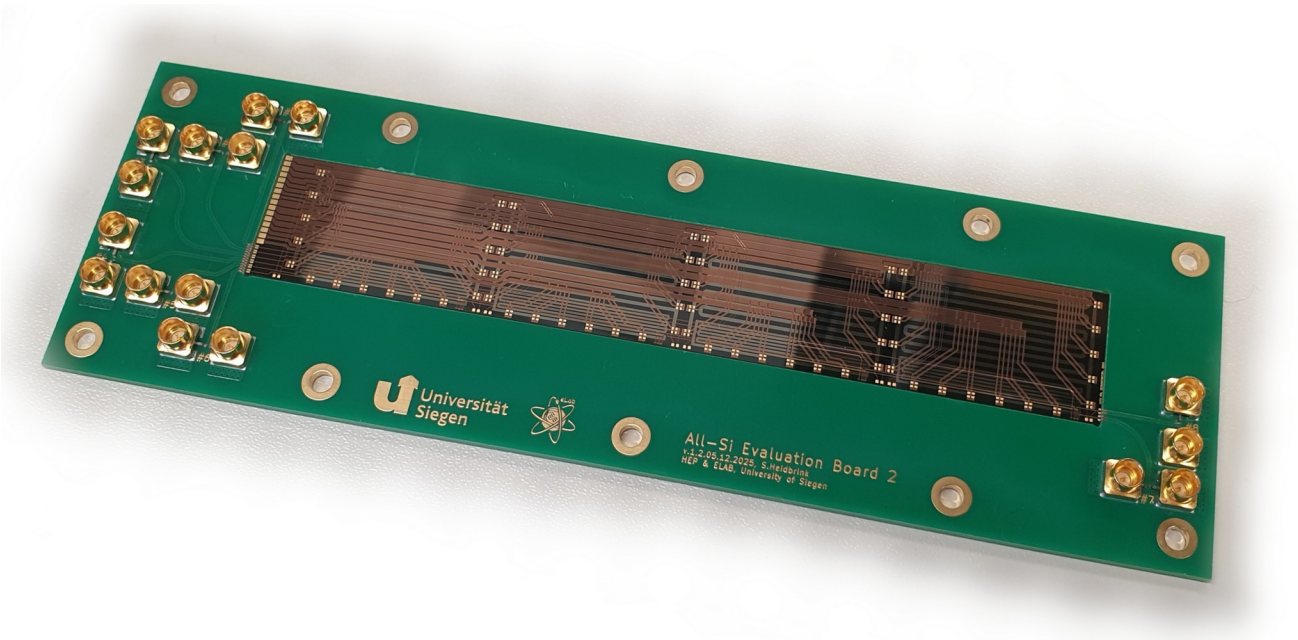



# Eye diagram measurements on IZM modules

- PCB from Siegen used for measurements of TDR and Eyediagram
- Created 8b/10b encoding patter with signal generator
- Measured with oscilloscope

- S-parameter measurements will follow

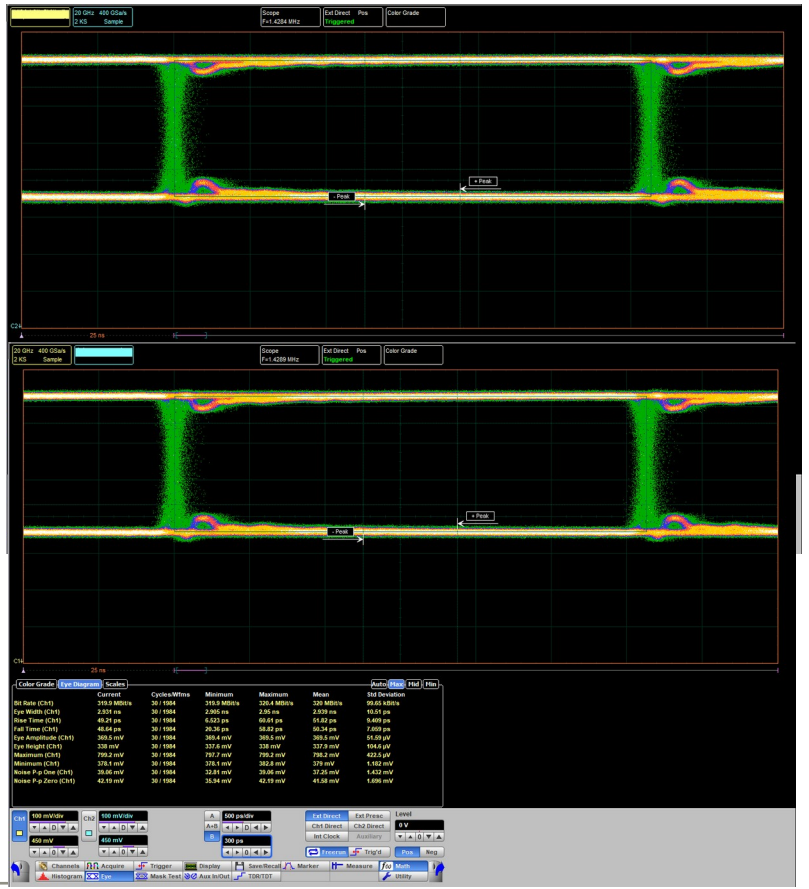


# Eye diagram measurements on IZM modules

- Reference measurement with 20cm long cables
- Measurement on CMD/CLK traces T5 and T6
- Measured each channel individually and differentially

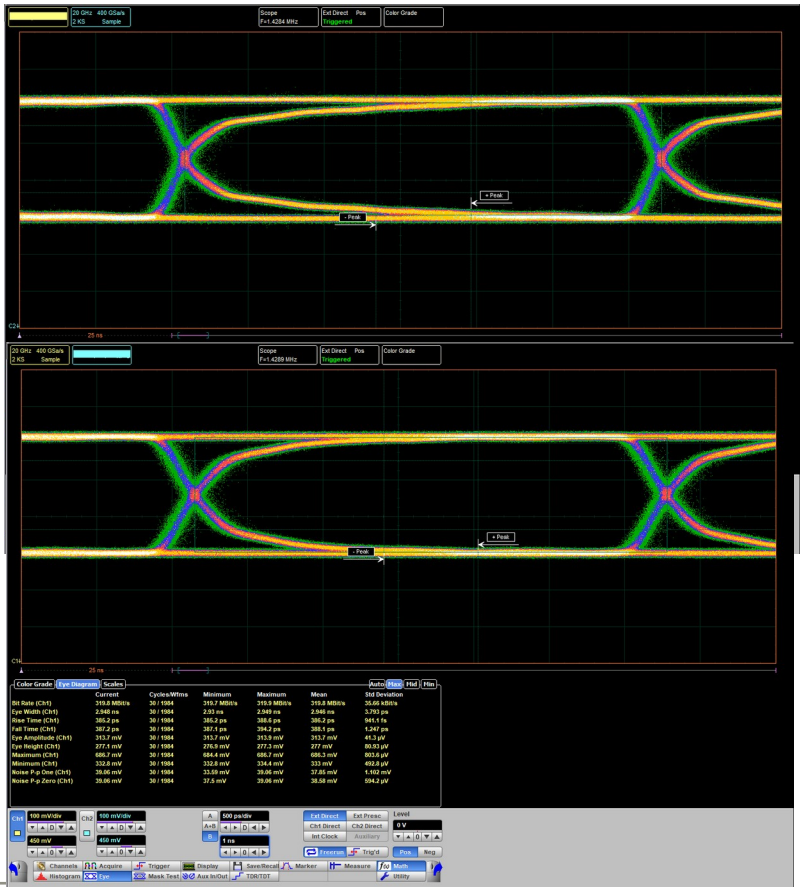
Color Grade | Eye Diagram | Scales — Auto | Max | Mid | Min

| | Current | Cycles/Wfms | Minimum | Maximum | Mean | Std Deviation |
|---|---|---|---|---|---|---|
| Bit Rate (Ch1) | 319.9 MBit/s | 30 / 1984 | 319.9 MBit/s | 320.4 MBit/s | 320 MBit/s | 99.65 kBit/s |
| Eye Width (Ch1) | 2.931 ns | 30 / 1984 | 2.905 ns | 2.95 ns | 2.939 ns | 10.51 ps |
| Rise Time (Ch1) | 49.21 ps | 30 / 1984 | 6.523 ps | 60.61 ps | 51.82 ps | 9.409 ps |
| Fall Time (Ch1) | 48.64 ps | 30 / 1984 | 20.36 ps | 58.82 ps | 50.34 ps | 7.059 ps |
| Eye Amplitude (Ch1) | 369.5 mV | 30 / 1984 | 369.4 mV | 369.5 mV | 369.5 mV | 51.59 µV |
| Eye Height (Ch1) | 338 mV | 30 / 1984 | 337.6 mV | 338 mV | 337.9 mV | 104.6 µV |
| Maximum (Ch1) | 799.2 mV | 30 / 1984 | 797.7 mV | 799.2 mV | 798.2 mV | 422.5 µV |
| Minimum (Ch1) | 378.1 mV | 30 / 1984 | 378.1 mV | 382.8 mV | 379 mV | 1.182 mV |
| Noise P-p One (Ch1) | 39.06 mV | 30 / 1984 | 32.81 mV | 39.06 mV | 37.25 mV | 1.432 mV |
| Noise P-p Zero (Ch1) | 42.19 mV | 30 / 1984 | 35.94 mV | 42.19 mV | 41.58 mV | 1.696 mV |



# Eye diagram measurements on IZM modules T5

- 400mV DC offset + 400mV PP per channel
- Eyes wide open
- Rise time <400ps
- Bit rate 320MHz
- Differential eye amplitude 620mV (>300mV per channel)

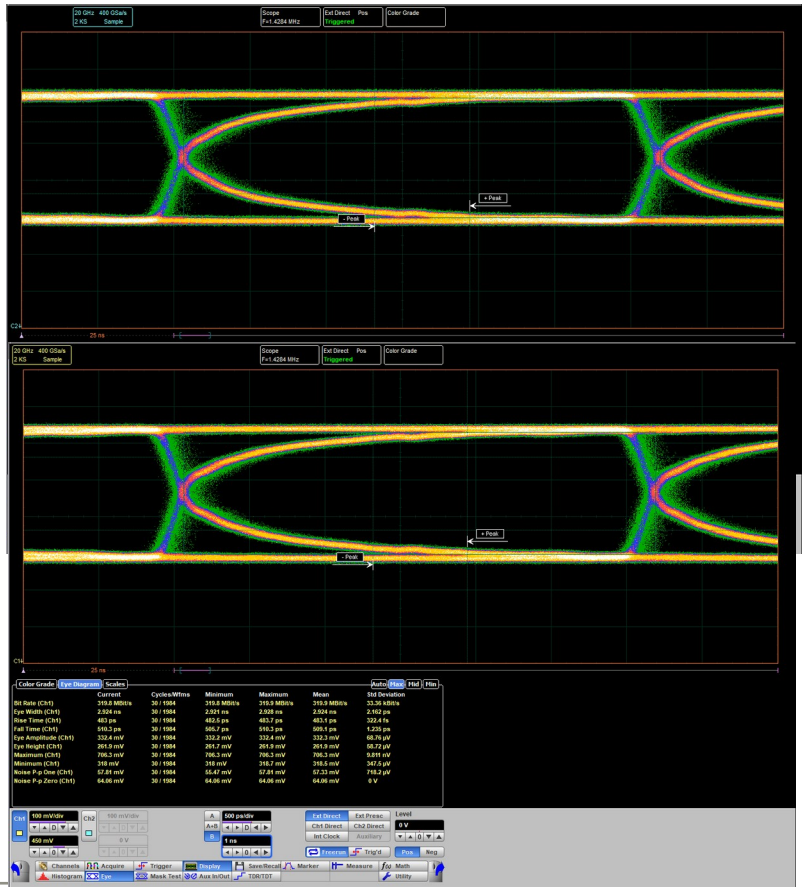


Color Grade | Eye Diagram | Scales — Auto | Max | Mid | Min

| | Current | Cycles/Wfms | Minimum | Maximum | Mean | Std Deviation |
|---|---|---|---|---|---|---|
| Bit Rate (F1) | 319.8 MBit/s | 32 / 2112 | 319.5 MBit/s | 319.8 MBit/s | 319.8 MBit/s | 72.05 kBit/s |
| Eye Width (F1) | 2.948 ns | 32 / 2112 | 2.941 ns | 2.959 ns | 2.947 ns | 4.178 ps |
| Rise Time (F1) | 377.6 ps | 32 / 2112 | 365.9 ps | 378 ps | 376.1 ps | 2.275 ps |
| Fall Time (F1) | 376.4 ps | 32 / 2112 | 372.2 ps | 378.2 ps | 375.5 ps | 1.252 ps |
| Eye Amplitude (F1) | 617.7 mV | 32 / 2112 | 617.3 mV | 617.7 mV | 617.5 mV | 124.1 µV |
| Eye Height (F1) | 525.5 mV | 32 / 2112 | 524.9 mV | 525.5 mV | 525.3 mV | 186 µV |
| Maximum (F1) | 353.9 mV | 32 / 2112 | 353.9 mV | 353.9 mV | 353.9 mV | 9.43 nV |
| Minimum (F1) | -346.1 mV | 32 / 2112 | -346.1 mV | -343 mV | -345.9 mV | 690.1 µV |
| Noise P-p One (F1) | 84.37 mV | 32 / 2112 | 75.78 mV | 84.37 mV | 82.81 mV | 2.278 mV |
| Noise P-p Zero (F1) | 85.94 mV | 32 / 2112 | 78.91 mV | 85.94 mV | 84.99 mV | 1.951 mV |

# Eye diagram measurements on IZM modules T6

- 400mV DC offset + 400mV PP per channel
- Eyes wide open
- Rise time <400ps
- Bit rate 320MHz
- Differential eye amplitude 660mV (>300mV per channel)

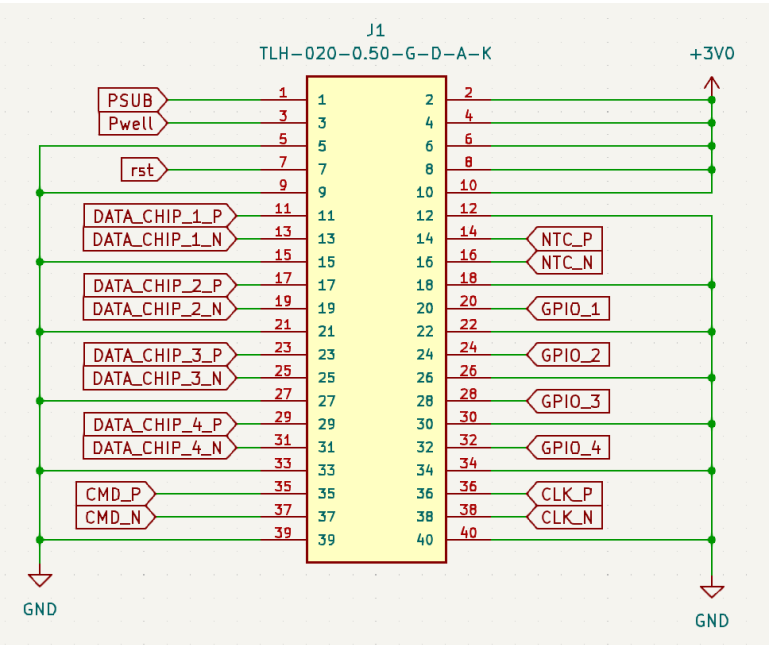


Color Grade | Eye Diagram | Scales — Auto | Max | Mid | Min

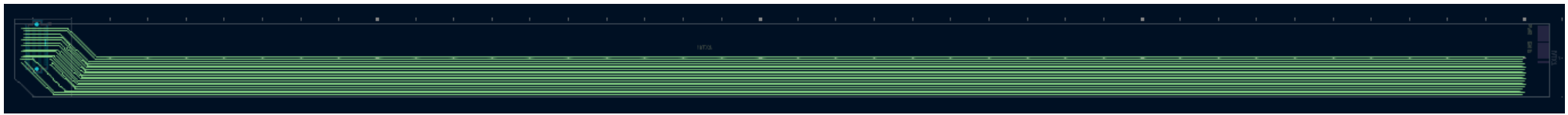
| | Current | Cycles/Wfms | Minimum | Maximum | Mean | Std Deviation |
|---|---|---|---|---|---|---|
| Bit Rate (F1) | 320 MBit/s | 31 / 2048 | 320 MBit/s | 320.1 MBit/s | 320 MBit/s | 9.561 kBit/s |
| Eye Width (F1) | 2.947 ns | 31 / 2048 | 2.947 ns | 2.95 ns | 2.949 ns | 1 ps |
| Rise Time (F1) | 479.2 ps | 31 / 2048 | 479.1 ps | 480 ps | 479.4 ps | 256.3 fs |
| Fall Time (F1) | 491.2 ps | 31 / 2048 | 490.3 ps | 491.3 ps | 490.7 ps | 366.3 fs |
| Eye Amplitude (F1) | 657.4 mV | 31 / 2048 | 657.2 mV | 657.4 mV | 657.3 mV | 48.2 µV |
| Eye Height (F1) | 524.4 mV | 31 / 2048 | 524.2 mV | 524.4 mV | 524.3 mV | 50.86 µV |
| Maximum (F1) | 380.5 mV | 31 / 2048 | 379.7 mV | 380.5 mV | 379.9 mV | 343.7 µV |
| Minimum (F1) | -380.5 mV | 31 / 2048 | -380.5 mV | -380.5 mV | -380.5 mV | 6.58 nV |
| Noise P-p One (F1) | 110.9 mV | 31 / 2048 | 110.9 mV | 110.9 mV | 110.9 mV | 1.104 nV |
| Noise P-p Zero (F1) | 118.7 mV | 31 / 2048 | 114.8 mV | 118.7 mV | 117 mV | 804.5 µV |

# Flex Cable to iVTX

- 3 layer Flexcable with signals in middle, power on top and bottom layer
- Connection to lpGBT PCB via TLH-020-0.50-G-D-A
  Connection to iVTX via wirebond pads
- 4x Chip data, CMD, CLK, RST, 4x ADC_Cal, on ladder NTC, PWR, GND, Sub, Well
- 40cm length (similar to PXD)
  1.9cm width (to fit iVTX ladder)

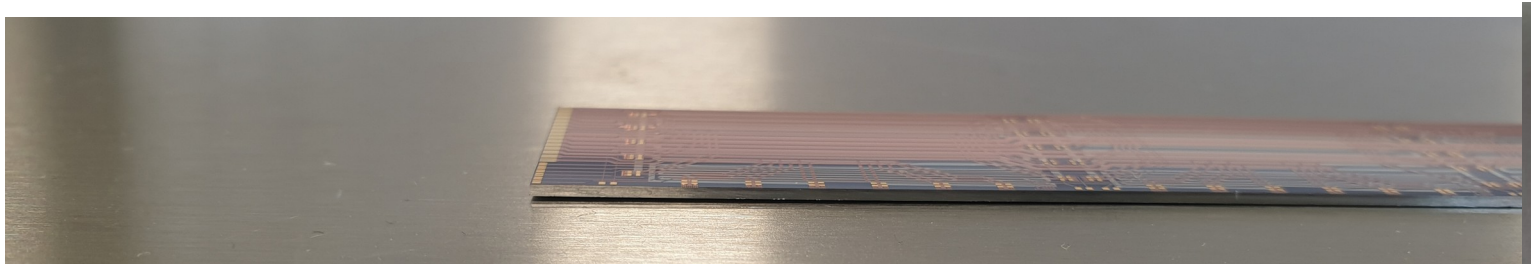






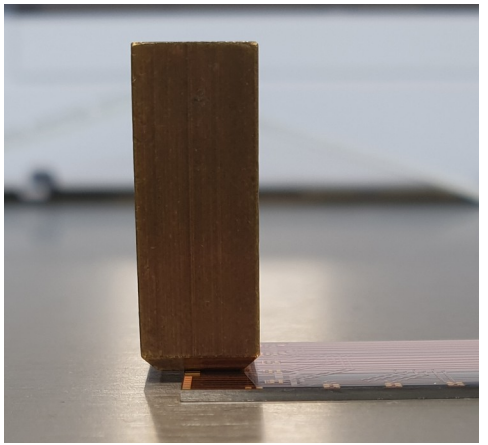
# Bending issues

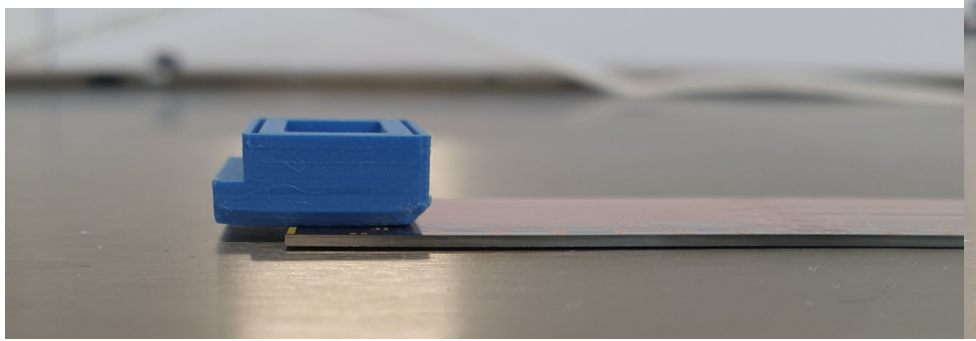
- Quick approximation of bending on IZM modules (725um thickness, 12.5cm length)
- 40g weight on one side, increase weight on other side until bending dissapears

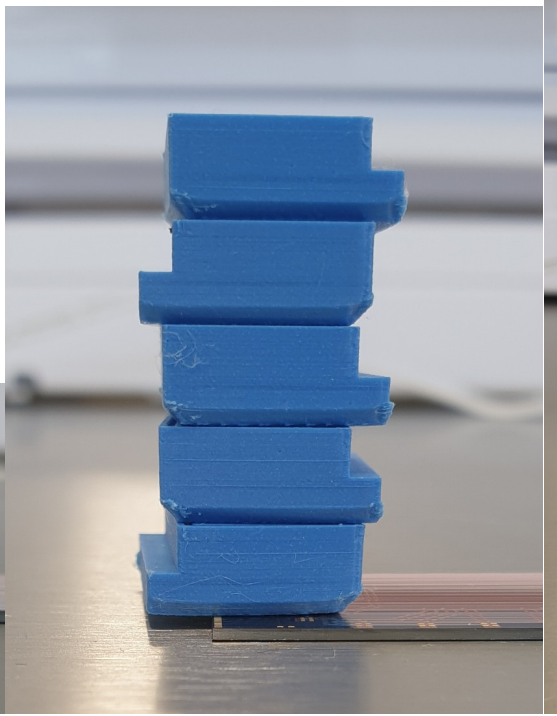


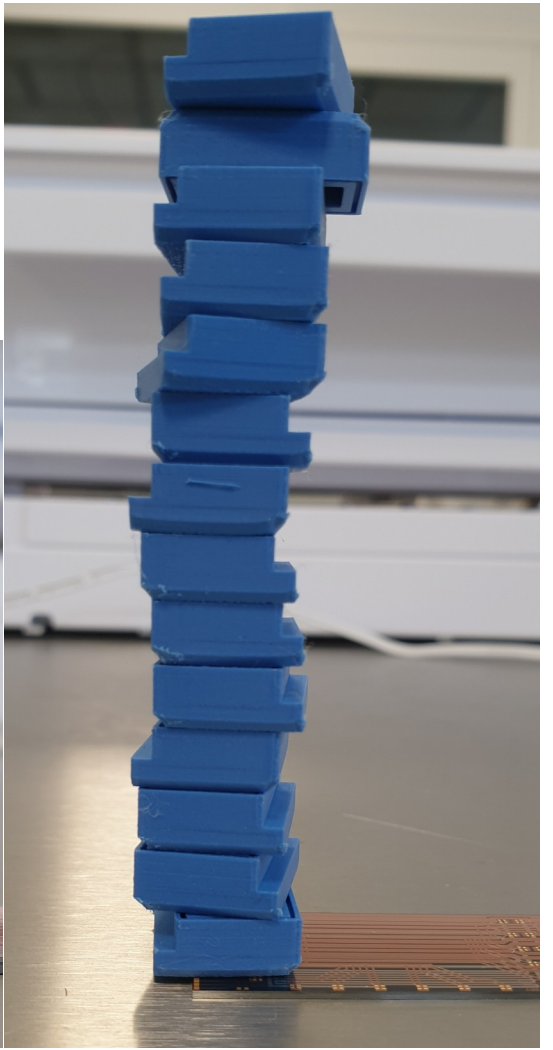
# Bending issues

- Tried with
  - 1 part (0.5g)
  - 5 parts (4.5g)
  - 15 parts (13.5g)
  - 20.5g weight





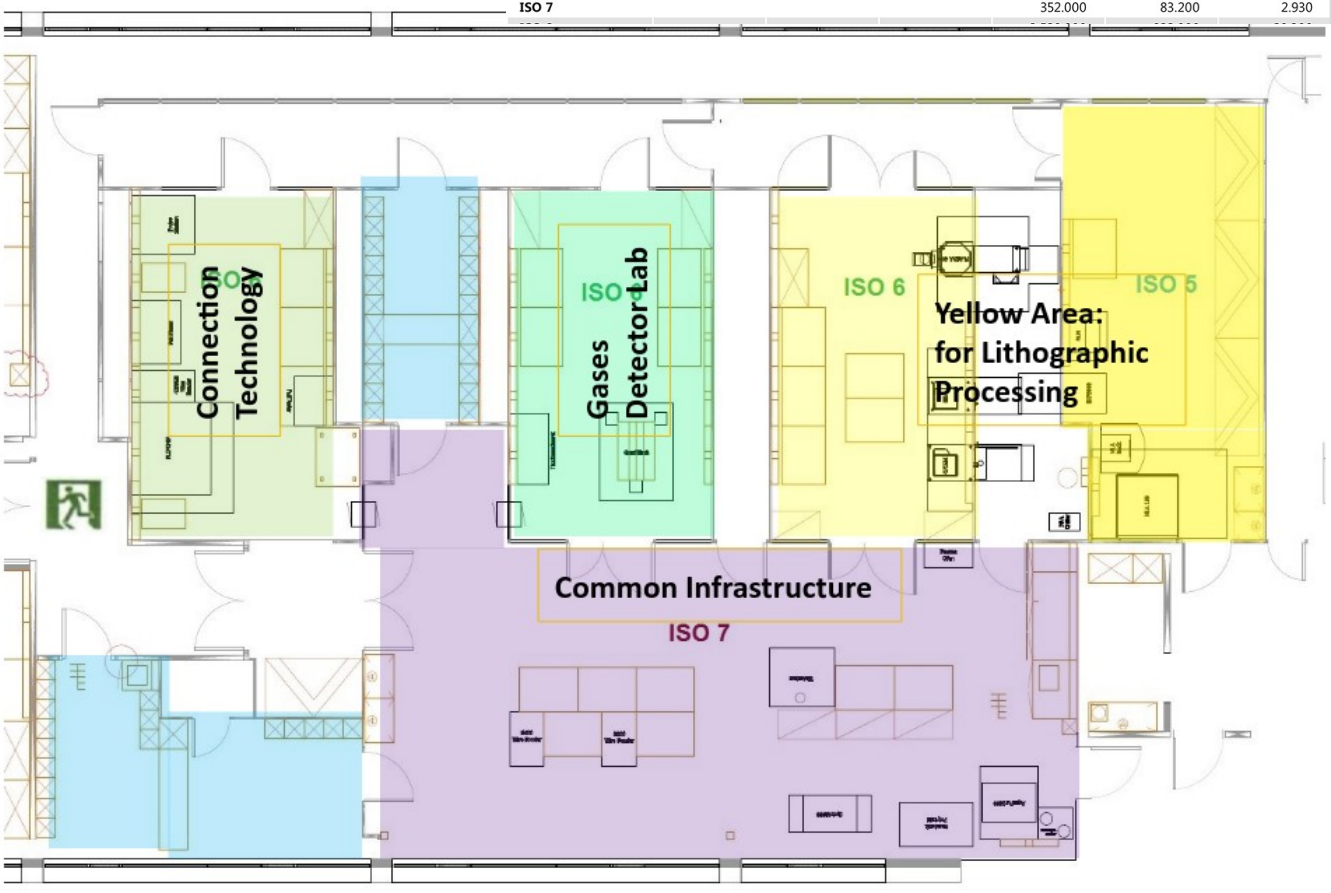




# FTD Cleanroom

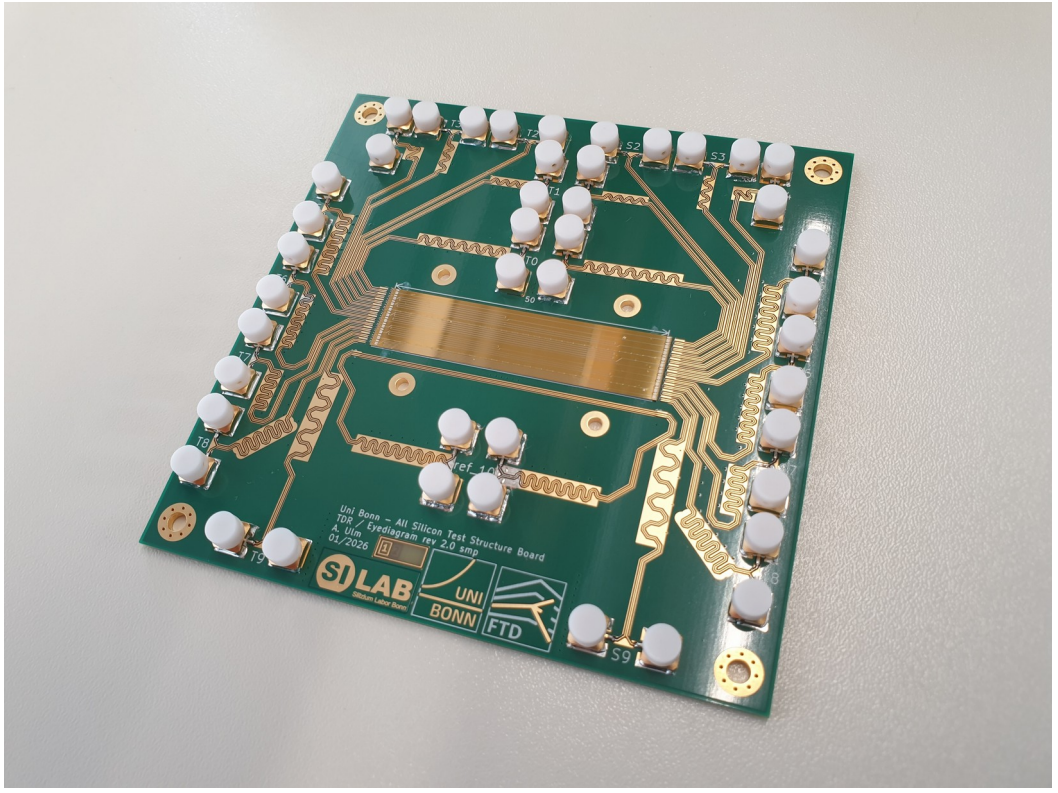
| DIN EN ISO 14644-1 | Höchstwert der zulässigen Konzentration (Partikel je m³) | | | | | |
|---|---|---|---|---|---|---|
| Klasse | ≥ 0,1 µm | ≥ 0,2 µm | ≥ 0,3 µm | ≥ 0,5 µm | ≥ 1,0 µm | ≥ 5,0 µm |
| ISO 1 | 10 | | | | | |
| ISO 2 | 100 | 24 | 10 | | | |
| ISO 3 | 1.000 | 237 | 102 | 35 | | |
| ISO 4 | 10.000 | 2.370 | 1.020 | 352 | 83 | |
| ISO 5 | 100.000 | 23.700 | 10.200 | 3.520 | 832 | |
| ISO 6 | 1.000.000 | 237.000 | 102.000 | 35.200 | 8.320 | 293 |
| ISO 7 | | | | 352.000 | 83.200 | 2.930 |

- ca. 350m² Cleanroom area
- Classes ISO 7 to ISO 5
- ISO 7 currently mostly occupied by ATLAS production
- ISO 6 area assigned to Interconnection Technologies and Wafer probing as well as Gaseous Detectors
- Yellow light area (ISO 6 and 5) used for photolithography processing



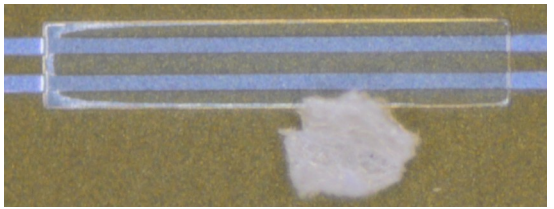
# Self build teststructures

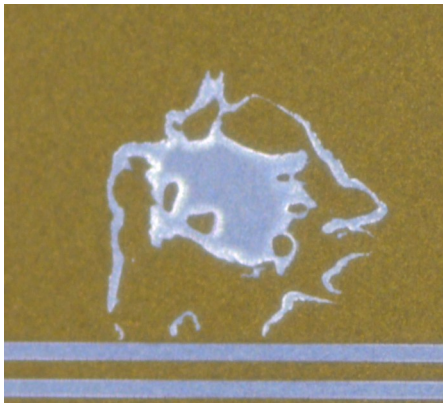
- 5cm to 20cm long test structures produced and bonded to pcb
- Dimensions 40um/40um/3um width/gap/height
- Currently fully aluminum, planned to increase thickness to 6 um and to investigate copper process
- measurements of resistance, TDR and eyediagrams
- Future plans to test transmission properties with FPGA

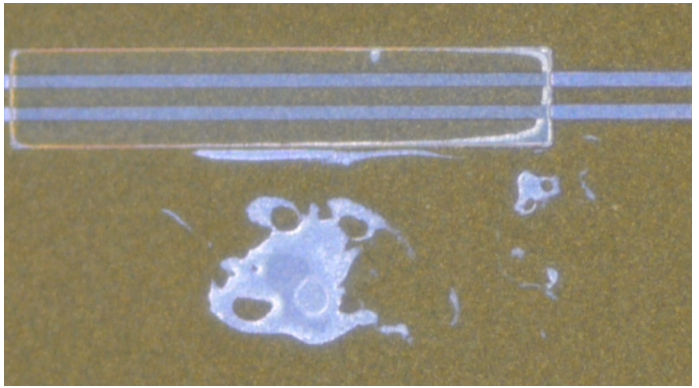


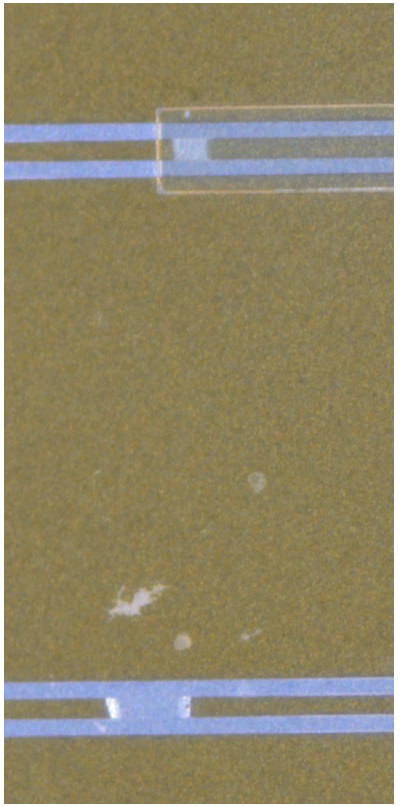
# Some defects (process need refinement)

- Some defects found on the new structures:



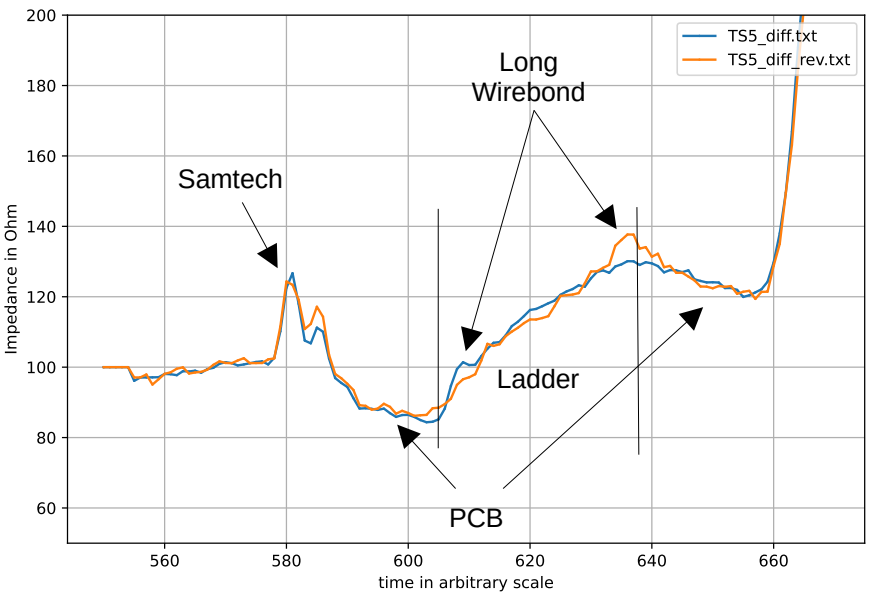


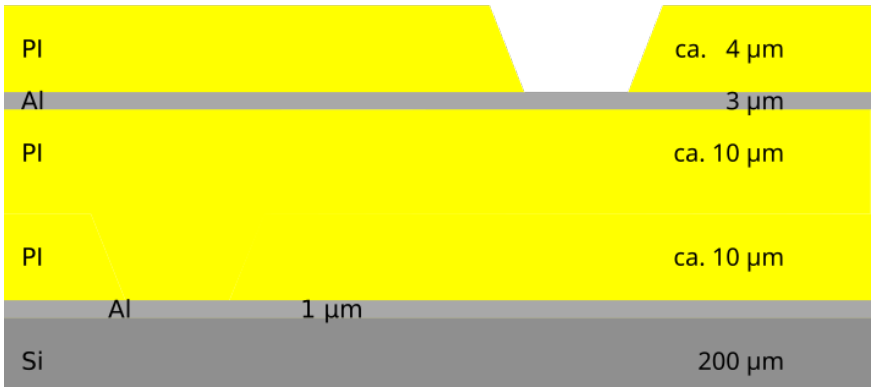


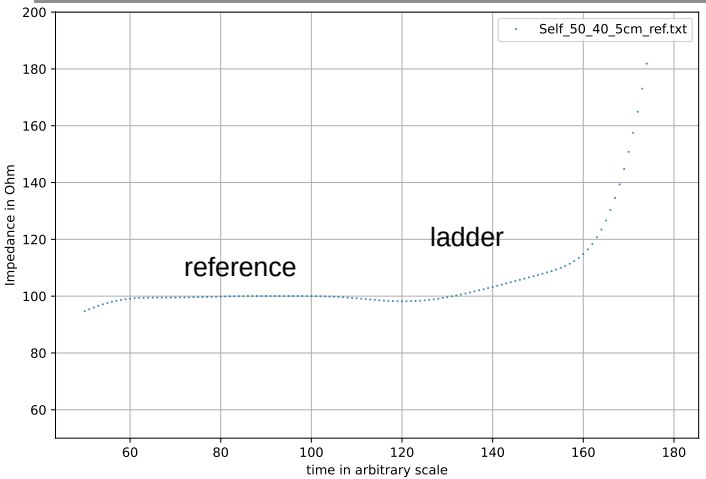


# Layer Stack-up Teststructures FTD

- width/gap: 50/40
- Simulation: $Z_0 = 98.5\Omega$



# Conclusion

- Talking to IZM for new test structures and first Obelix prototypes
  - Two approaches, ladder first preffered
- Impedance measurement agrees well with simulations (simulation of complete design ongoing)
- Eye diagrams show wide open eyes
- Flex cable design soon to be finished
  - Looking for manufacturer, then order and test
- Bending issues quickly investigated, will follow with thinned modules
- New RDL design will be started soon