Update of lpGBT testing for iVTX
April 22 of 2026

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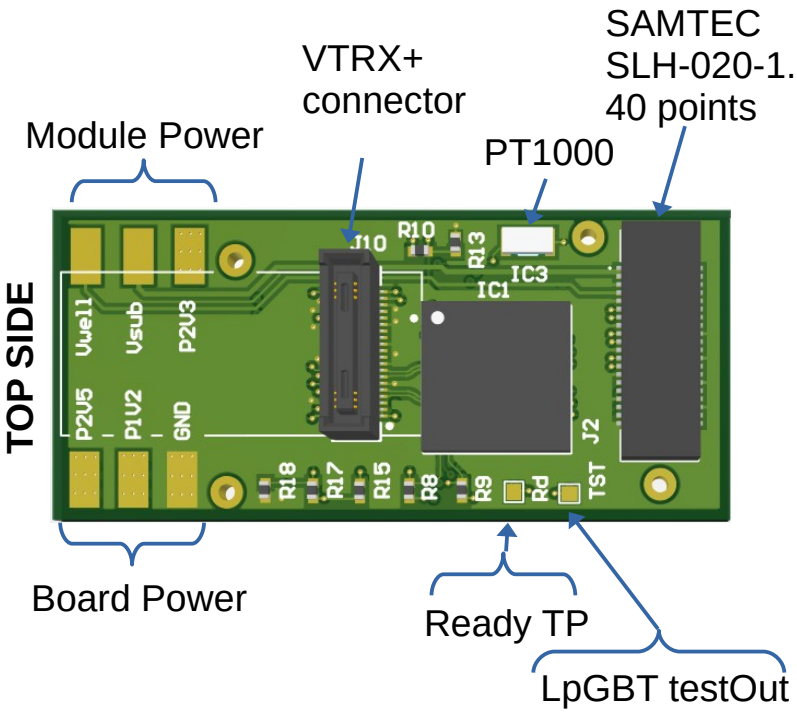
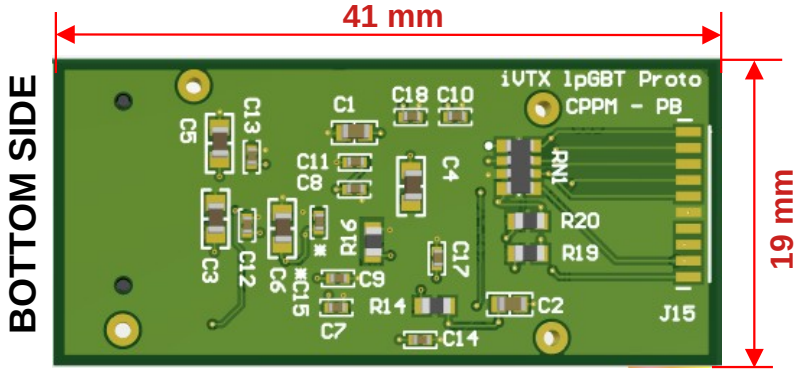
Development of iVTX lpGBT board
Prototype version

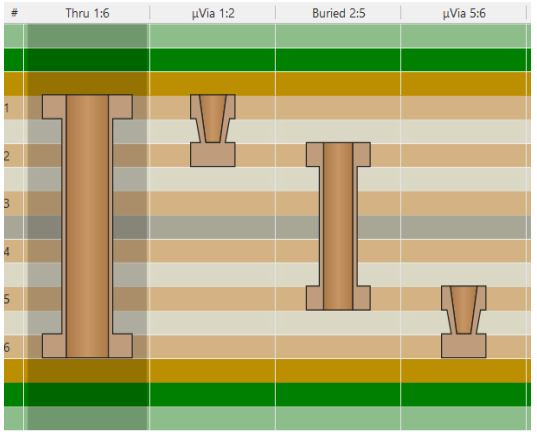
Current patch panel, PCB of 42 x 25 mm²



Total thickness **5.1mm**



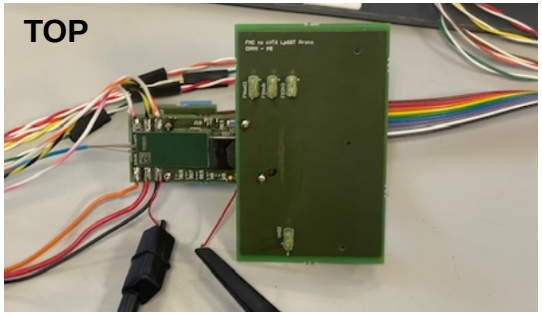
PCB Technology : HDI 6 layers

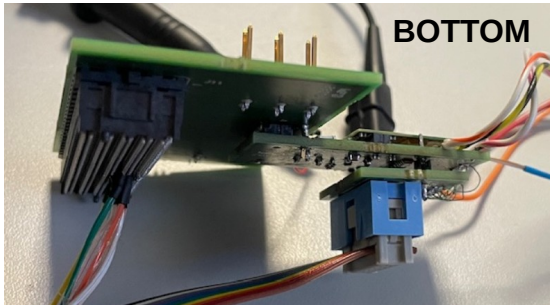


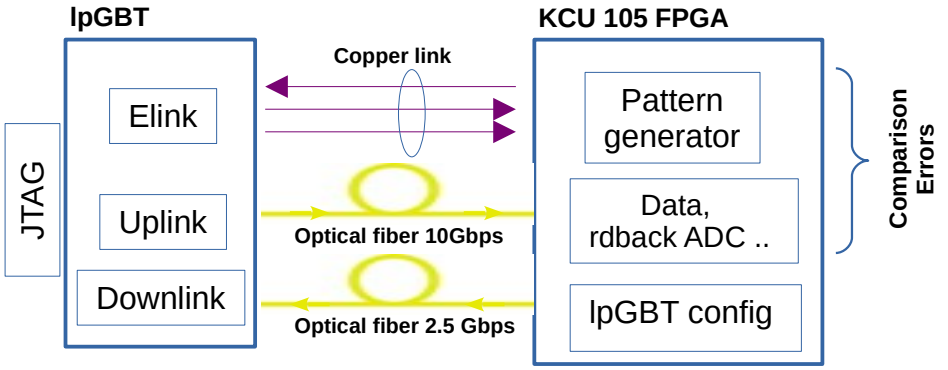
- BGA 0.5mm / 289 pins
- Samtec, 0.5mm
- uVias
- Burried vias

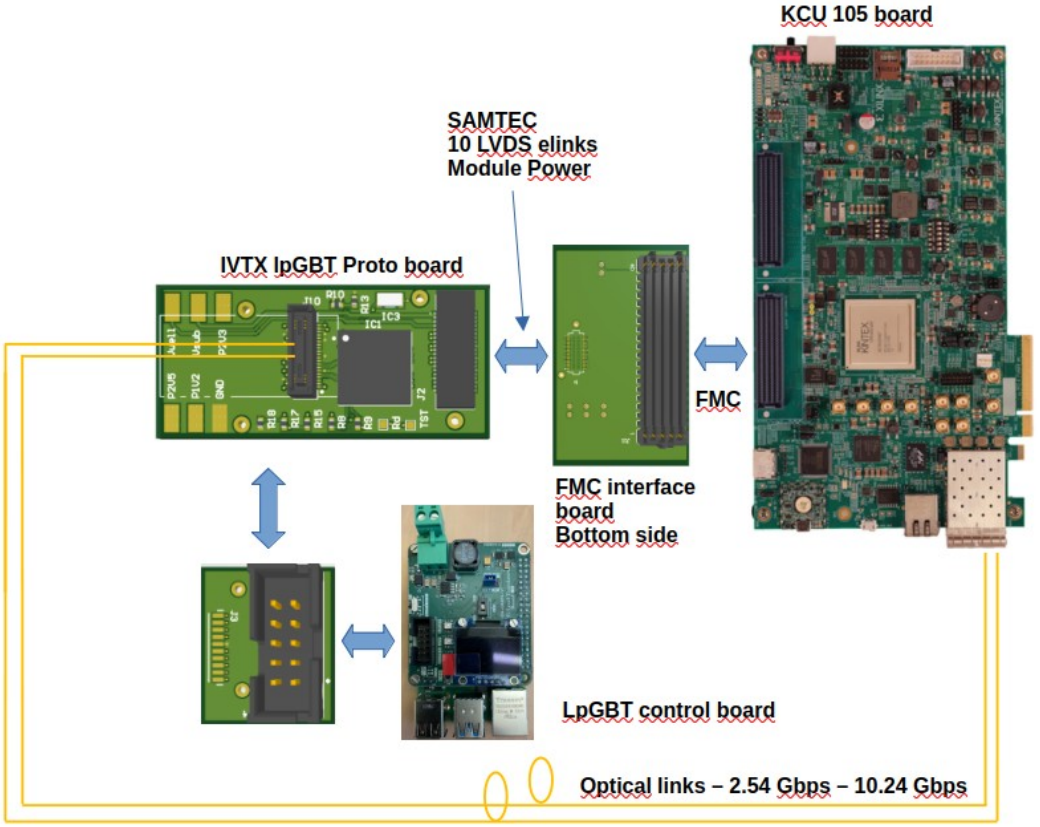
iVTX lpGBT Prototype board setup test

We received boards on third week of february

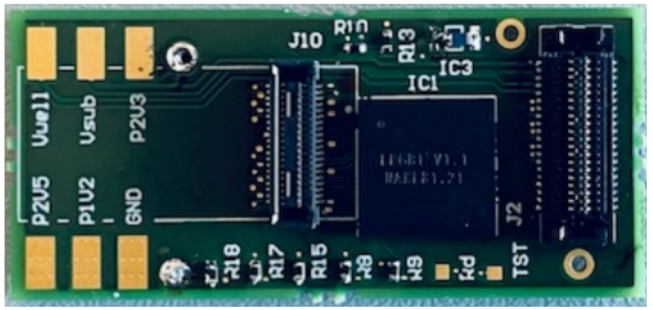








Tests of iVTX lpGBT prototype board



We received boards on third week of february

First tests shows that

- Consumptions
  1.2V => 128mA to 147mA unstable and 2.5V => 53mA stable

- Through the JTAG
  Manage the JTAG manage to read ChipID=acaca35 and version=1
  Status of lpGBT, MODE_10G_FEC5_TRX, RECOVERED_REF_CLK, WAIT_PLL_LOCK

- But stuck on the state **WAIT_PLL_LOCK**, the lpGBT seems to not get data from the FPGA
  We suspected a soldering problem of lpGBT BGA or a bad contact on the VTRX+ connector.

Tests of iVTX prototype board, cn't

After reflow of the board

- Consumptions were stable
  1.2V => 215mA and 2.5V => 53mA

- Manage to get PLL_LOCK => lpGBT_READY state

- Manage to get downlink and uplink communication, reading temperature and VDD, VDDA, VDDTX, VDDRX

Next steps

- Continue the debugging, implementation of the elinks communication (Pattern to lpGBT)

- Make cabling of the second board