中国科学院高能物理研究所
Institute of High Energy Physics
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Belle II Chinese group Activities for VTX WG5

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2n General VTX workshop
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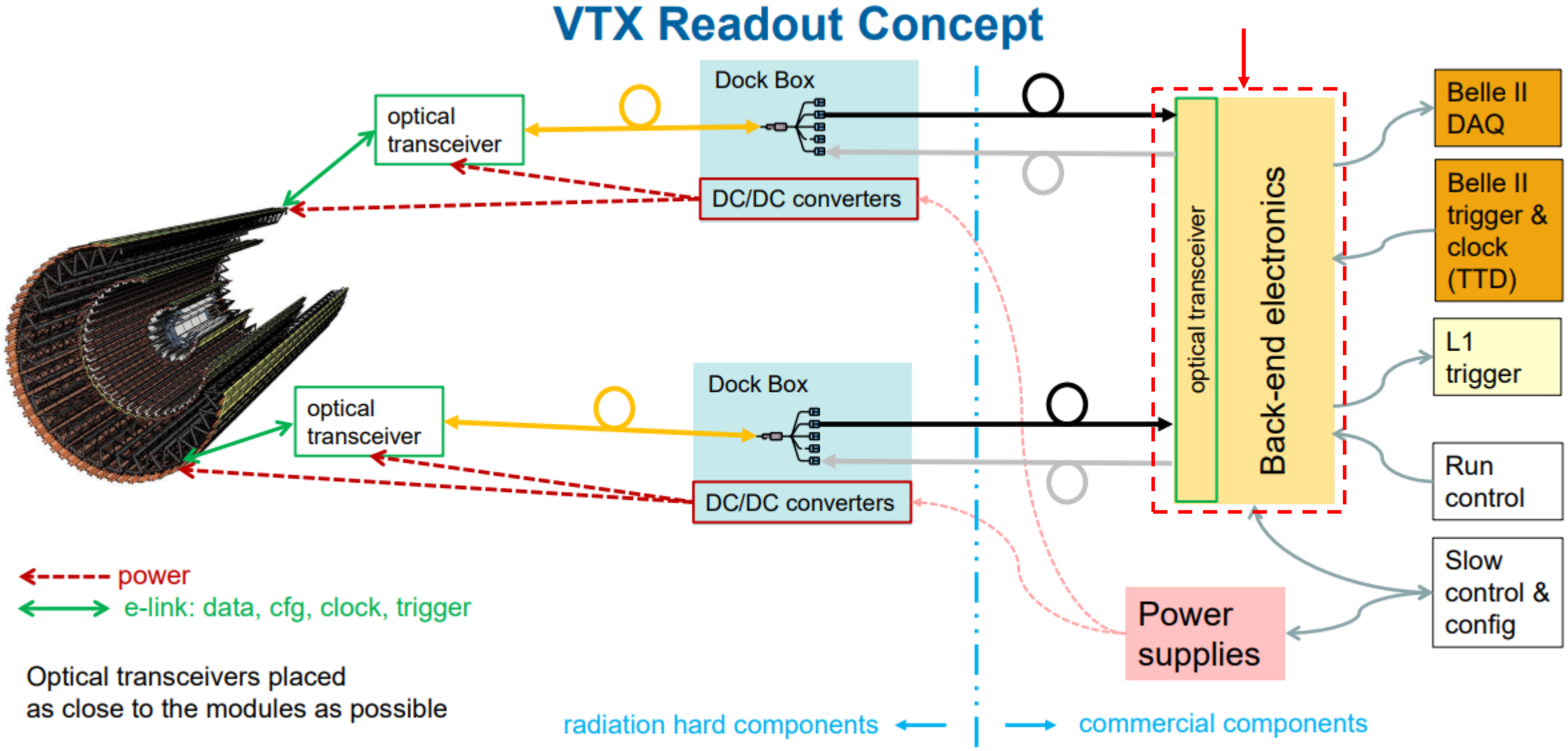
https://indico.belle2.org/event/18167/

Outline

- VTX Readout concept
- IHEP Propose for VTX Backend
- ATCA BE/TRG progress
- Firmware development
- Power supply for VTX
- Summary

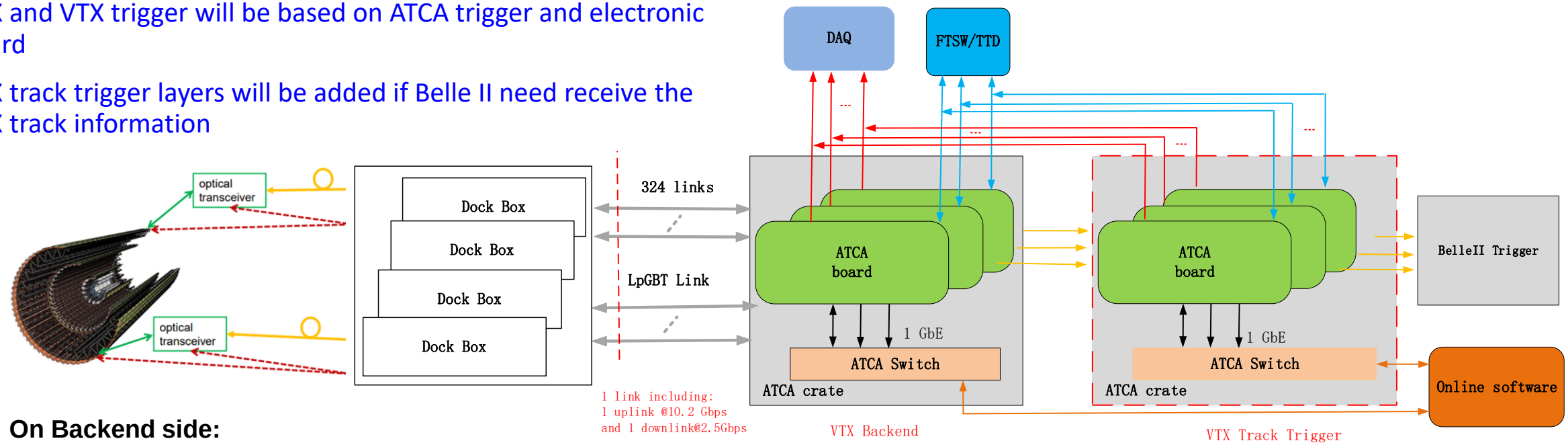
VTX Readout concept



VTX Backend IHEP Proposal

IHEP

- VTX and VTX trigger will be based on ATCA trigger and electronic board
- VTX track trigger layers will be added if Belle II need receive the VTX track information



- **On Backend side:**
  - Receive and decode TTC signals from FTSW and feedback BUSY and Error signal to FTSW
  - Separate the hit data and trigger data;
  - Generate the cluster Trigger Primitive(TP)
  - Send TP data to VTX tracker in pipeline way
  - Package the hit data and TP data based on L1
  - Send data package to DAQ via TPC/RDMA
  - ATCA Switch board as a 1GbE Ethernet switch for Online connection with ATCA board for Slow control

- **On Track trigger side(If needed):**
  - Receive and decode TTC signals from FTSW and feedback BUSY and Error signal to FTSW
  - Receive Cluster TP data and do track finding in section;
  - Send track data to Belle II trigger based on BelleII trigger transmission Protocol
  - Package the TP data and Track data based on L1
  - Send data package to DAQ via TPC/RDMA
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VTX Backend IHEP Proposal(con't)

IHEP

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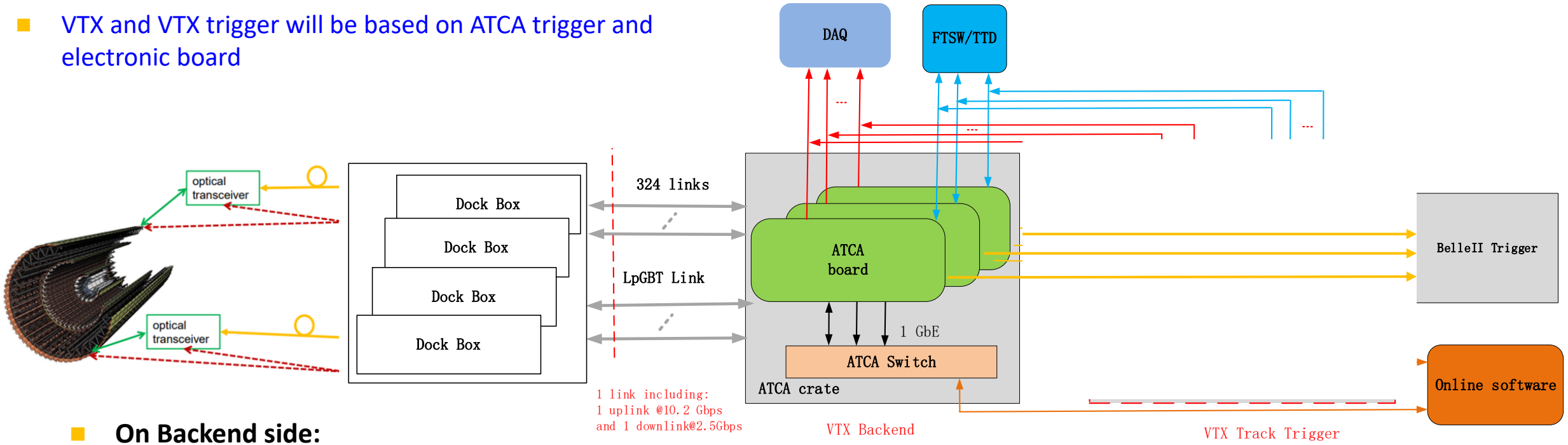

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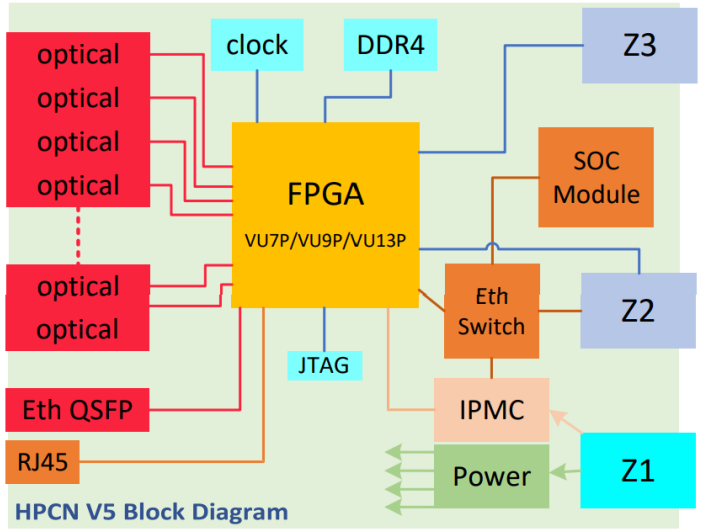
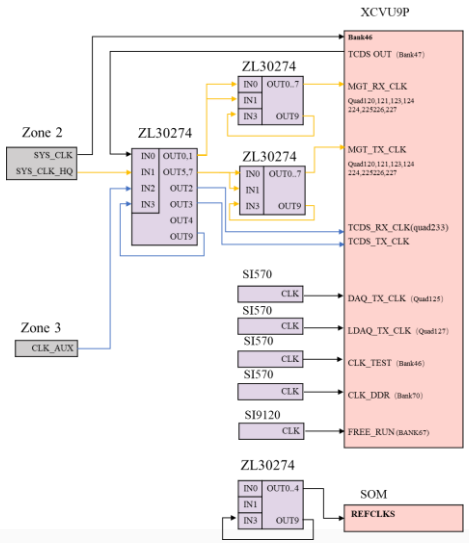
- **On Track trigger side(If not needed):**

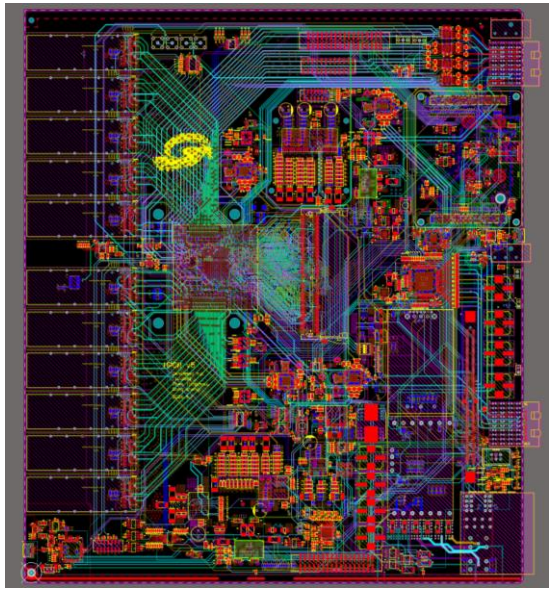
Option1: Common Trigger R&D Board for CEPC

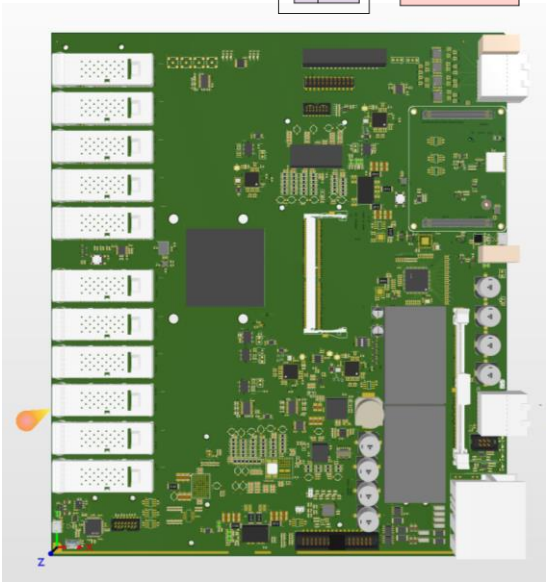
IHEP

- Common Trigger board function list
  - ATCA standard
  - Virtex Ultrascale Plus FPGA(VU9P,VU13P pin compatible)
  - 44 channels for optical, 11 QSFP+
    - Optical channel: 10-25 Gbps/ch
    - 40 channels for links to FEE and Trigger
    - 4 channels for DAQ readout
    - Optical Ethernet or RDMA : 40-100GbE
    - RDMA IP core is under developing
  - DDR4 for mass data buffering:16GB
  - Front 1 GbE and Z2 GbE Fabric port for parameter configuration and control
  - SoC module for board management
  - IPMC module for Power management
  - 8 LVDS In and Out ports connection with Z3
    - RTM can be used for TTC interface with BelleII FTSW/TTC
- Progress update
  - **PCB is under production in factory.**
    - **Will be finished in two months.**
  - **First version is expected at Middle of 2026,**
    - **Performance testing will be started.**
  - ATCA crate manufacturer:
    - https://www.vadatech.com/product-category/chassis-rack-products/
    - https://www.yzitech.com/index.php









Option2: MTCA xFP board first prototype

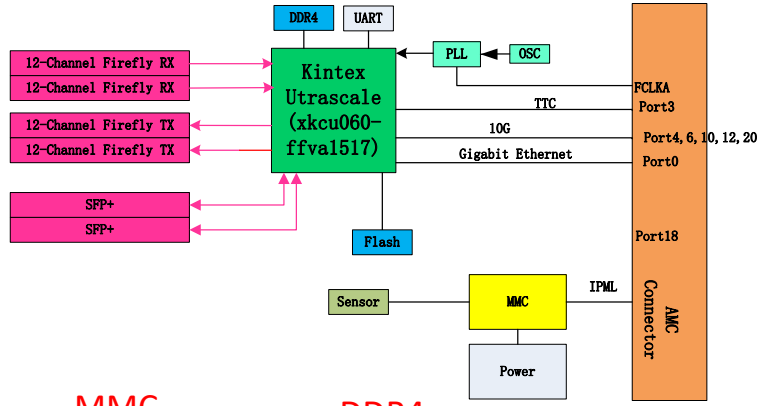
IHEP

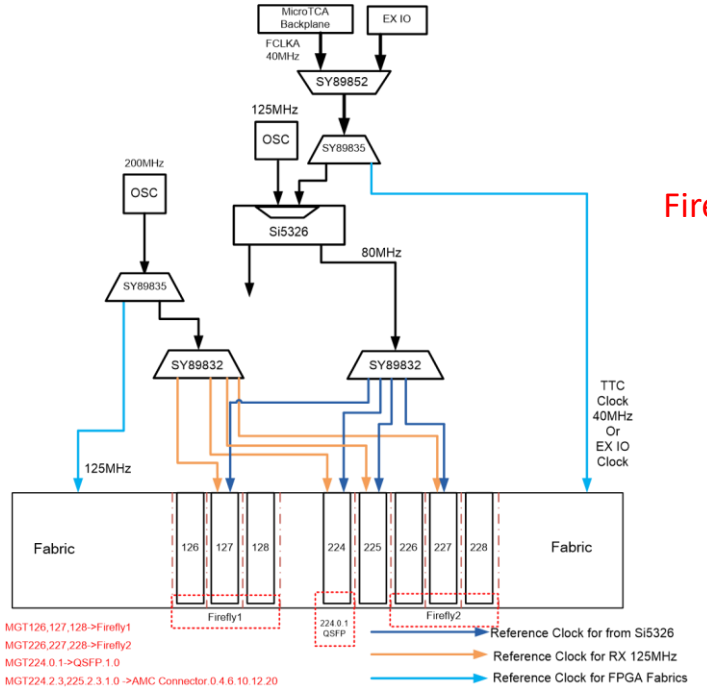
- Function list:
  - MTCA standard
  - KU060 FPGA, pin compatible with KU085, KU095 and KU115
  - GTH+firefly: 24-36 channels up to 16 Gbps/ch
  - DDR4: 16GB
  - Flexible clock tree for clock selection
  - MMC for Power Management
  - EX IO for clock and trigger signal
- Status
  - First version finished,
  - Second version will be modified slightly according to requirement if possible.

Kintex UltraScale Device-Package Combinations and Maximum I/Os

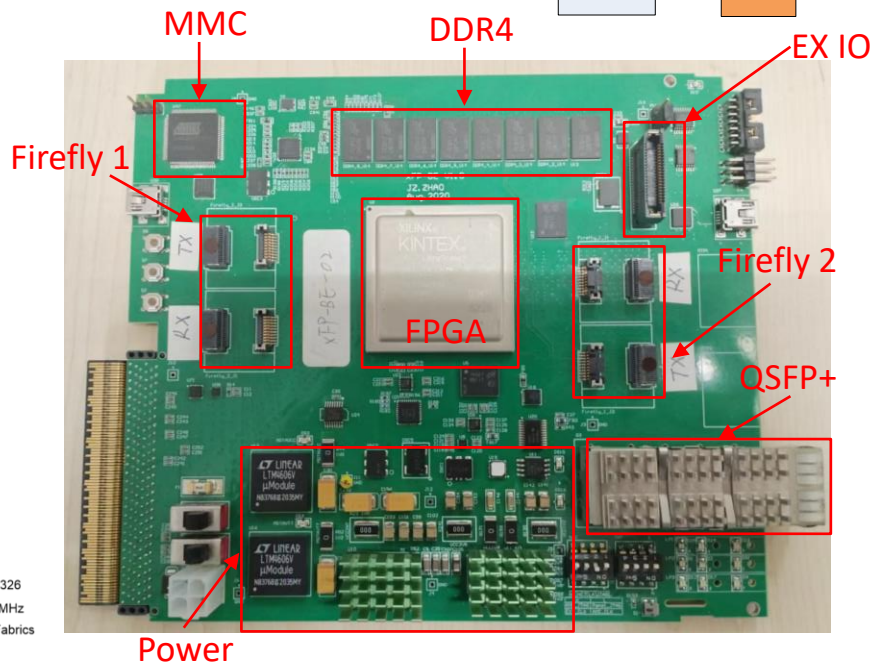
Table 8: **Kintex UltraScale Device-Package Combinations and Maximum I/Os**

Package (1)(2)(3)	Package Dimensions (mm)	KU025 HR, HP GTH	KU035 HR, HP GTH	KU040 HR, HP GTH	KU060 HR, HP GTH	KU085 HR, HP GTH	KU095 HR, HP GTH, GTY(4)	KU115 HR, HP GTH
SFVA784(5)	23x23		104, 364 8	104, 364 8				
FBVA676(5)	27x27		104, 208 16	104, 208 16				
FBVA900(5)	31x31		104, 364 16	104, 364 16				
FFVA1156	35x35	104, 208 12	104, 416 16	104, 416 20	104, 416 28		52, 468 20, 8	
FFVA1517	40x40				104, 520 32			
FLVA1517	40x40					104, 520 48		104, 520 48





Clock tree of xFP



Kintex UltraScale FPGA Feature Summary

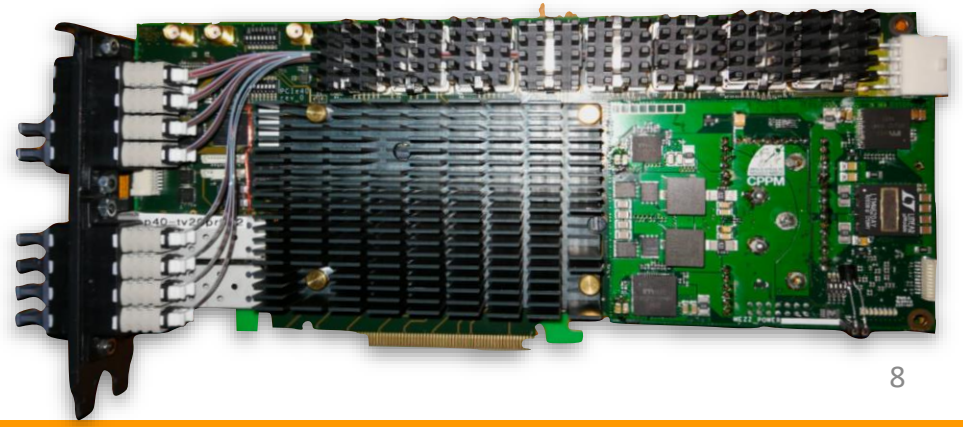
Table 7: **Kintex UltraScale FPGA Feature Summary**

	KU025(1)	KU035	KU040	KU060	KU085	KU095	KU115
System Logic Cells	318,150	444,343	530,250	725,550	1,088,325	1,176,000	1,451,100
CLB Flip-Flops	290,880	406,256	484,800	663,360	995,040	1,075,200	1,326,720
CLB LUTs	145,440	203,128	242,400	331,680	497,520	537,600	663,360
Maximum Distributed RAM (Mb)	4.1	5.9	7.0	9.1	13.4	4.7	18.3
Block RAM Blocks	360	540	600	1,080	1,620	1,680	2,160
Block RAM (Mb)	12.7	19.0	21.1	38.0	56.9	59.1	75.9
CMTs (1 MMCM, 2 PLLs)	6	10	10	12	22	16	24
I/O DLLs	24	40	40	48	56	64	64
Maximum HP I/Os(2)	208	416	416	520	572	650	676
Maximum HR I/Os(3)	104	104	104	104	104	52	156
DSP Slices	1,152	1,700	1,920	2,760	4,100	768	5,520

Firmware development for backend

IHEP, Shandong, Jilin

- The link protocol of lpGPT from frontend to backend
- User logic on backend
- **Clustering algorithm (if needed on the backend)**
- **Trigger algorithm (interest, collaboration with trigger group)**
- A pocket DAQ system with PCIe40 at Shandong Univ.
- It is better to setup a testbench with frond-end and back-end boards



Power supplies for VTX

USTC

- DC-DC Specific requirement
  - Radiation dose (<56 Mrad), magnetic field (1.5 T)
  - Output Current up to 8A
- Survey on DC-DC chips
  - Commercial DC-DC converters (< 100 krad) cannot meet the TID requirement
  - CERN radiation-hardened DC-DC converters
    - ✓ bPOL12V, bPOL2V5 and bPOL48V are widely applied.
    - ✓ bPOL12V has reliability issues in certain situations, particularly after irradiation, thermal cycling, and repeated enable/disable operations.

	Model	Vin	Vout	Output Current/Power	TID	MAG (Gauss)
CERN	FEAST2.1/FEAST2.3	5 ~ 12 V	0.9 ~ 5 V	0~4 A	>200 Mrad(Si)	40000
CERN	bPOL48V_V2	13 ~ 48 V	0.6 ~ 24 V	0~10 A	>50 Mrad(Si)	40000
CERN	bPOL12V_V6	5.5 ~ 12 V	0.63 ~ 5 V	0~4 A	>150 Mrad(Si)	40000
CERN	bPOL2V5_V3.3	2.1 ~ 2.5 V	0.6 ~ 1.5 V	0~3 A	>100 Mrad(Si)	40000
CERN	AMIS2	6 ~ 11 V	1.2/1.8/2.5/3.3/5 V	0~3 A	300 Mrad(Si)	40000
MAGICS	MAG-PSU00001-NP	5~11 V	0.9~5 V	0~4 A / 0~10 W	> 100Mrad(Si)	40000

Back-end power units

Manufacturer	Model	Output voltage	Output current	Output channels	Ripple
CAEN	A2551	0–8 V	12A	8	<5 mVpp
CAEN	A2552	0–16 V	6A	8	<5 mVpp
CAEN	A2553	0–32 V	3A	8	< 8 mVpp
CAEN	A2554	0–64 V	1.5 A	8	< 8 mVpp
CAEN	A3006	4–16 V	6A	6	<20 mV pp on 10 µF // 0.1 µF 10 Hz-15 MHz

Summary

- Belle II China (IHEP, USTC, Jilin, Shandong) made some progress related with WG5
  - Proposal of BE structure updated with ATCA/MTCA board developed by IHEP.
  - Testbench of Front-end will be helpful for firmware development.
  - Collected requirements and surveyed on DC-DC chips: DC/DC converters, design

Thanks !

Back-End Electronics Tasks

- Collect lpGBT data from front-end via optical links
- Data stream contains 4 types of data:
  - Hit data: particle hits = physics data
  - Trigger data from TTT: input for L1 trigger, need low latency readout
  - OBELIX configuration and register values: read on demand, are sent via hit data path
  - Monitoring data from lpGBT ADC, e.g. temperature probes, voltages, etc.
- Data handling
  - Unpack and split lpGBT data into individual data streams
  - Discard OBELIX IDLE patterns
  - Forward these data streams to
    - DAQ: hit data
    - Trigger system: TTT data with low latency
    - Slow control SW: monitoring data
- Receive configuration from run and slow control and forward it to lpGBT and OBELIX chips

Answer to questions in Jingzhou‘s presention

- Koga-san sent answers to the questions raised in Jinqzhou's presentation:
- What does Belle-II trigger need from VTX?
  - Now our baseline(?) plan to perform track **reconstruction in CDCTRG and VTXTRG independently**. After that, track matching between VTXTRG and CDCTRG is performed by using phi (possibly theta too) information on GRL.
    So, at least VTX trigger need to send track information of phi, theta, pt in each track to TRG system of GRL.
  - As an alternative plan, if we perform **combined track reconstruction of CDCTRG and VTXTRG** as Torben mentioned, **we need raw hit level information of VTXTRG**. (in page11 of Torben's presentation at Belle II Trigger/DAQ Workshop 2025)
    It might be interesting idea in future, but for now, there is no study at all and it is difficult to determine what information we need.
    Compared with baseline plan, we need much larger bandwidth to send such raw hit information to GRL.
- What is the maximum latency allowed for VTX backend?
  - After LS2, total maximum latency is around 9μs.
    With baseline plan, VTXTRG needs to send the track information to GRL by 7μs (2μs earlier than 9μs).
    I guess between VTXTRG and GRL, additional board (UT4/5 or IHEP board) is needed to merge all VTXTRG track from all VTX backend. I am not sure how much latency it takes, but let's assume it as 1μs.
    If so, all up-link process from OBELIX chip to TTT data processing should finish by 6μs
- Data transmission protocol with Belle-II trigger?
  - We have our custom developed protocol with GTH/GTY.
  - We would like to ask you to use common protocol. We can share source code etc. at any time.