Requirements on the Interface between VTX back-end and Belle II Trigger (and event timing resolution)

2026/4/22

T.Koga

Contents

-Share and discuss requirement from TRG to VTX

- -optical transceiver bandwidth to send TTT data from VTX backend to TRG
- -L1 event timing resolution for VTXDAQ

Requirements on the Interface between VTX back-end and Belle II Trigger

requirement for VTXTRG

-1. all hits should be sent from VTX to VTXTRG with pipeline
(=no deadtime, fixed latency, independent from hit occupancy)

-2. VTXTRG efficiency is >~95% or more for single charged particle from IP

-3. fake track rate is < ~1000kHz(~10% per 100ns) for CDCTRG matching
(in the case of standalone VTXTRG, it is well less than 30kHz)

-4. VTXTRG ϕ resolution is better than ~5degree for CDCTRG matching

-5. VTXTRG z resolution is better than a few cm to reject off-IP particles

-6. track trigger latency from VTX to GRL is 7~8μs
(assuming 9μs is required to entire TRG after LS2)

taken from
1st VTX workshop

This (and Strixels segmentation) will determine needed total bandwidth between VTX backend and TRG

Assumption for discussion

-TTT data is sent from OBELIX chip to ipGBT+VTRx+

-TTT data is sent from ipGBT+VTRx+ to backend board

-TTT data is send from backend board to TRG module

-no trigger logic on backend board, all hit data is passed to TRG(UT4,UT5,UT6)

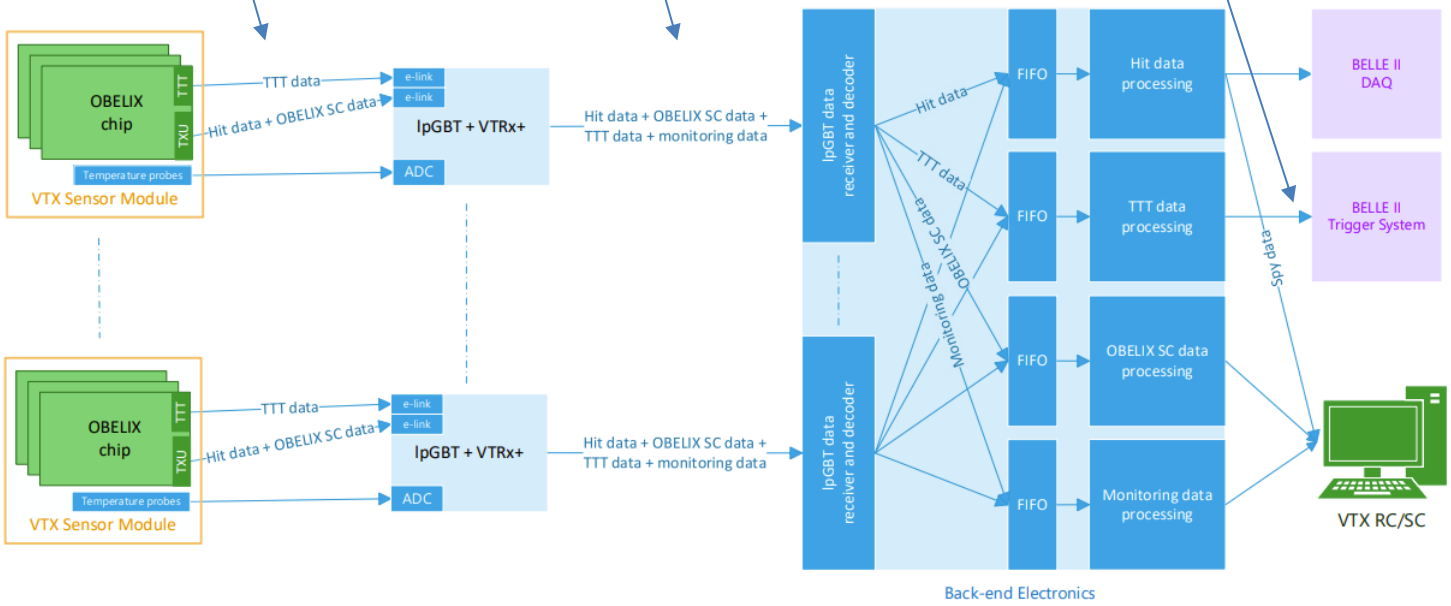


figure taken from 1st VTX workshop (link)

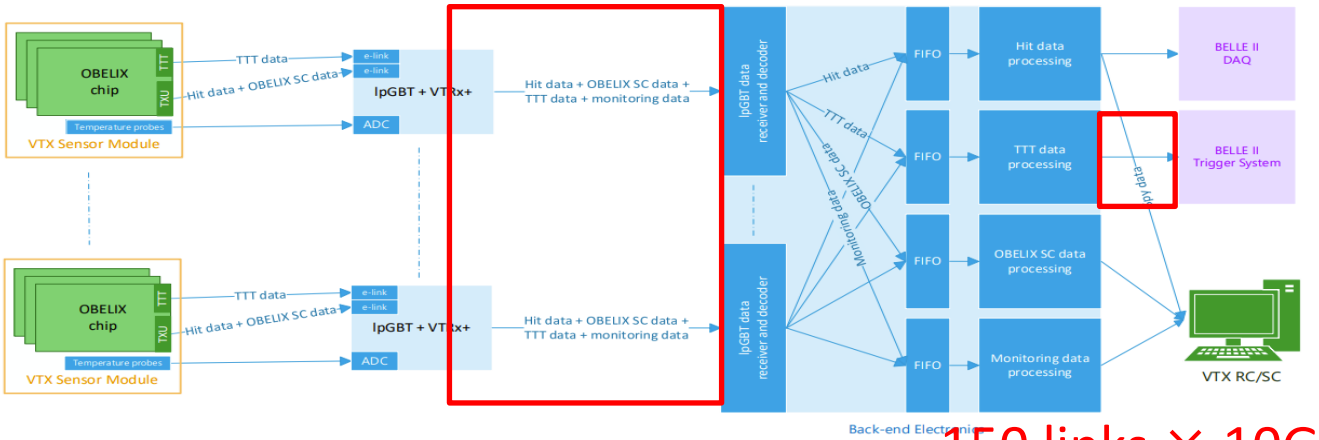
Bandwidth from IpGBTs to backend

-Information from Christian Irmer (thanks!)

-From IpGBTs to backend, total bandwidth for TTT is 150 links × 10 Gb/s

- -We have about 300 optical links from IpGBTs to VTX backend
- -each have 2 e-links with 10Gb/s, about 50% data will come from TTT
- -In total, 300× 10Gb/s × 50% = 150 × 10 Gb/s
- -(does this 300 include inner VTX, which does not have TTT ??)

-Same total bandwidth (＋α, chipID etc.) is needed from backend to TRG



300 links × 10Gbps
(half come from TTT)

150 links × 10Gbps or
60 links × 25Gbps or
46.875links × 32Gbps

transceiver speed from backend to TRG(UT)

-The number of needed UT4/UT5 board depends on transceiver speed
 -UT4 has:　32 link × 25Gbps and　32 link × 12Gbps
 -UT5 has: 64-96 link × 32Gbps and 16-32 link × 58Gbps　(not fixed)

Speed between backend and TRG	Needed #link	Needed number of UT (#needed link/#UT link)
10Gbps	150	UT4 × 5 or UT5 × 5
20Gbps	75	UT4 × 3 or UT5 × 1-2
25Gbps	60	UT4 × 2 or UT5 × 1
32Gbps	46.875	UT5 × 1

-※This table does not consider
 -the number of available VTX backend input/output transceiver port
 -the bit number of ＋α information on backend (chipID etc.)

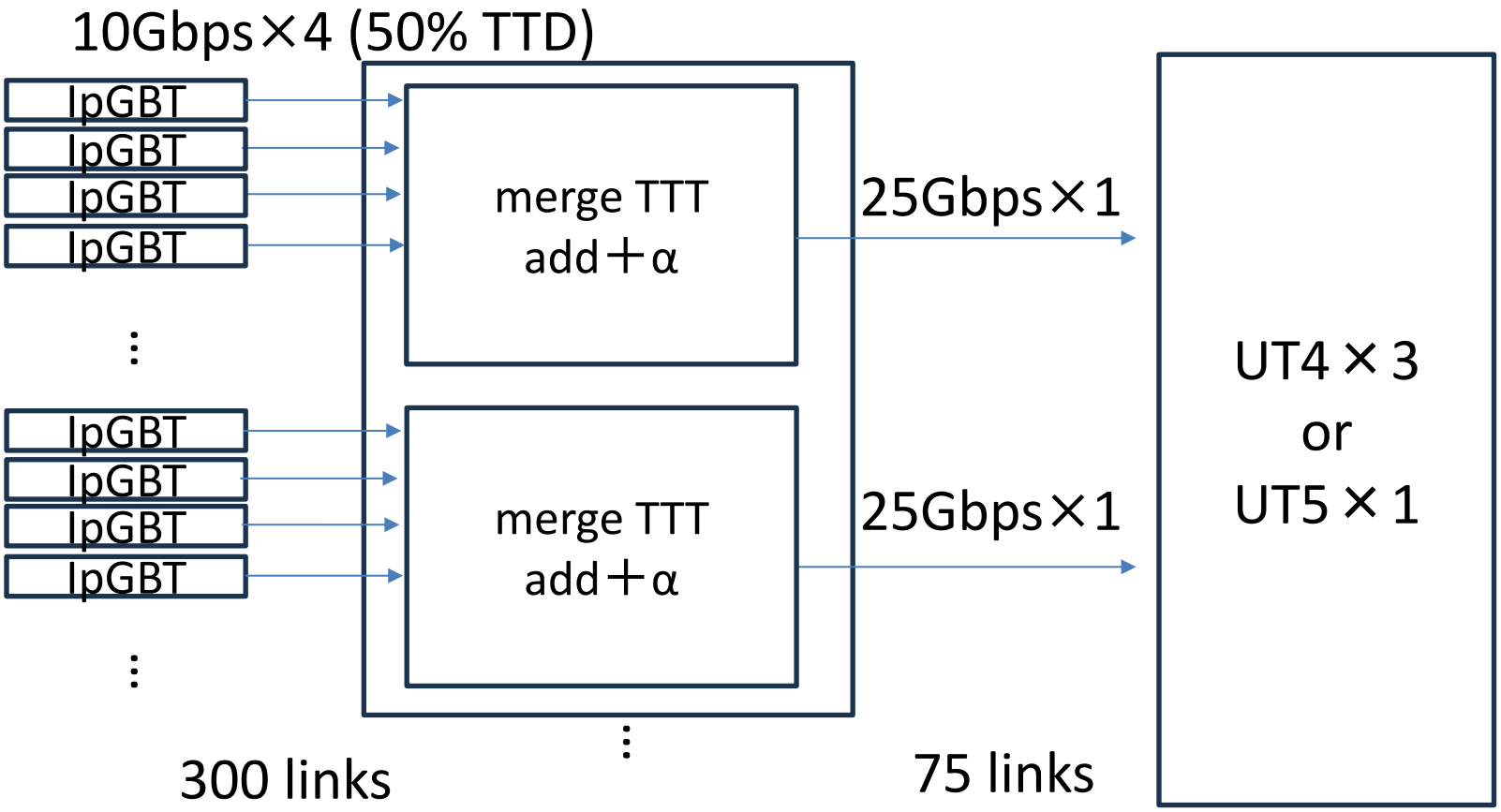
-higher transceiver speed is preferred for TRG
 -32Gbps per link ?　I want to know feedback from you.

Example of backend board input/output: 25Gpbs

-If we would like to use 32Gbps(or more) between VTX backend and TRG, data from different lpGBTs should be merged on backend

possible example configuration with 25Gbps

-merge TTT from four lpGBT into one

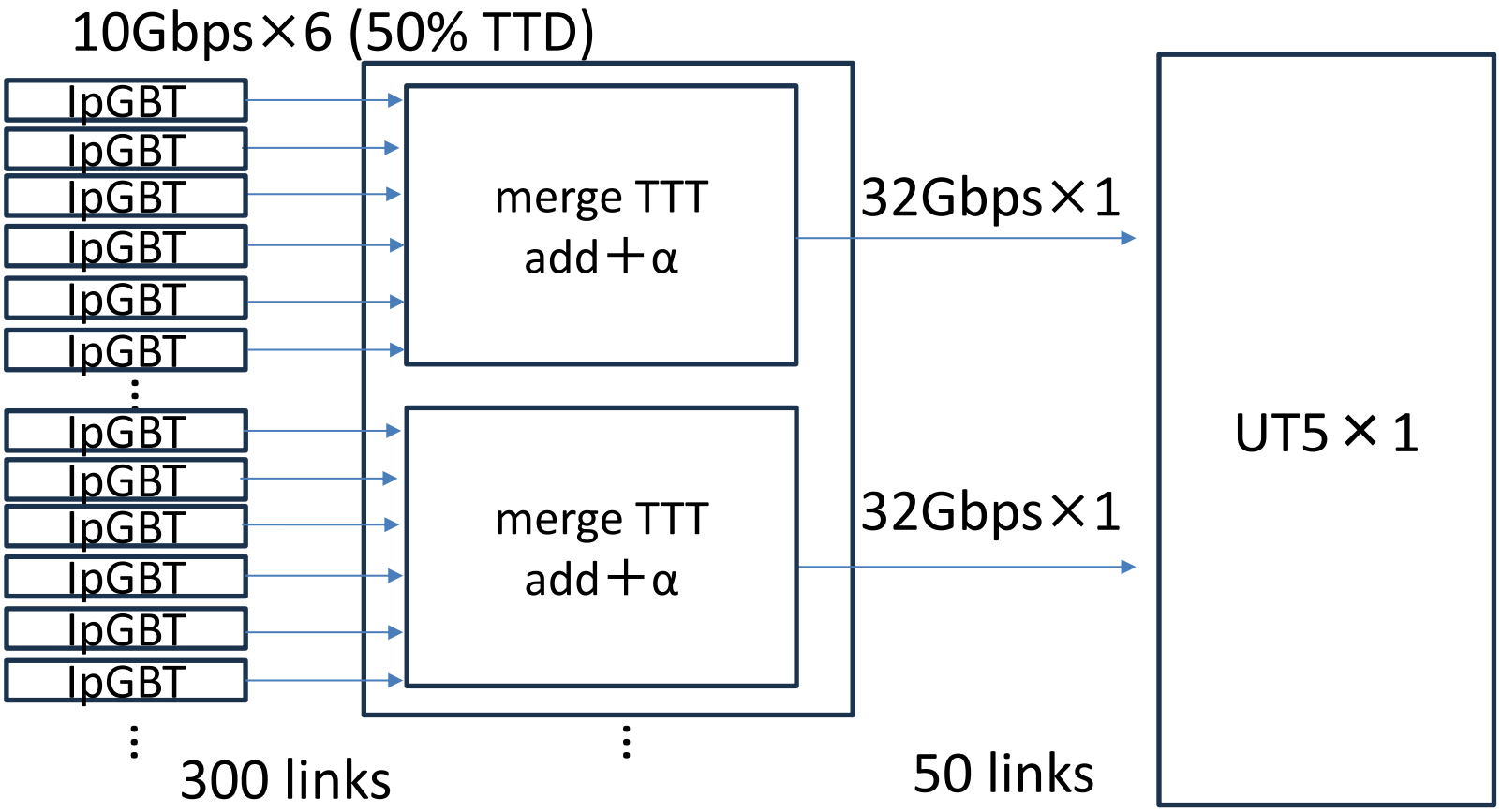


Example of backend board input/output: 32Gpbs

-If we would like to use 32Gbps(or more) between VTX backend and TRG, data from different IpGBTs should be merged on backend

possible example configuration with 32Gbps

-merge TTT from six IpGBT into one

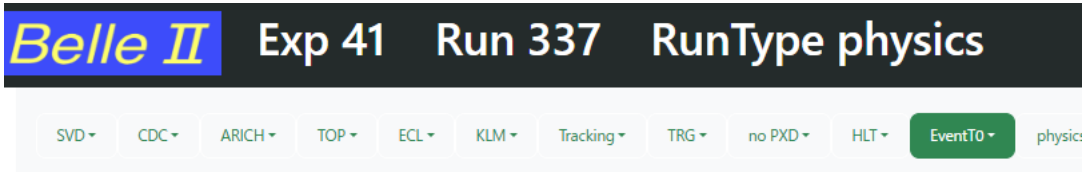


Requirements on event timing resolution

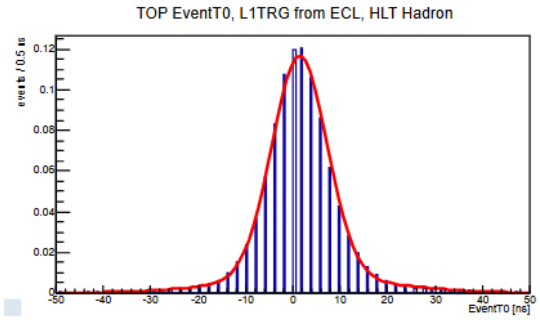
TRG event timing resolution

-Belle II TRG system will send trigger signal to VTX and other detector

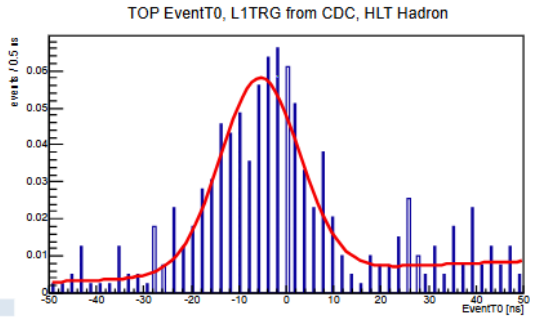
-The timing resolution(1σ) of trigger signal is a few--20ns, depending on event multiplicity and ECL energy deposit. Tail is spread to about ±~50ns at maximum.



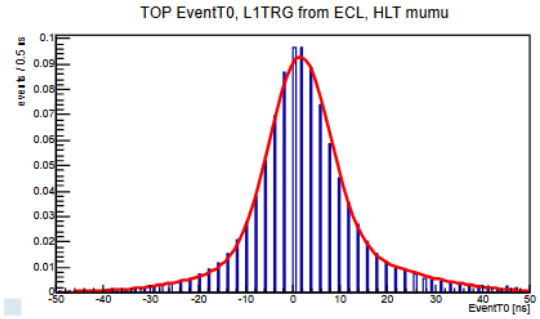
double gaussian fit on DQM



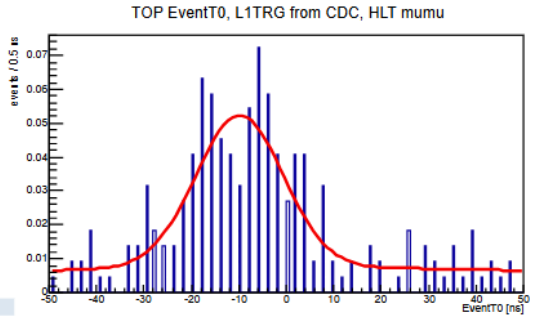
ECLTRG
hadron skim
σ1=~6ns
σ2=~20ns



CDCTRG
hadron skim
σ1=~8ns
σ2=~100ns



ECLTRG
mumu skim
σ1=~8ns
σ2=~20ns



CDCTRG
mumu skim
σ1=~9ns
σ2=~100ns

offline eventT0 – trigger timing (ns)

offline eventT0 – trigger timing (ns)

TRG event timing resolution

-Belle II TRG system will send trigger signal to VTX and other detector

-The timing resolution(1σ) of trigger signal is a few--20ns,
depending on event multiplicity and ECL energy deposit.
Tail is spread to about ±~50ns at maximum.

TRG does not plan to improve timing resolution at LS2.
Please assume the same or worse timing resolution than now.

Other question

-How much is the reference clock of transceiver on VTX backend board ?
(Is the clock driven by RF ?)

-How much is maximum latency of VTXDAQ ?
(L1 latency will be extended to 9μs or more at LS2)

-Do you have any update of Strixels segmentation size discussion since the last workshop ?

Summary

-Discuss TRG requirement to VTX

- optical bandwidth to send TTT data from VTX backend to TRG:

  -higher transceiver speed is preferred for TRG to reduce number of UT

  -32Gbps per link by merging TTT from several IpGBT data on backend ?
  I want to know feedback from you.

- L1 event timing resolution for VTXDAQ

  -The timing resolution(1σ) of trigger signal is a few--20ns,
  depending on event multiplicity and ECL energy deposit.
  Tail is spread to about ±~50ns at maximum.

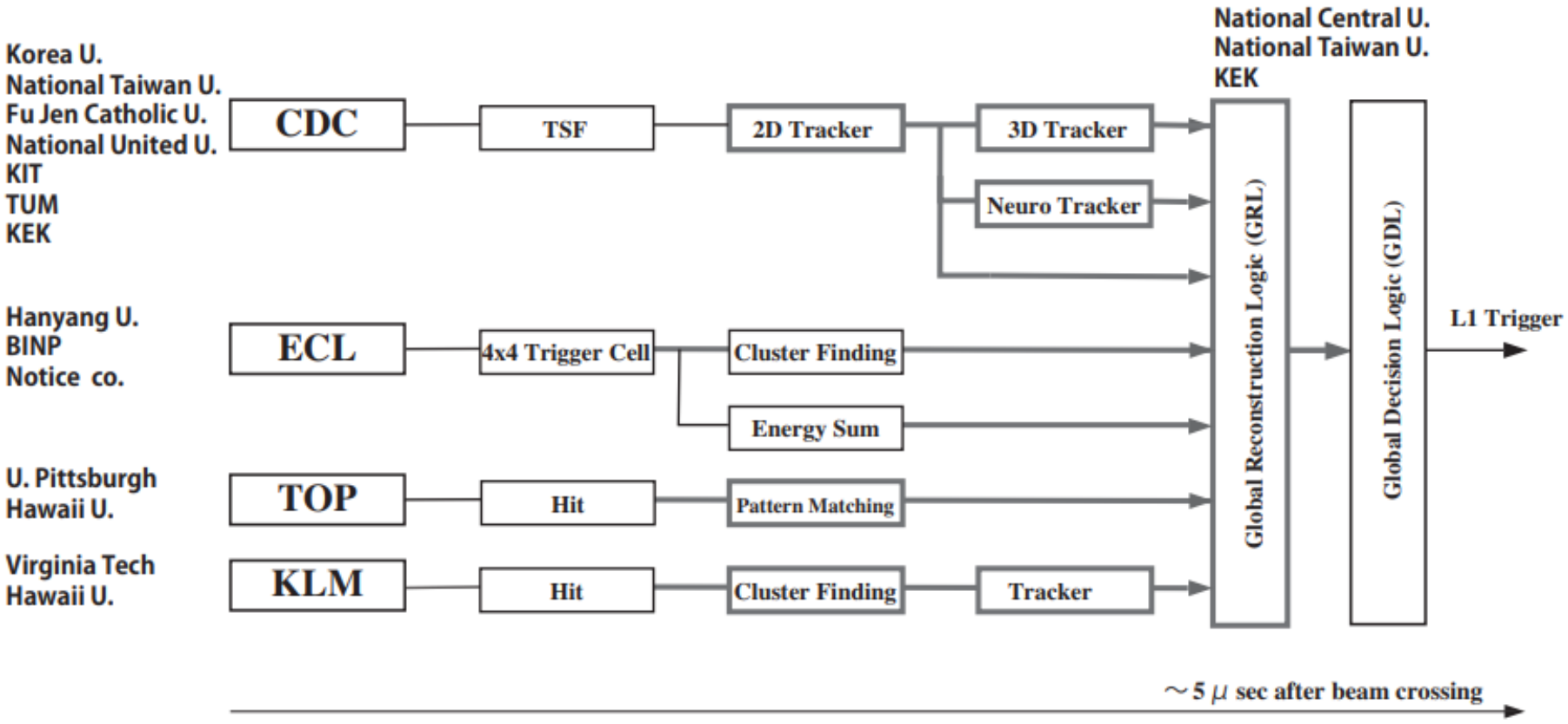
  -TRG does not plan to improve timing resolution at LS2.
  Please assume the same or worse timing resolution than now.

backup

Present TRG system

-So far, CDCTRG is a main system to trigger charged particles

-SVD/PXD does not have trigger functionality

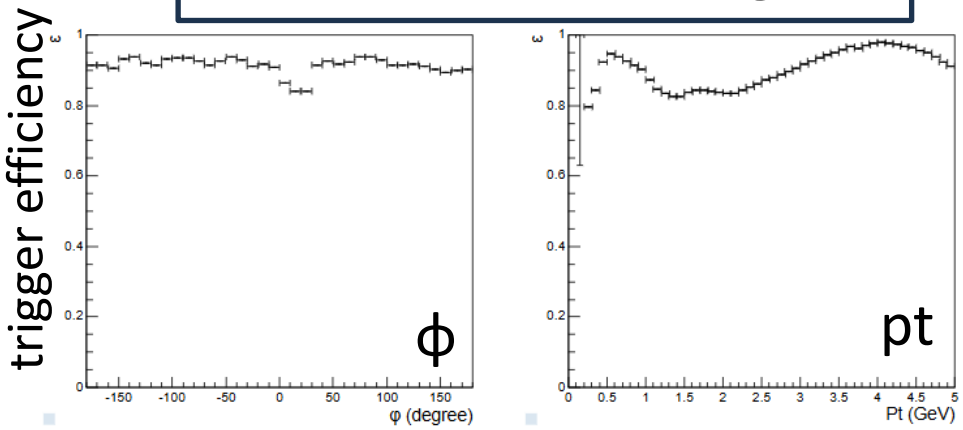


possible CDCTRG issue after LS2 (1)

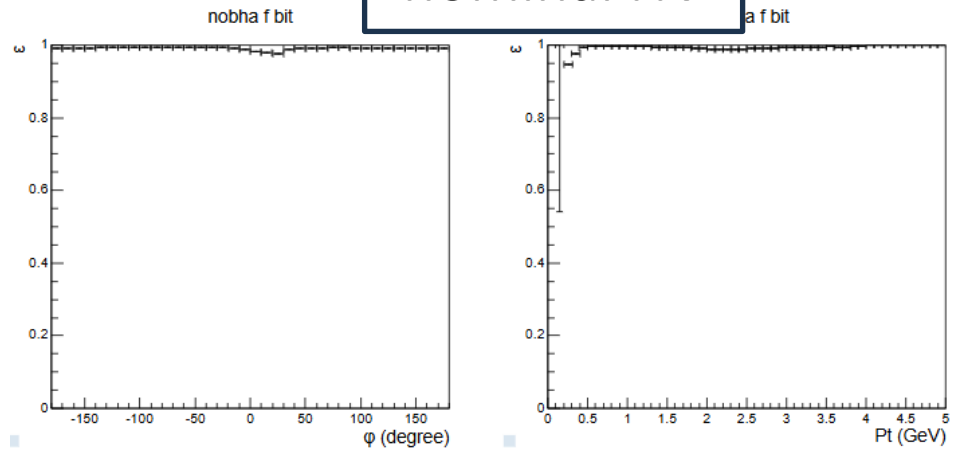
-Low trigger efficiency due to CDC detector issue/change

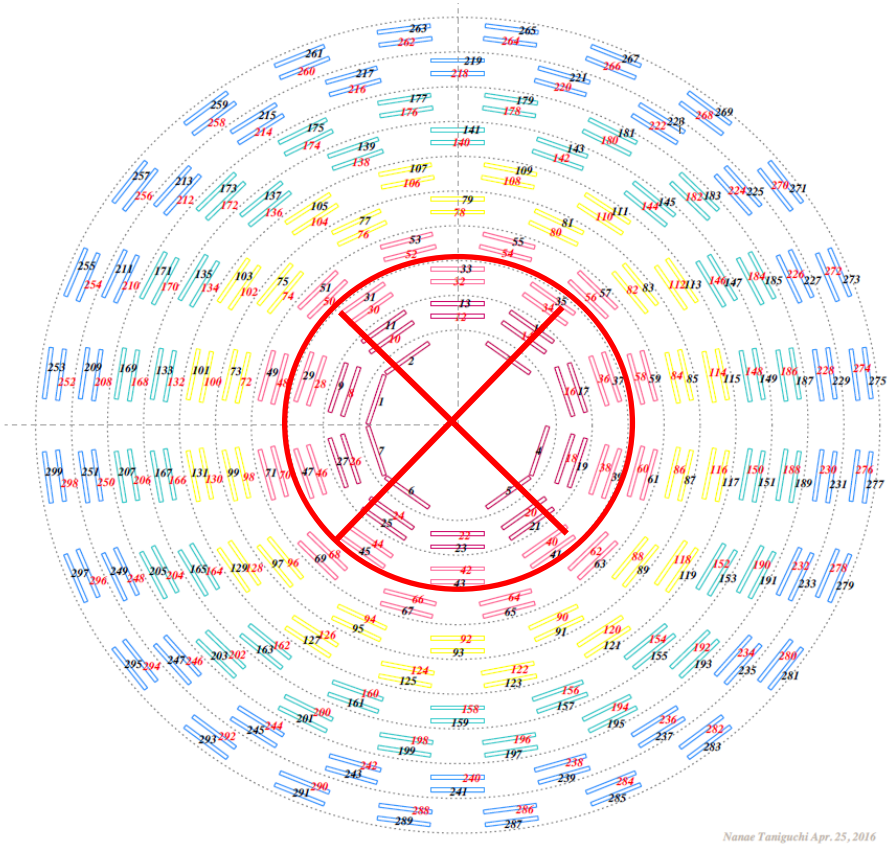
- -low hit efficiency by low gas gain and low HV
- -possible removal of inner layers

lowerHV (50% lower gain)



nominal HV





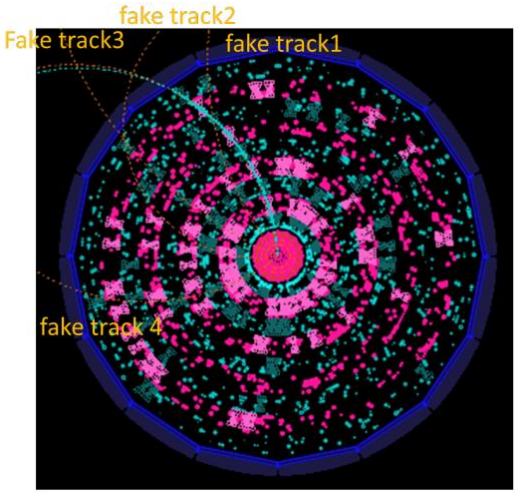
possible CDCTRG issue after LS2 (2)

-low-multi trigger rate may exceed 30kHz limitation due to beamBG

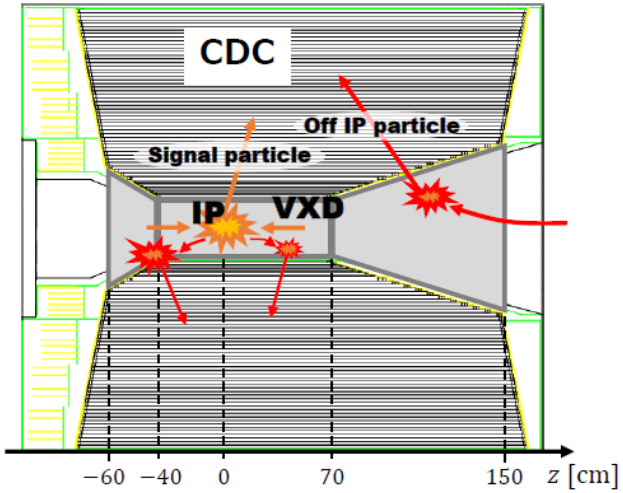
-fake track: high detector occupancy or cross talk: $\propto (\text{beamBG})^2$

-off-IP particle: real charged particle outside from IP $\propto$ beamBG

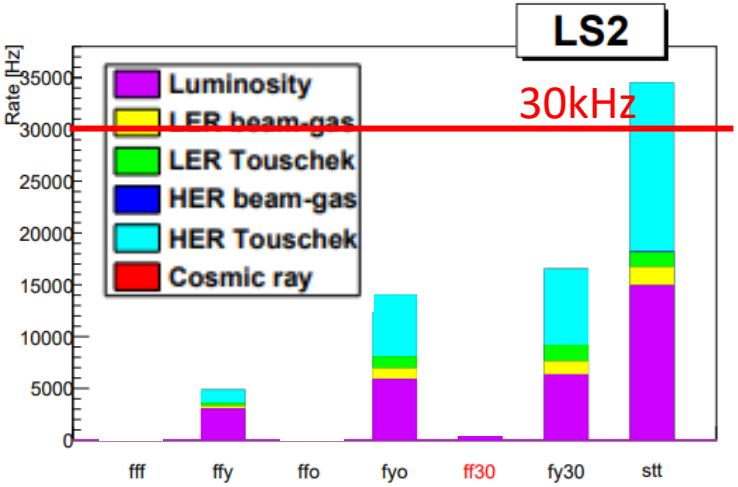
fake track



off-IP particle



Expected trigger rate after LS2



three tracks for BB

two tracks for BB

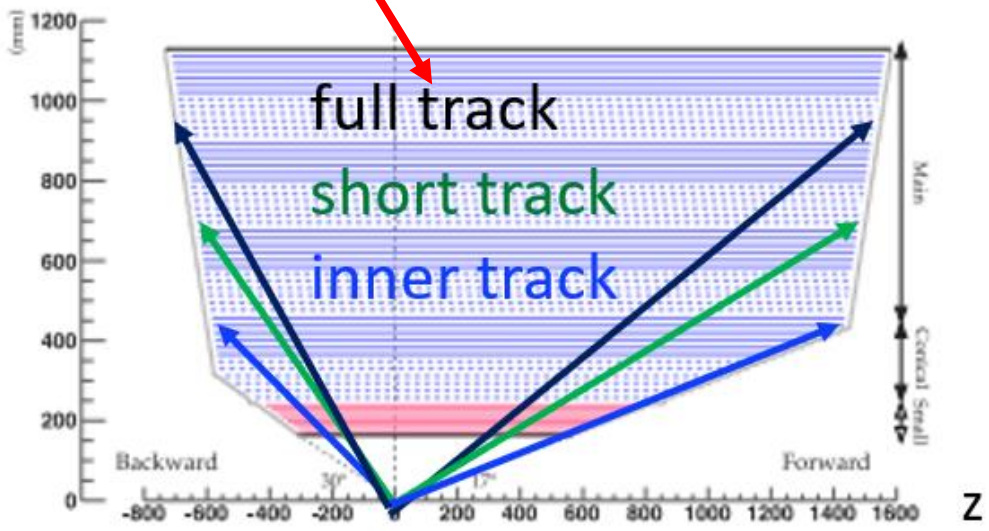
single track for lowmulti

possible CDCTRG issue after LS2 (3)

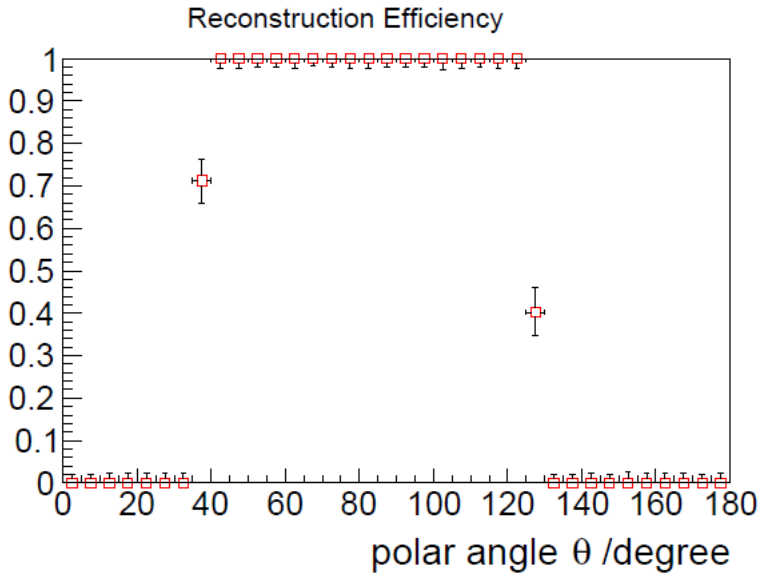
-limited angular acceptance for low-multi physics and PID calibration

-"full track"(f) at barrel is always required for trigger decision

-standalone "short track", "inner track" triggering is impossible due to high rate



efficiency of full track (MC)

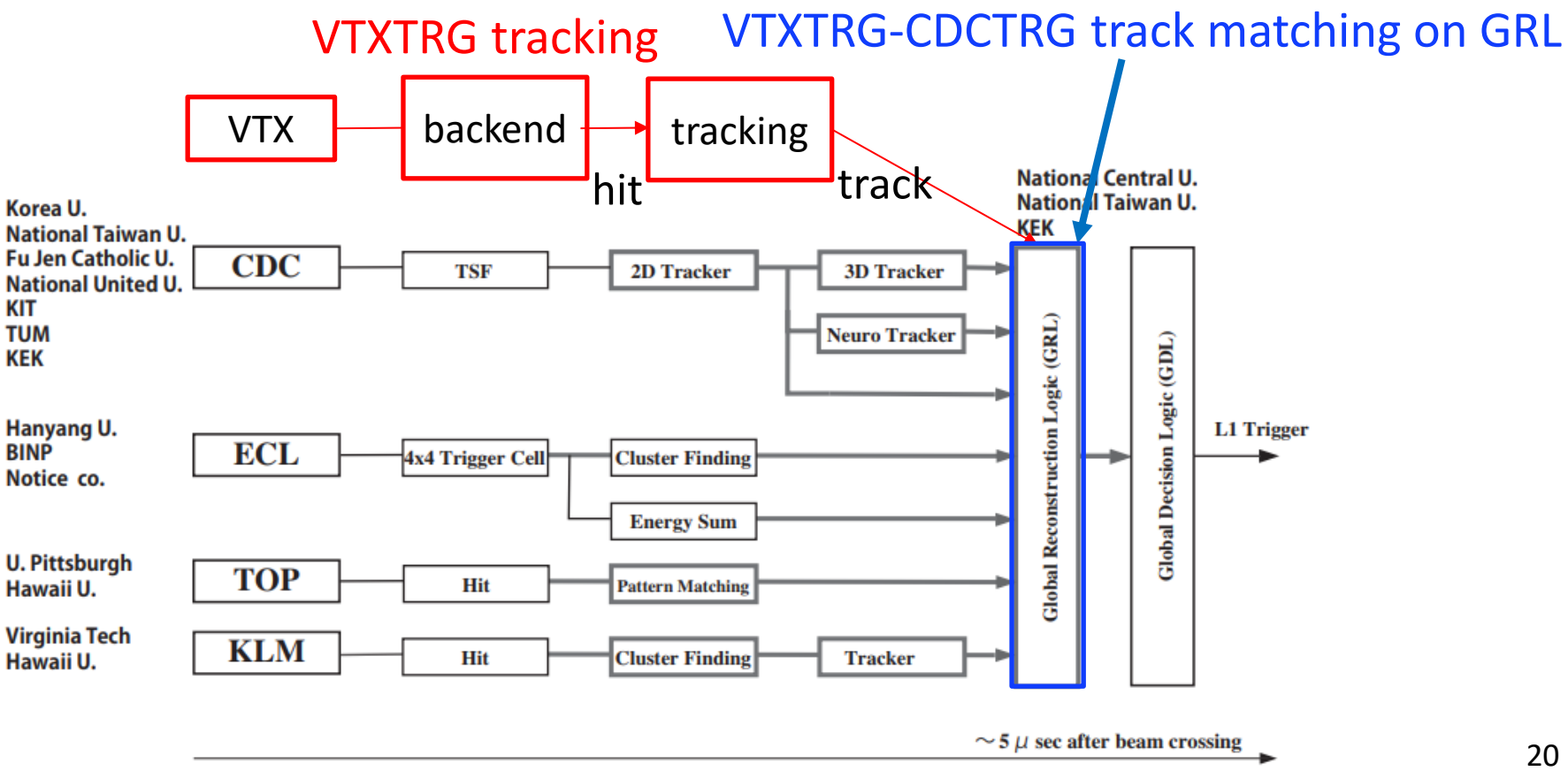


Motivation of VTXTRG

-By introducing VTXTRG and taking VTXTRG-CDCTRG matching, we solve:

- -CDCTRG low efficiency issue
- -CDCTRG high trigger rate issue
- -CDCTRG angular acceptance issue by using short/inner track

-VTXTRG standalone triggering might be possible too, but not must.



requirement for VTXTRG

-1. all hits should be sent from VTX to VTXTRG with pileline
(=no deadtime, fixed latency, independent from hit occupancy)

-2. VTXTRG efficiency is >~95% or more for single charged particle from IP

-3. fake track rate is < ~1000kHz(~10% per 100ns) for CDCTRG matching
(in the case of standalone VTXTRG, it is well less than 30kHz)

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-5. VTXTRG z resolution is better than a few cm to reject off-IP particles

-6. track trigger latency from VTX to GRL is 7~8μs
(assuming 9μs is required to entire TRG after LS2)

VTXTRG development status

-Jerome has kindly communicated with Koga time to time,
when he has VTXTRG related update

-Maximilian mainly consider the design of TTT and Strixel segment

-Matteo(IPHC) and Jerome designed VTXTRG tracking logic by simulation.
Performance is evaluated and summarized at 2025 Feb. B2GM (link).
(just software simulation, not firmware)

-Yiwei (Nankai U.) and Junhao, Koga are going to design VTXTRG-CDCTRG matching logic on GRL.
He finishes to implement Matteo's code to basf2 framework.

-(Sorry I think I am missing many contributers..)

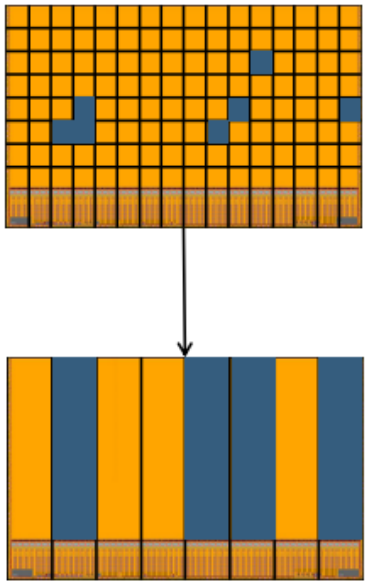
Assumed sensor segment for TTT

-We have assumed 8 x 1 Strixels per sensor for our VTXTRG simulation
-every 29.6ns, all hit information of Strixels will be send to TRG

VII. Strixel segmentation

- A major problem:
  - 896 x 464 pixels per sensor
  - ≈ 1,000,000,000 pixels in the detector
    - An excessive number of combinations

- Solution :
  - Strixel (Stx) : reduced spatial accuracy
  - 8 x 1 Strixels per sensor
    - ✓ Considerable reduction in the number of combinations
    - ✓ Reduction of the Pattern table size
  - Faster to search through a small table

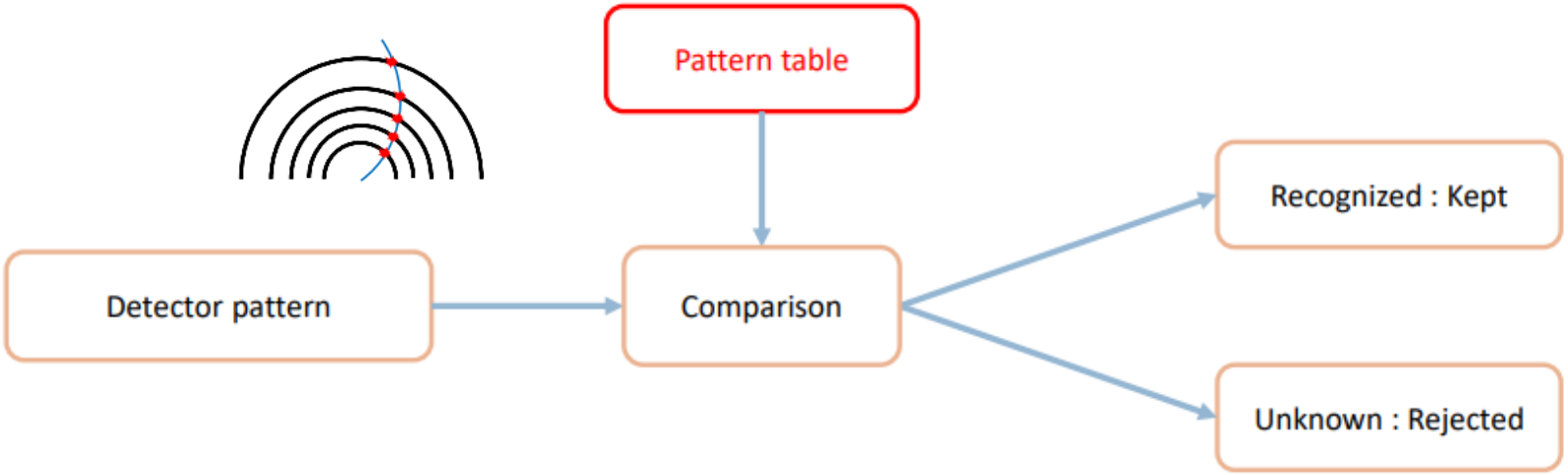


-Question: is this segmentation and #layer determined ?
how/when will you determine ?

VTXTRG tracking on simulation

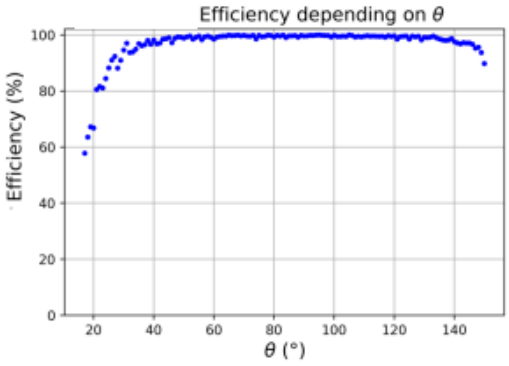
-VTXTRG tracking is simulated by look-up-table method by Matteo

- Look-Up Table (LUT) logic:
  1. Pattern table : Stored physical track patterns from simulation
  2. Detector/Table pattern comparison : Triggered track if recognized from the table

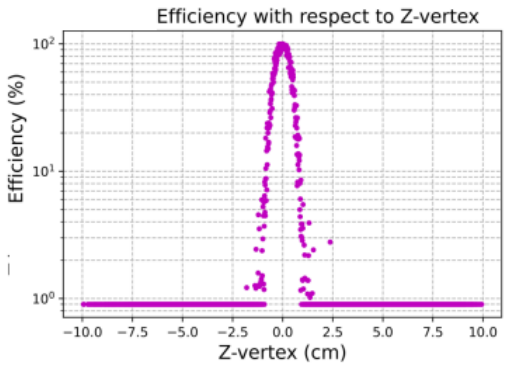


VTXTRG performance on simulation

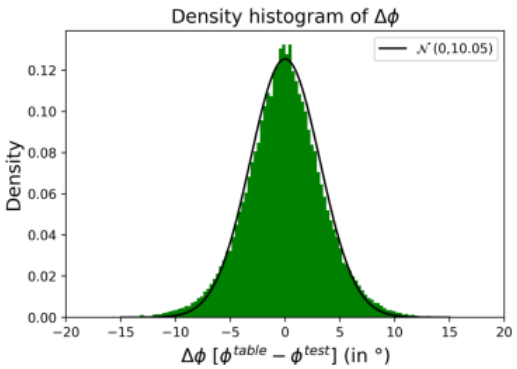
-Efficiency, z/ϕ resolution requirements are satisfied



Z-vertex Acceptance : |z| < 2.5 cm



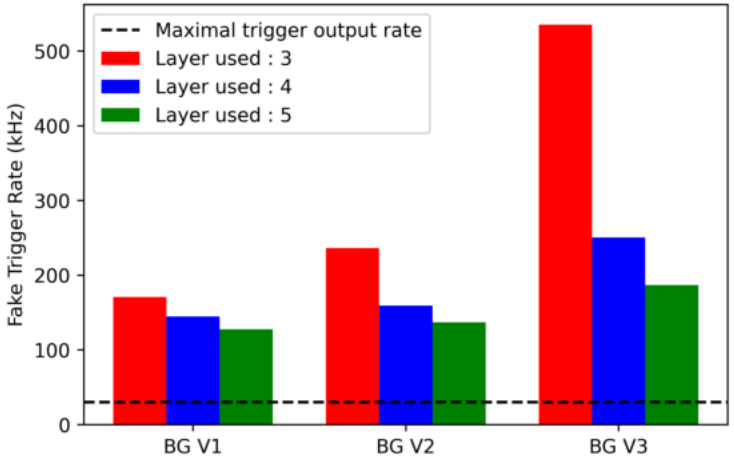
ϕ Accuracy : Gaussian σ = 3.17°



-Fake track rate is 100~500kHz with 3 layer, it is OK for CDCTRG matching

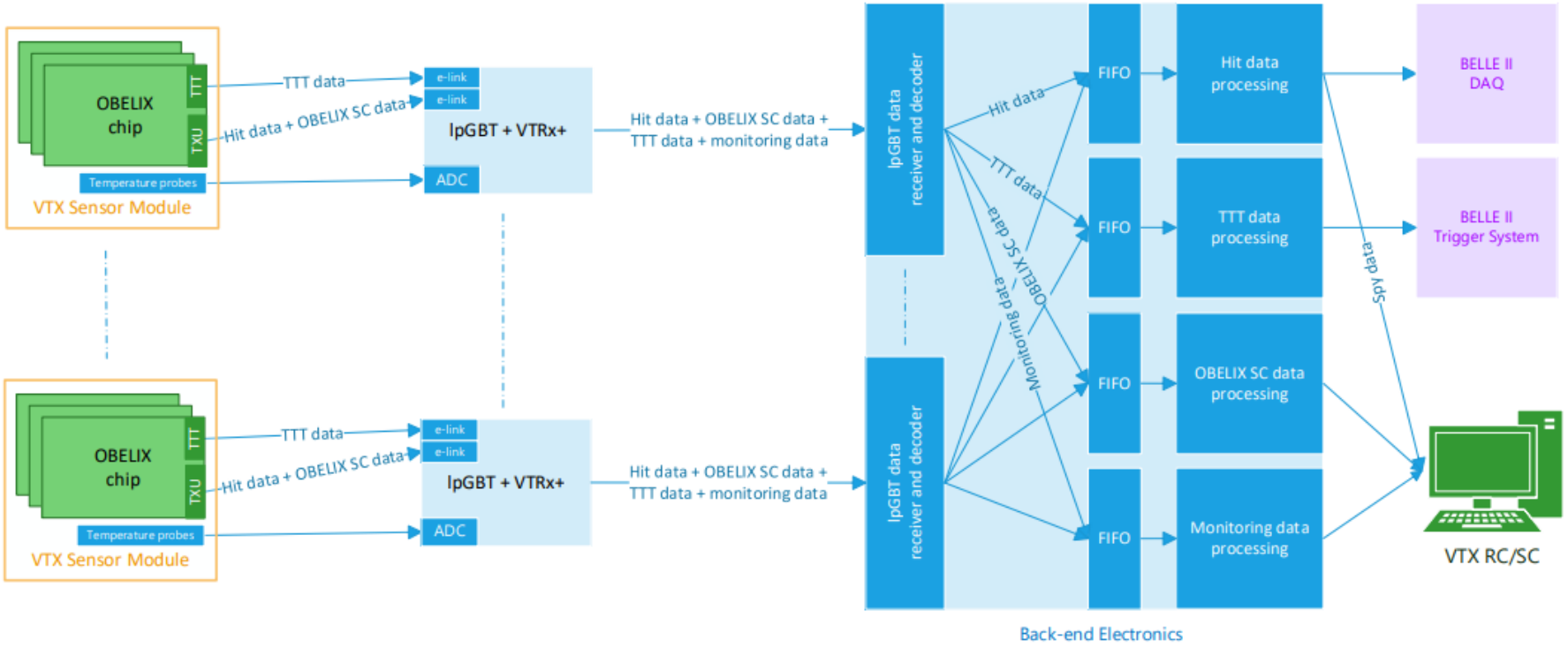
-standalone VTXTRG triggering is difficult

- Initial Fake Trigger Rate



VTX->VTXTRG->GRL dataflow

-Markus's Presentation at TRG-DAQ workshop



-I think you are considering to use a Back-end Electronics to prosessing TRG and DAQ data together on the board

backend electronics choice ?

-Markus's Presentation at TRG-DAQ workshop

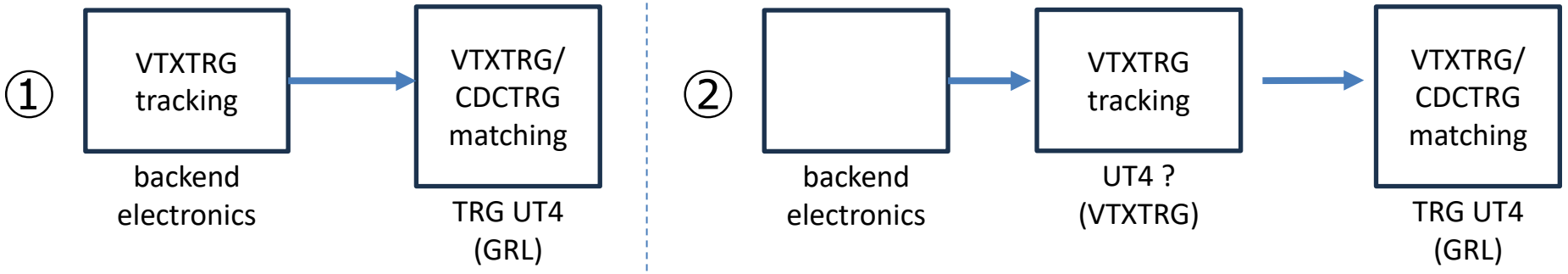
-Candidate of back-end electronics

- -PCIe40
- -PCIe400
- -CEPC TDAQ board
- -UT4 is one of candidate I think

Question: how/when will you determine ?

-Where trigger tracking logic can be implemented ?

- -①If you choose large FPGA (CEPC/UT4?), it can be implemented on the back-end electronics, probably. Better option in terms of cost.
- -②If you choose small FPGA, another trigger board (UT4?) is needed I guess



UT4

-Let me introduce UT4 as one of candidate

-FPGA: Virtex Ultrascale XCVU080/160
 -975-2350k logic cell

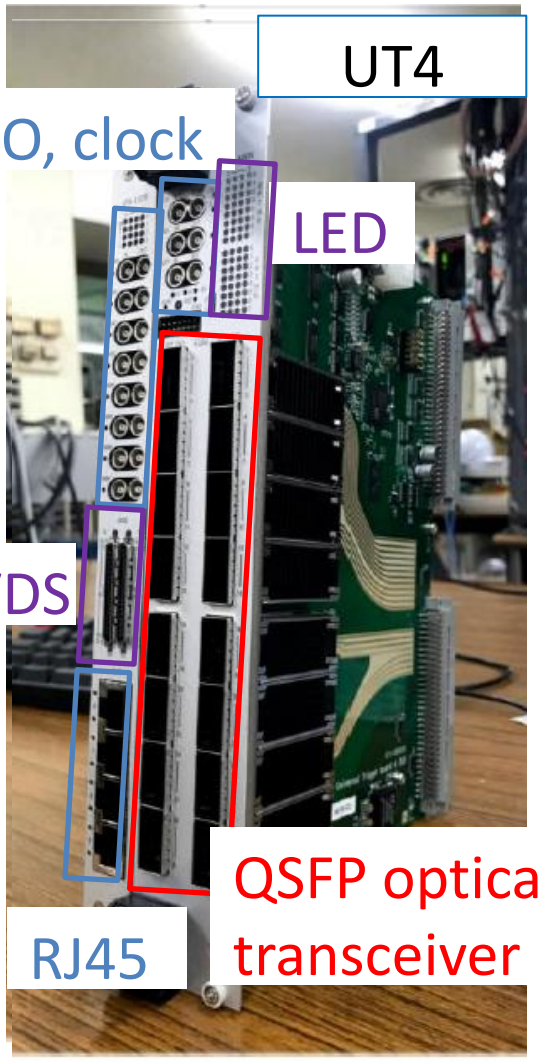
-QSFP optical transceiver/receiver
 -GTY(25Gbps)×32 lanes
 -GTH(16Gbps)×32 lanes

-VME 6U

-I/O of RJ45, LVDS(64ch), LEMO, clock

-Detail is in backup or contact me

-Price: 3~5,000,000 JPY per a board
(※KEK does not have funding to purchase additional UT4..)



responsible institute

-So far, only Jerome(IPHC) and Koga(KEK) are main staff for VTXTRG R&D

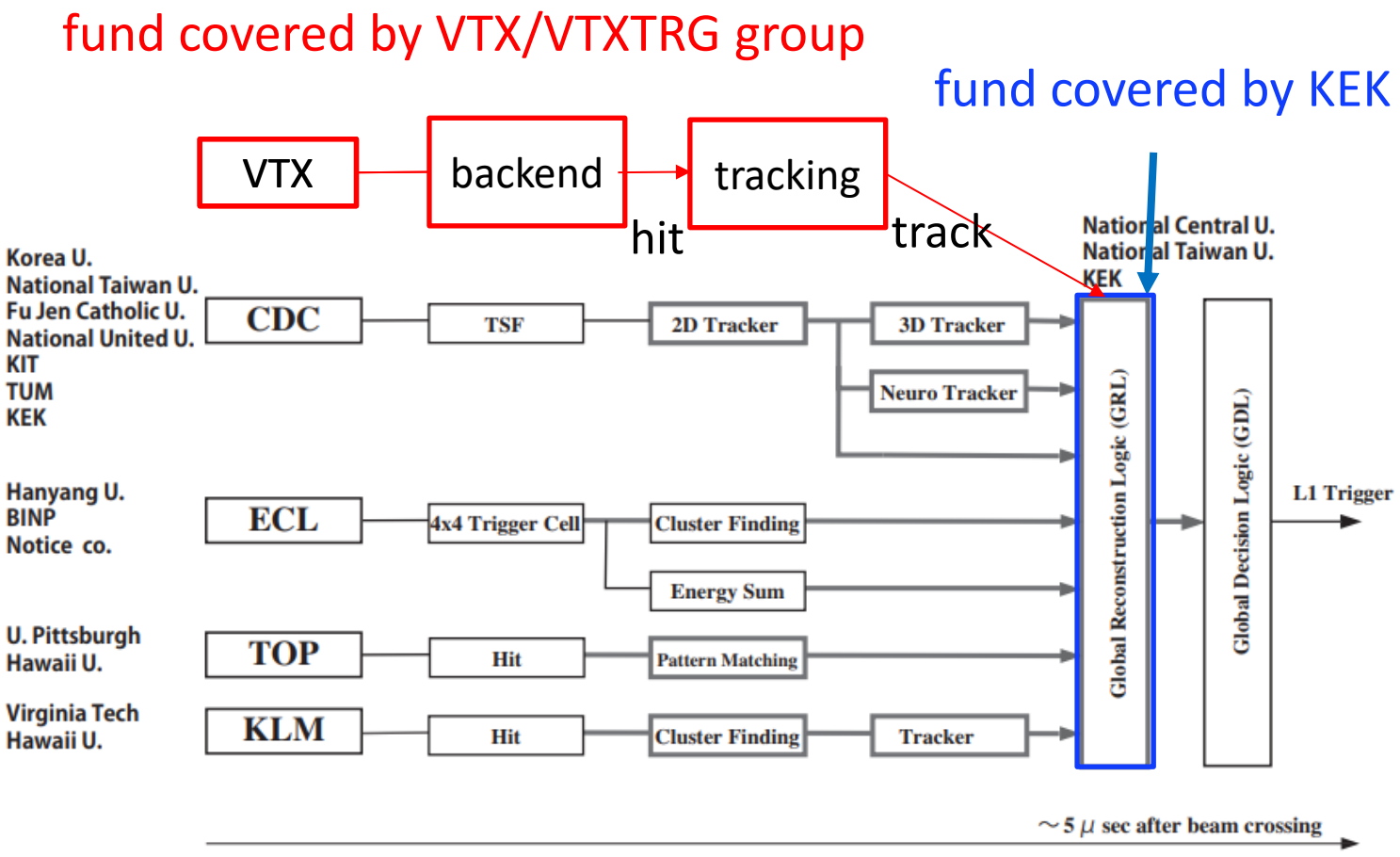
-Backend is responsible by OAW ? (or other VTX institute?)
-VTXTRG is responsible by IPHC ?
-VTXTRG-CDCTRG matching on GRL is responsible by KEK (or Nankai U.)

-link

sub-trigger / category	stage / sub-category	Coordinator, liaison	FW developer	SW (TSIM etc.) developer
TRG leader		leader: @Taichiro Koga (KEK) deputy: @Hideyuki Nakazawa (NTU)	--	--
GDL		@Hideyuki Nakazawa (NTU)	@Hideyuki Nakazawa (NTU)	@Hideyuki Nakazawa (NTU)
GRL	Matching	@Taichiro Koga (KEK)	@Taichiro Koga (KEK) @Hanwook Bae (KEK)	@Taichiro Koga (KEK), @Junhao Yin (Nankai U.),
	Neural net		@Deven Misra (U.Tokyo)	@Junhao Yin (Nankai U.), @Yubo Li (Xi'an Jiaotong U.)
CDC	Merger	@Jing-Ge Shiu (NTU)	@Taichiro Koga (KEK), @Yun-Tsung Lai (KEK)	--
	TSF	@Taichiro Koga (KEK)	@Taichiro Koga (KEK) @Hanwook Bae (KEK)	@Taichiro Koga (KEK)
	2D		@Taichiro Koga (KEK)	@Taichiro Koga (KEK)
	3D		@Zepeng Xu (U.Tokyo)	(KEK)
	ETF		@Taichiro Koga (KEK)	@Taichiro Koga (KEK)
	Neuro-3D	@Torben Ferber (KIT), Christian Kiesling (MPI)	@Kai Lukas Unger (KIT) @Yuxin Liu (SOKENDAI) --> Yang Yi (Fuan)	@Yuxin Liu (SOKENDAI) --> Yang Yi (Fudan)
	3D Hough		@Kai Lukas Unger (KIT)	empty
	Displaced vertex		empty	empty
	GNN R&D		Marc Neu (KIT)	@Lea Reuter (KIT)
ECL	FAM	@Unno Yuji (Hanyang.U)	@Unno Yuji (Hanyang.U)	@Unno Yuji (Hanyang.U)
	TMM		@Unno Yuji (Hanyang.U)	@Unno Yuji (Hanyang.U)
	ETM		@Unno Yuji (Hanyang.U)	@Unno Yuji (Hanyang.U)
	Calibration		--	@Eunji Jang (GNU)
	GNN-ETM		Marc Neu (KIT)	@Isabel Haide (KIT)
	BG study, ShaperDSP Upgrade		empty	empty
TOP		@Vladimir Savinov (Pittsburgh U.)	@Vladimir Savinov (Pittsburgh U.) @Kimika Arai (Pittsburgh U.)	@Vladimir Savinov (Pittsburgh U.)
KLM	Tracking	@Richard Peschke (Hawai U.)	@Richard Peschke (Hawai U.)	@Richard Peschke (Hawai U.)
	NN R&D		@Anthony Craig Little (Sydney U.)	@Anthony Craig Little (Sydney U.)
VTX (R&D for upgrade)		@Jerome Baudot (IPHC)	@Matteo Maushart (IPHC), @Maximilian Babeluk (HEPHY, trigger out electronics)	@Matteo Maushart (IPHC),

funding

-So far, subtrigger institutes have responsibility of budget for their own subtrigger system



Summary

-Motivation and requirement for VTXTRG

-improve charged particle's trigger efficiency/rate/acceptance

-requirements in page7

-Development status

-First VTXTRG tracking simulation is performed by Matteo(IPHC), Jerome. performance looks enough to satisfy requirements.

-VTXTRG-CDCTRG matching simulation is on-going by Yiwei(Nankai U.), Junhao, Koga (GRL group).

-Questions:

-Are segmentation of Strixels and #layer for TRG determined ? How/when will you determine ?

-How/when will you determine back-end electronics board ? Could we discuss dataflow design of VTX->VTXTRG->GRL in detail ?

-Could we share information of TTT and VTXTRG related development status more closely ? (We can attend some VTX meeting, or you can attend TRG upgrade meeting)

backup

UT4 FPGA

-Vertex Ultrascale XCVU080,160,190

-common pin package

Virtex® UltraScale™ FPGAs

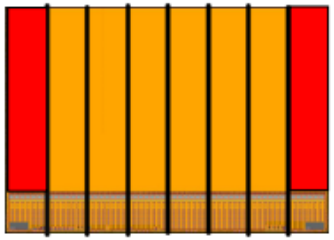
	Device Name	XCVU065	XCVU080	XCVU095	XCVU125	XCVU160	XCVU190	XCVU440
Logic Resources	System Logic Cells (K)	783	975	1,176	1,567	2,027	2,350	5,541
	CLB Flip-Flops	716,160	891,424	1,075,200	1,432,320	1,852,800	2,148,480	5,065,920
	CLB LUTs	358,080	445,712	537,600	716,160	926,400	1,074,240	2,532,960
Memory Resources	Maximum Distributed RAM (Kb)	4,830	3,980	4,800	9,660	12,690	14,490	28,710
	Block RAM/FIFO w/ECC (36Kb each)	1,260	1,421	1,728	2,520	3,276	3,780	2,520
	Block RAM/FIFO (18Kb each)	2,520	2,842	3,456	5,040	6,552	7,560	5,040
	Total Block RAM (Mb)	44.3	50.0	60.8	88.6	115.2	132.9	88.6
Clock Resources	CMT (1 MMCM, 2 PLLs)	10	16	16	20	28	30	30
	I/O DLL	40	64	64	80	120	120	120
	Transceiver Fractional PLL	5	8	8	10	13	15	0
I/O Resources	Maximum Single-Ended HP I/Os	468	780	780	780	650	650	1,404
	Maximum Differential HP I/O Pairs	216	360	360	360	300	300	648
	Maximum Single-Ended HR I/Os	52	52	52	52	52	52	52
	Maximum Differential HR I/O Pairs	24	24	24	24	24	24	24
Integrated IP Resources	DSP Slices	600	672	768	1,200	1,560	1,800	2,880
	System Monitor	1	1	1	2	3	3	3
	PCIe® Gen1/2/3	2	4	4	4	4	6	6
	Interlaken	3	6	6	6	8	9	0
	100G Ethernet	3	4	4	6	9	9	3
	GTH 16.3Gb/s Transceivers	20	32	32	40	52	60	48
	GTY 30.5Gb/s Transceivers	20	32	32	40	52	60	0
Speed Grades	Commercial	–	–	–	–	–	–	-1
	Extended	-1H -2 -3	-1H -2 -3	-1H -2 -3	-1H -2 -3	-1H -2 -3	-1H -2 -3	-2 -3
	Industrial	-1 -2	-1 -2	-1 -2	-1 -2	-1 -2	-1 -2	-1 -2

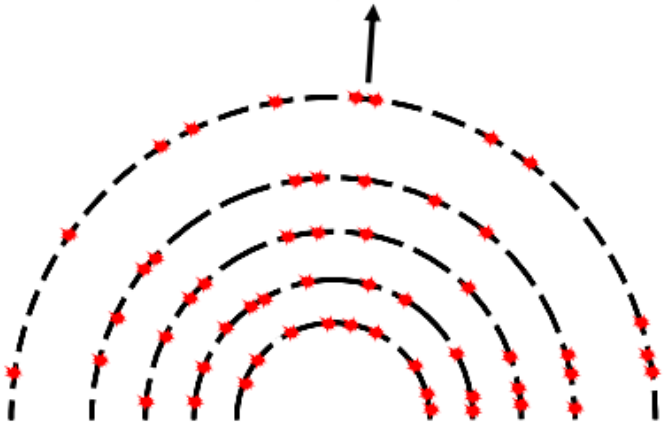
	Package Footprint[1, 2, 3]	Package Dimensions (mm)			HR I/O, HP I/O, GTH 16.3Gb/s, GTY 30.5Gb/s			
Footprint Compatible with Kintex® UltraScale Devices	C1517	40x40	52, 468, 20, 20	52, 468, 20, 20	52, 468, 20, 20			
	D1517	40x40		52, 286, 32, 32	52, 286, 32, 32	52, 286, 40, 32		
	B1760	42.5x42.5		52, 650, 32, 16	52, 650, 32, 16	52, 650, 36, 16		
	A2104	47.5x47.5		52, 780, 28, 24	52, 780, 28, 24	52, 780, 28, 24		
	B2104	47.5x47.5		52, 650, 32, 32	52, 650, 32, 32	52, 650, 40, 36	52, 650, 40, 36	52, 650, 40, 36
	C2104	47.5x47.5			52, 364, 32, 32	52, 364, 40, 40	52, 364, 52, 52	52, 364, 52, 52
	B2377	50x50						52, 1248, 36, 0
	A2577	52.5x52.5					0, 448, 60, 60	
	A2892	55x55						52, 1404, 48, 0

Notes:
1. Packages with the same package footprint designator, e.g., A2104, are footprint compatible with all other UltraScale devices with the same sequence. See the migration table for details on inter-family migration.
2. For full part number details, see the Ordering Information section in DS890, *UltraScale Architecture and Product Overview*.
3. See UG575, *Kintex UltraScale and Virtex UltraScale FPGAs Packaging and Pinouts User Guide* for more information.

X. VTX TRG : Recap

OBELIX n°2435





OBELIX n°2435 TTT Output

10000001

Event Bitword

0001000111001000 10….00010100

LUT Comparison

Pattern Table :

Index	Pattern	Θ (°)	Φ (°)	p_T (GeV)
1	001…010….0001	67	259	1.56
2	010…010….0001	125	23	0.89
…	……..	…	…	…
126304	100…010….0100	43	344	2.34
126305	100…010…0010	175	88	1.71