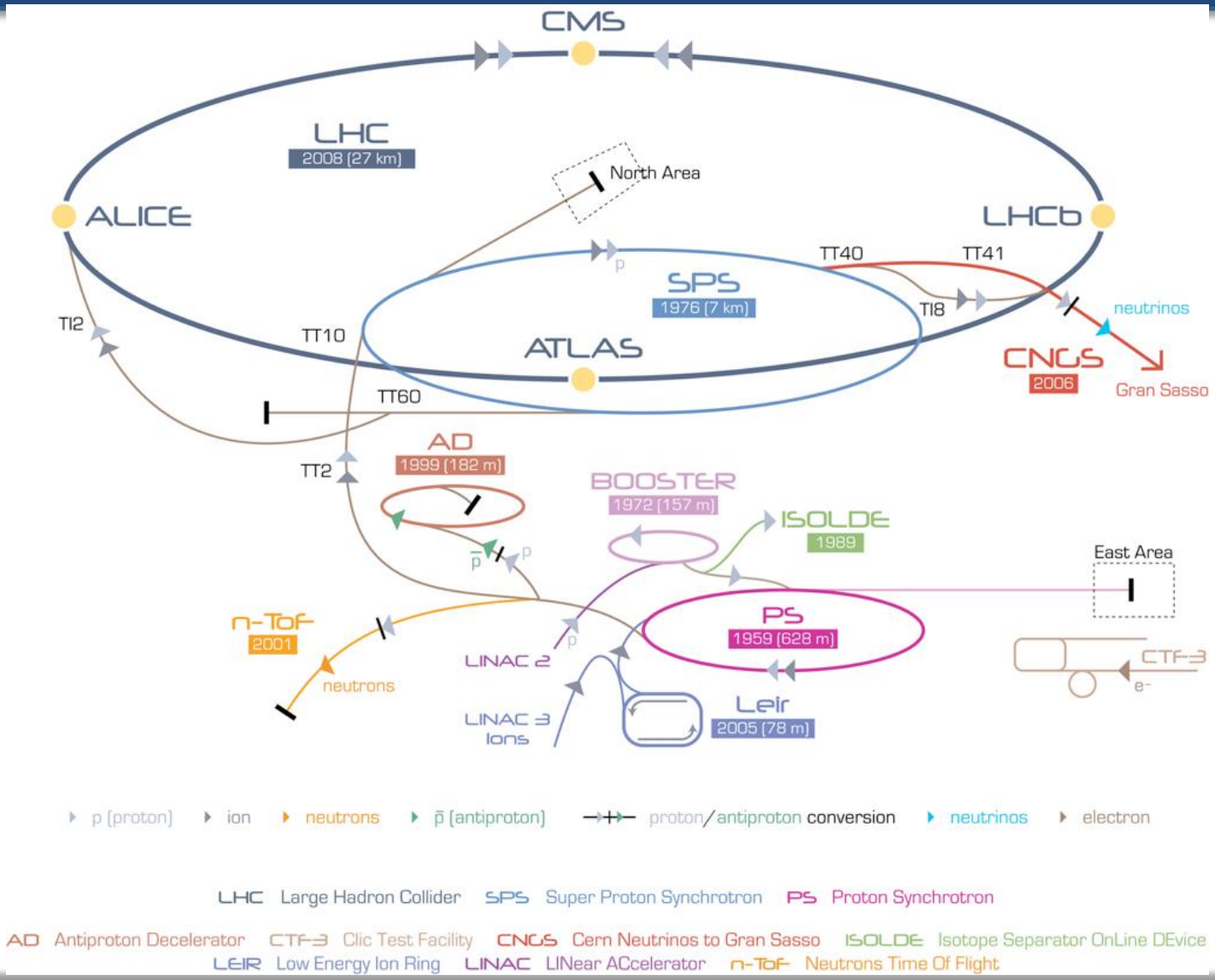
29th May 2020

CERN BEAM LOSS MONITORING SYSTEM FOR LHC INJECTORS COMPLEX

William Viganò (william.vigano@cern.ch)

The CERN Accelerator Complex



Outline

- System architecture
- Front-Ends
- Installations

SYSTEM ARCHITECTURE

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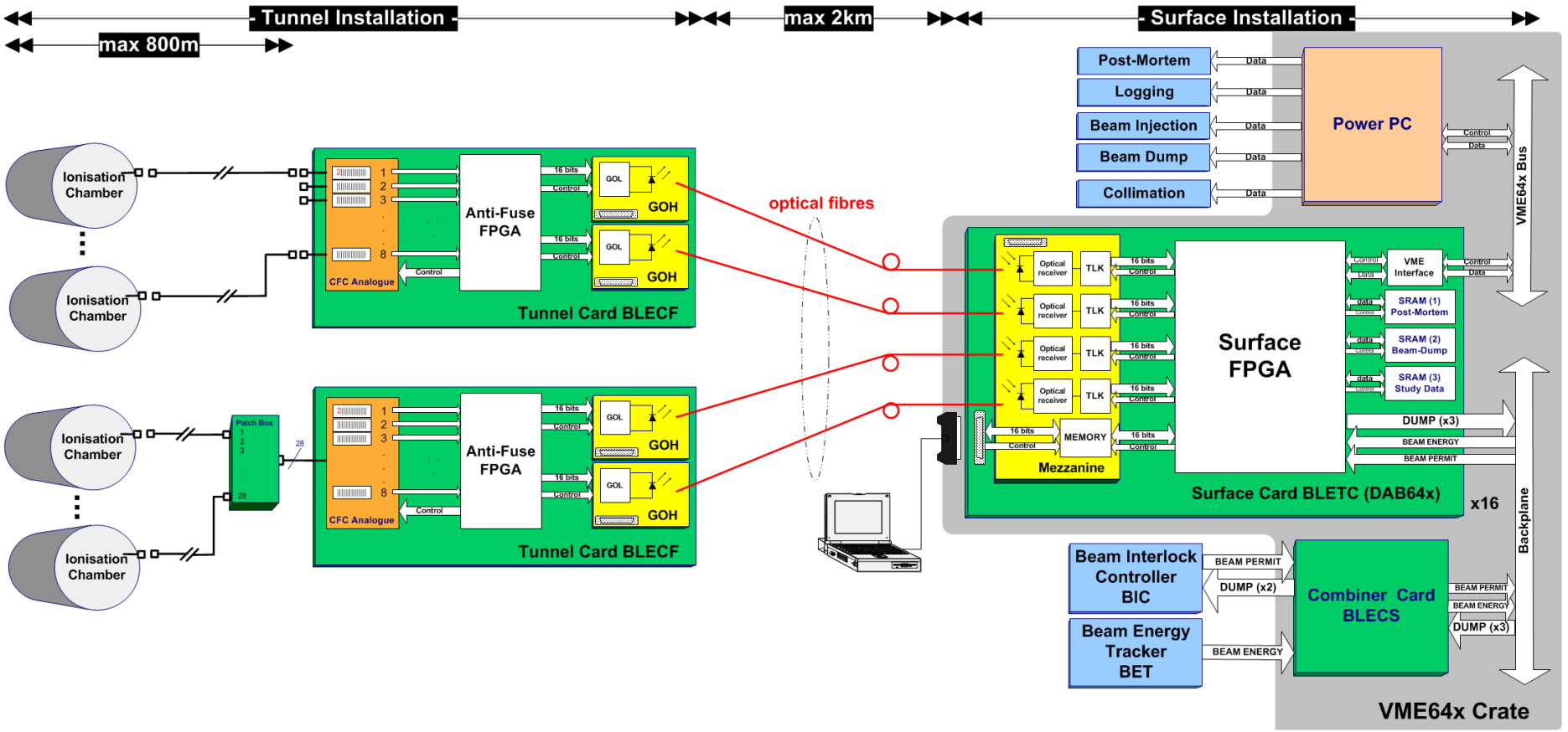
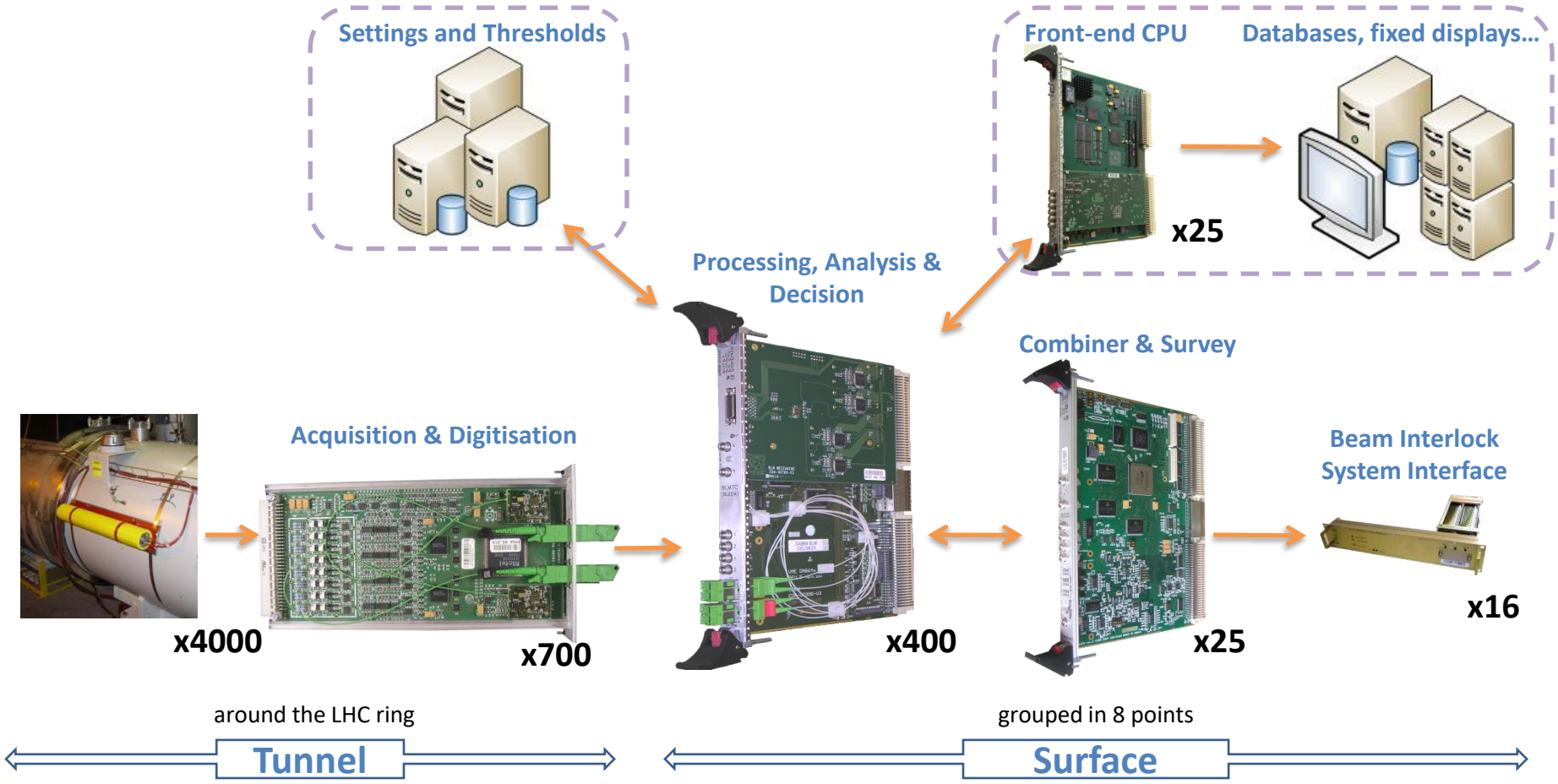
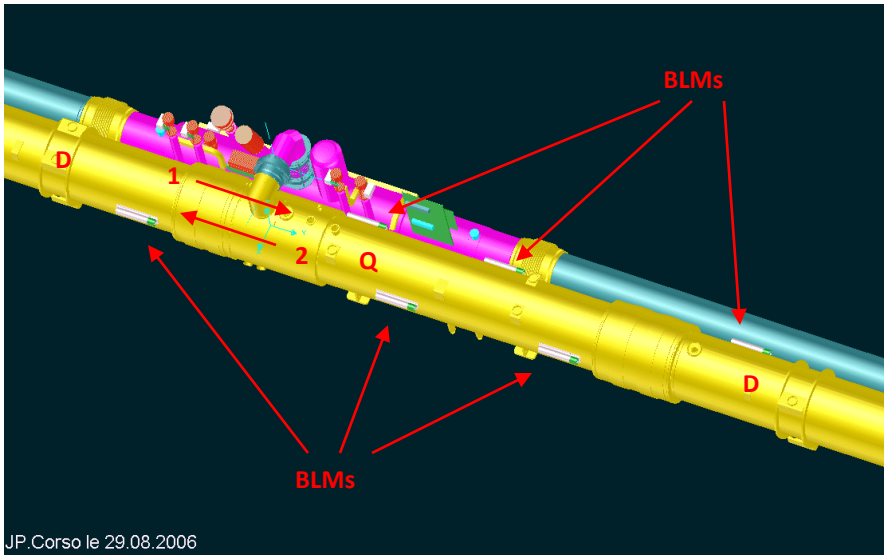
LHC System Overview



LHC System Overview

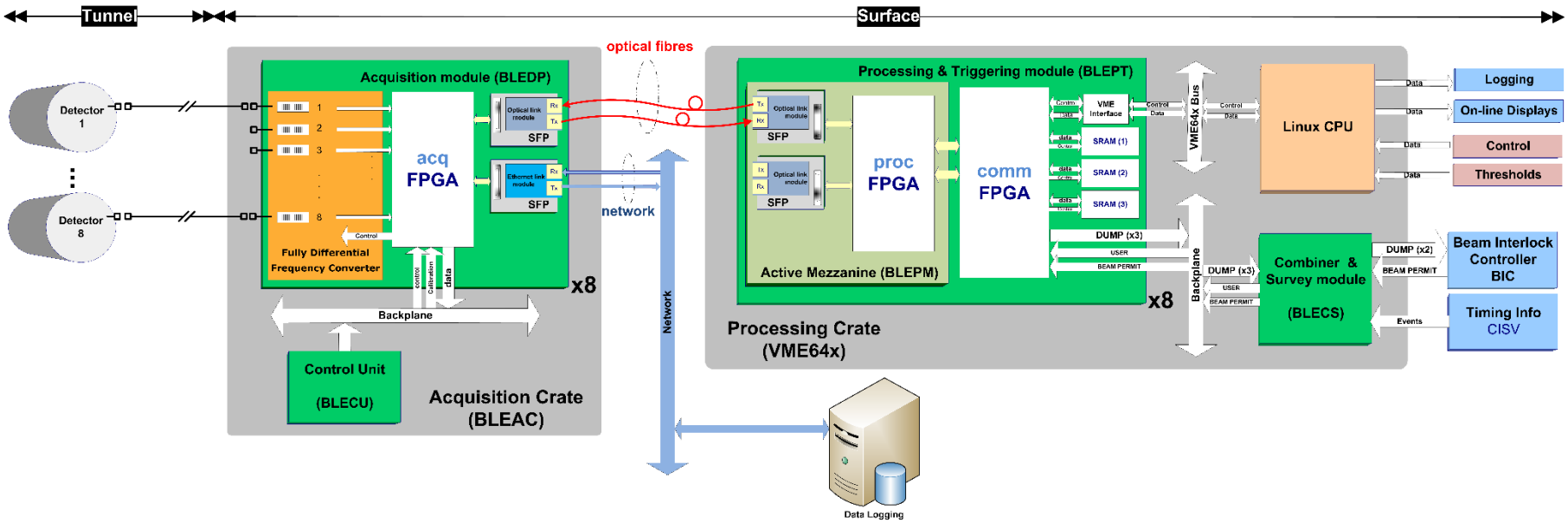


General Information



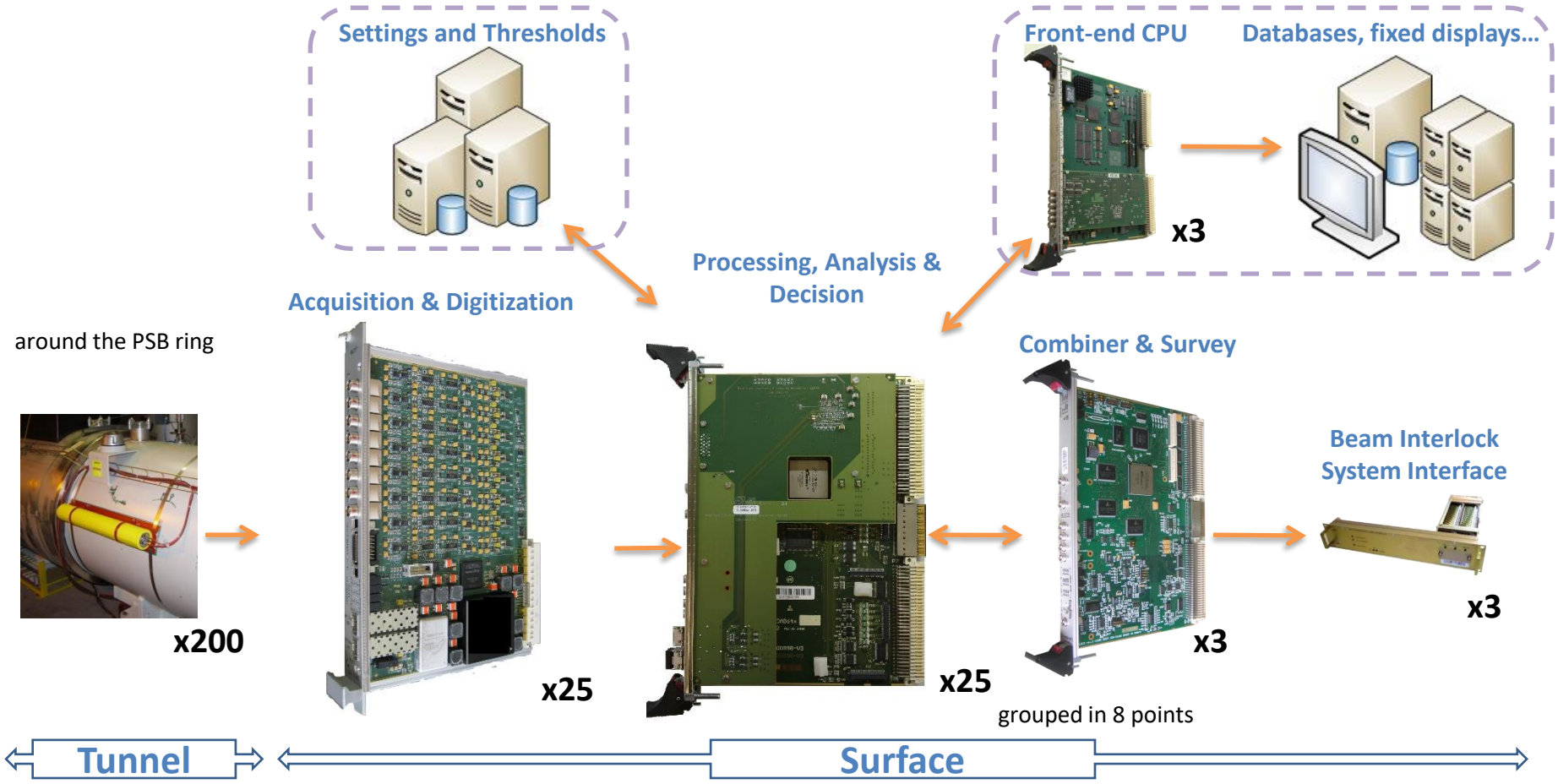
- ~ 4000 Sensors.
- ~ 3600 Ionization chambers.
- ~ 400 Secondary emission monitors.
- ~ 700 BLM data acquisition cards installed.
- In the LHC arc cards are installed underneath the magnets in a 19'' create.
- In the LHC straight section cards are installed in the nearby side-tunnels, because of higher radiation.
- Up to 3 x 19“ crates with 10 DACs are installed in the straight section.
- Signal cable with length up to 600m.

Injector Complex System Overview



Injector Complex System Overview

Example application At Proton Synchrotron Booster



FRONT-ENDS

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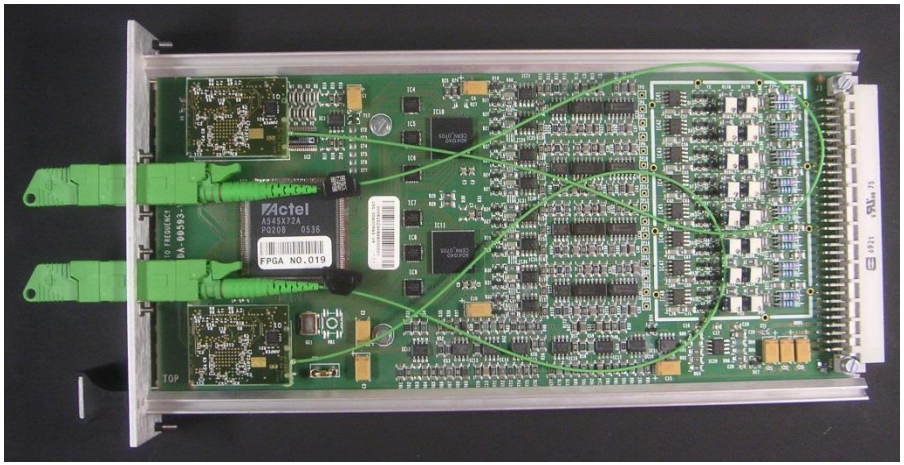
LHC Front End

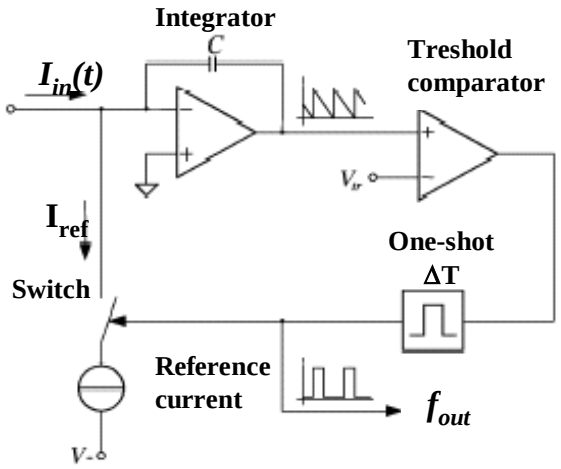


- LHC Front end functions:
  - 8 current inputs (CFC)
  - FPGA for data combiner
  - Two redundant GOH from CMS as optical link
  - High Voltage feedback input

LHC Front End

- LHC Front end specification:
  - Radiation tolerant up to 500Gy (20 LHC lifetime).
  - Reliability level SIL3 to prevent false dump.
  - Current measuring range 2.5pA to 1mA.
  - Integration time window 40us.
  - Input current protection ~ 10A @100us.
  - Input voltage protection ~ 1500V @100us.
  - Redundant optical data transfer to surface.
  - Test features for system check.
  - Survey of the card voltage supplies.
  - Survey of detector high voltage supply.

LHC Front End



Input Current	Output frequency
1mA	5MHz
1uA	5kHz
1nA	5Hz
1pA	5mHz

- Essentials of the input circuit:
  - Current to frequency converter (CFC).
  - Balanced charge integrator.

LHC Front End

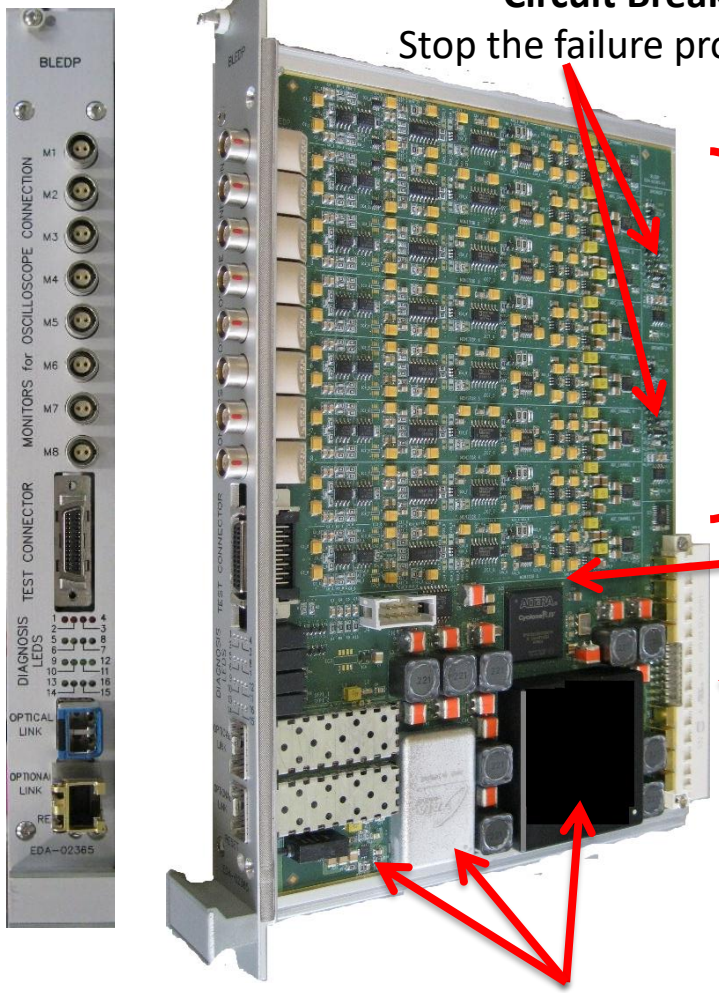
- Constant 10pA offset current
  - Check on channel availability.
  - In case of exceeding limits, a beam dump can be generated.
- Continuous status monitoring
  - Monitoring of voltage supplies and other status information.
  - Should failure occur, a beam dump can be generated.
- Continuous check while data transmission
  - Card identity number check.
  - Frame identity number check.
  - Cycle redundancy check.
  - Checked at each transmission.
  - Should failure occur, a beam dump can be generated.

LHC Front End

- High Tension (HT) activation test
  - 100pA added, dynamic test.
  - Degradation of electronic can be detected.
  - In case limits are exceeded, no beam permission given.
  - To be carried out before each beam fill.

- HT modulation test
  - Capacitive current injection via ionization chamber electrodes.
  - Degradation of complete chain can be detected.
  - In case limits are exceeded, no beam permission given.
  - To be carried out before each beam fill.

Injector complex Front End



Circuit Breakers
Stop the failure propagation

Acquisition
digitisation of 8 channels

FPGA
Altera Cyclone IV

JTAG connection
Local programming and diagnostics

SFP connectors
Gigabit optical and/or Ethernet links

Backplane connection
Analogue inputs, power and control

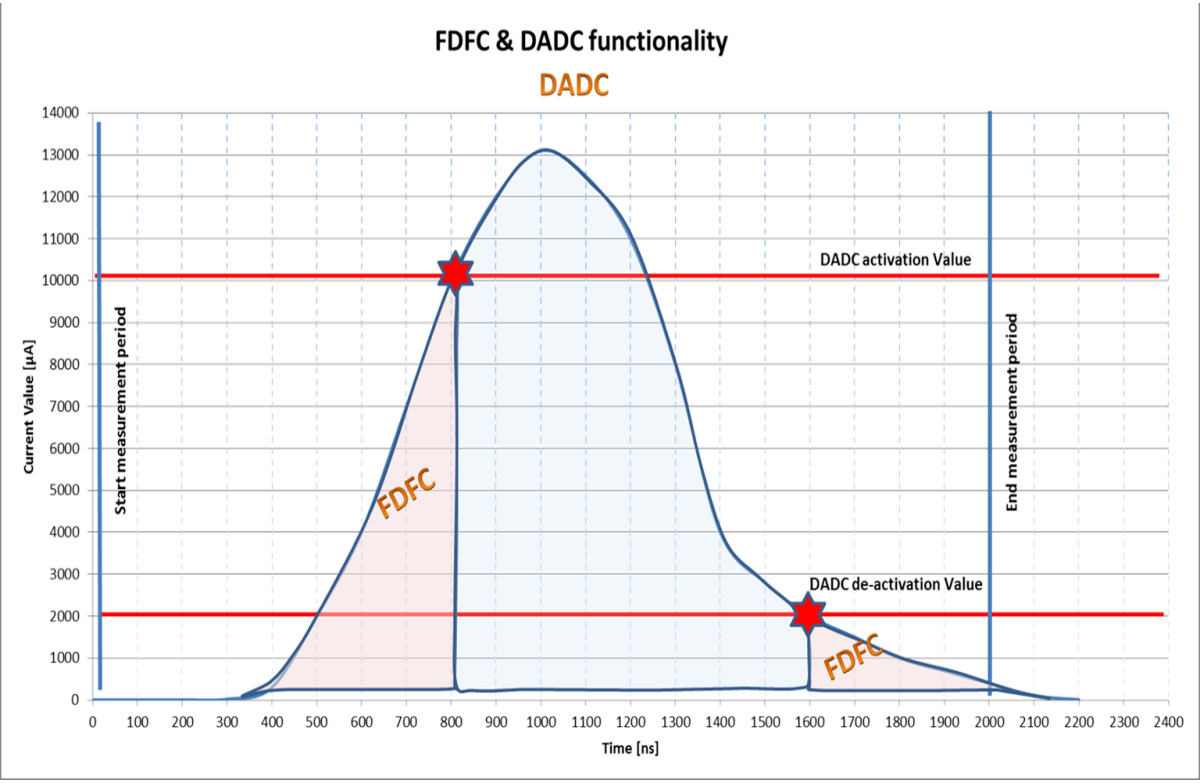
Local power supplies
Separated for Digital and Analog

Acquisition principle (ACFC & DADC)

by William Viganò

The input channel circuit is able to measure current input from 10pA to 200mA.
The measurement of the current input is performed by two different techniques:

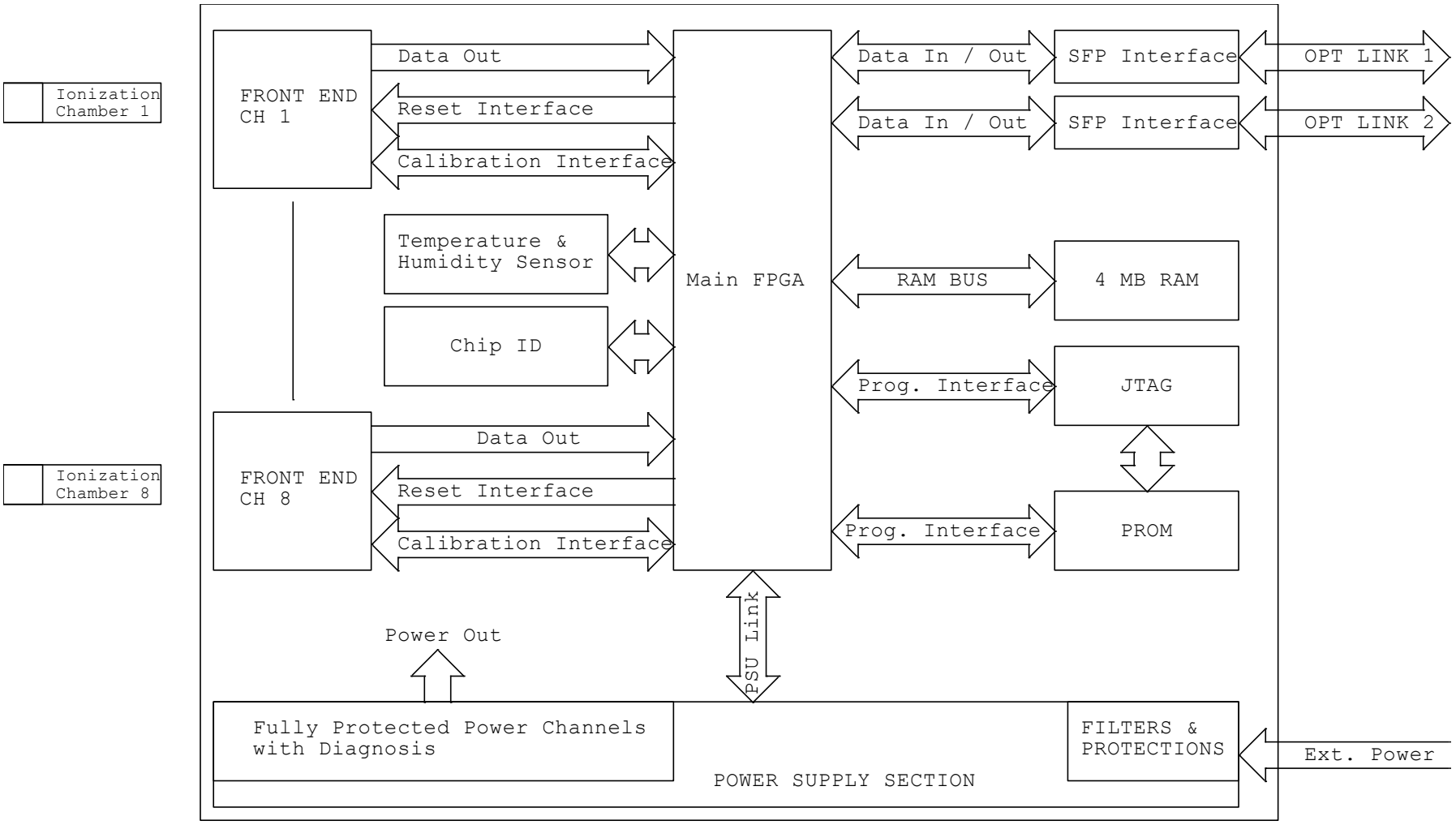
1) Fully Differential current to Frequency Converter (FDFC) used in the range **10pA to 10mA.**
2) Direct ADC acquisition (DADC) used in the range **100µA to 200mA.**



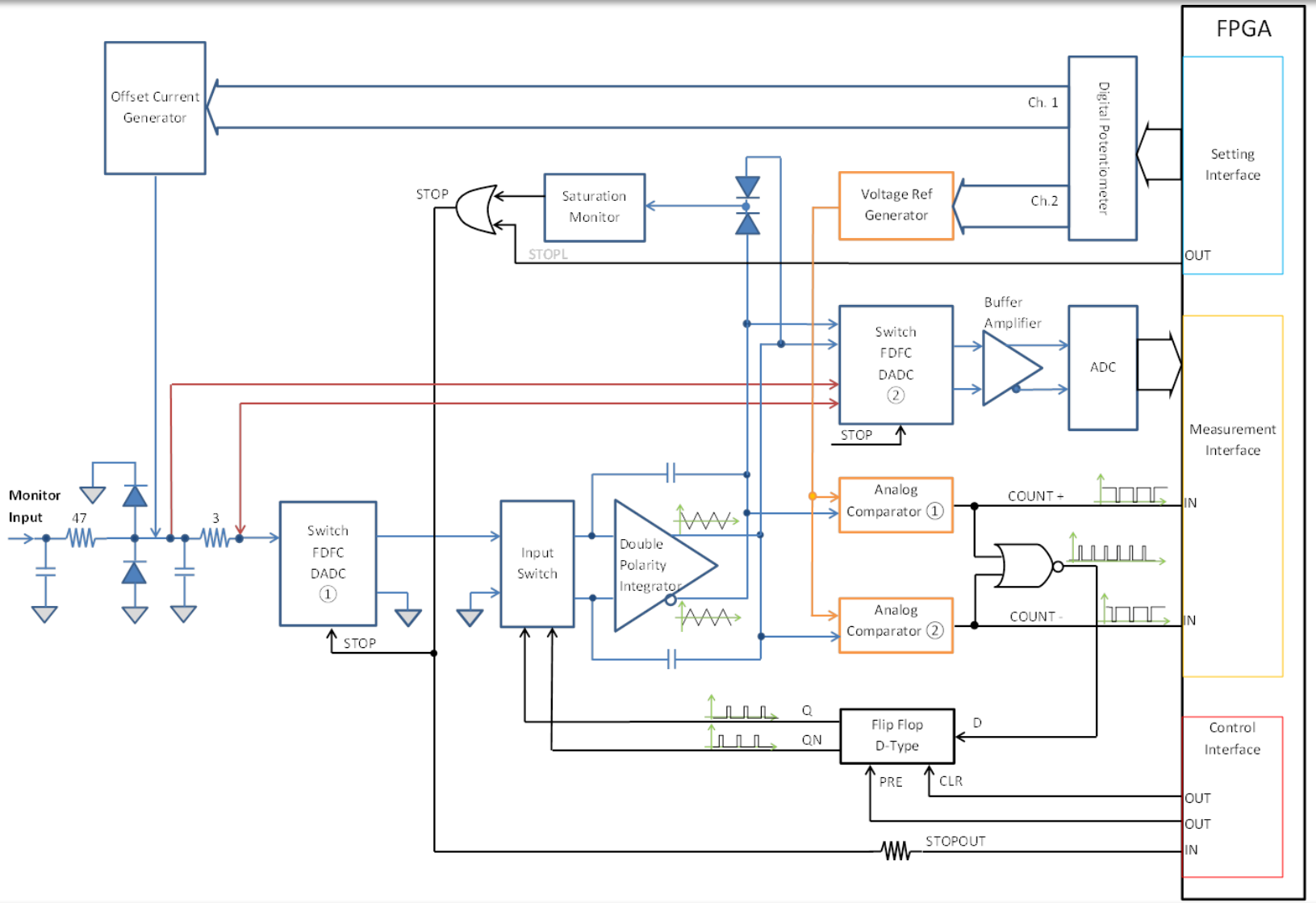
No gain change required:
The switch between the 2 ranges is managed by the *FPGA*.

- If the maximum FDFC counts is reached, the FPGA switches the circuit to the DADC mode.
- When the value of the DADC falls below a threshold, the FPGA switches the circuit to the FDFC mode.

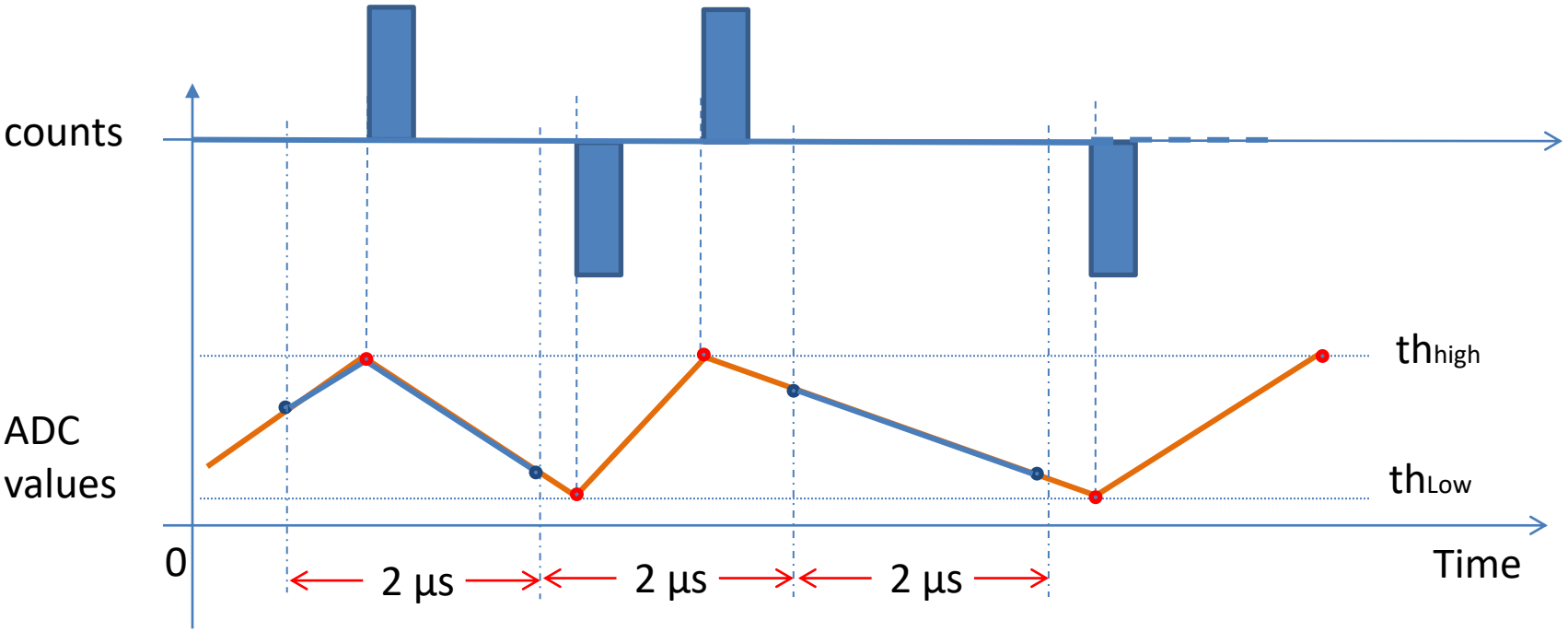
Injector complex Front End Block Diagram



Input Monitor Block Diagram



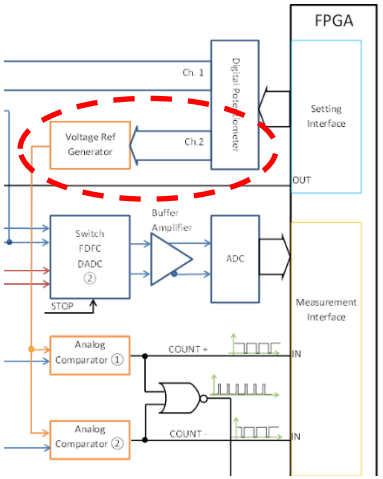
Injector complex Front End



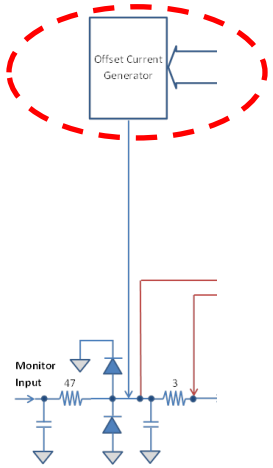
- The number of accumulated counts are combined with the ΔADC values to calculate the integrated loss over a 2 µs period.

Settings

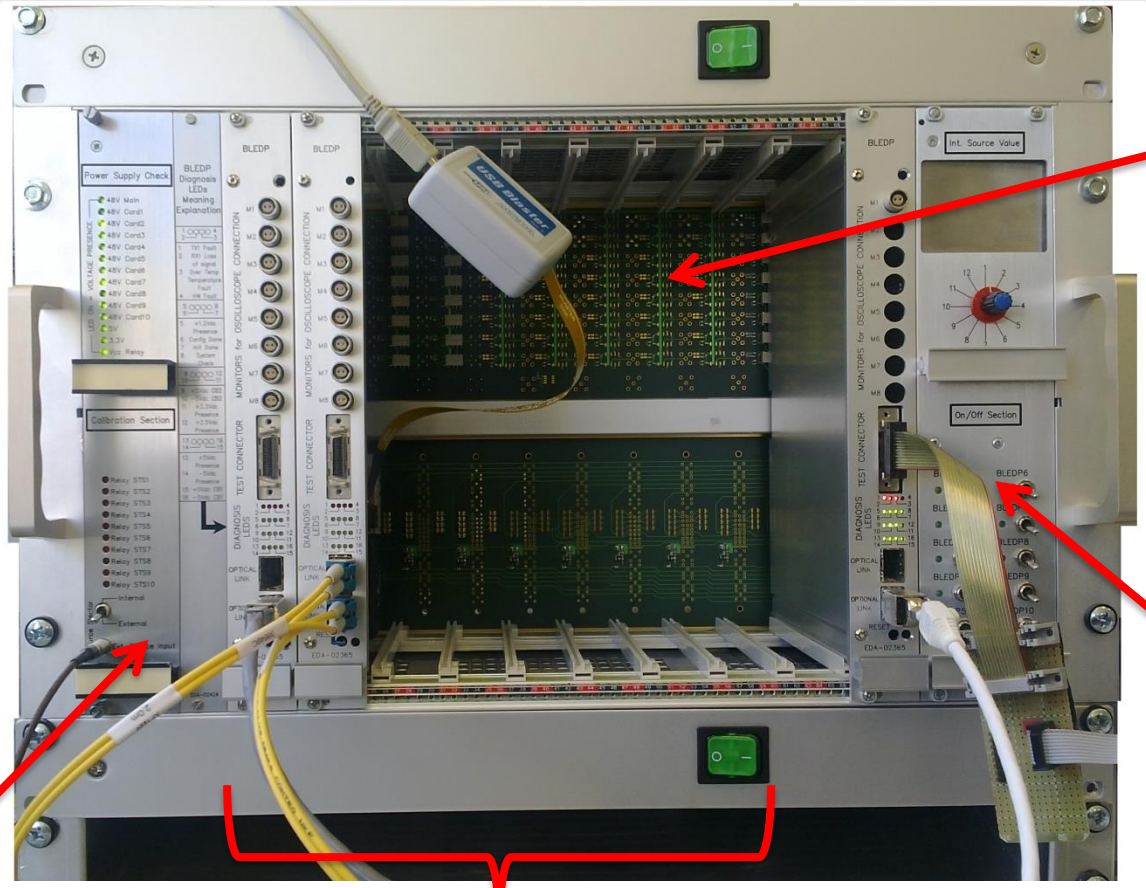
- Analog Comparator thresholds can be set by remote by means of digital potentiometers. That allows to calibrate the measurement executed by the Fully Differential Frequency Converter when a reference current is injected in the channel.



- Offset current can be set by remote by means of digital potentiometers. That allows a self-check of the channel when no signal is applied at the input.



Acquisition Crate



Custom Backplane
See next slides

Control Unit
Later version w/ advanced remote functions

Main panel

Acquisition module (BLEDP)
Up to 8 modules with 8 channel each

INSTALLATION OVERVIEW

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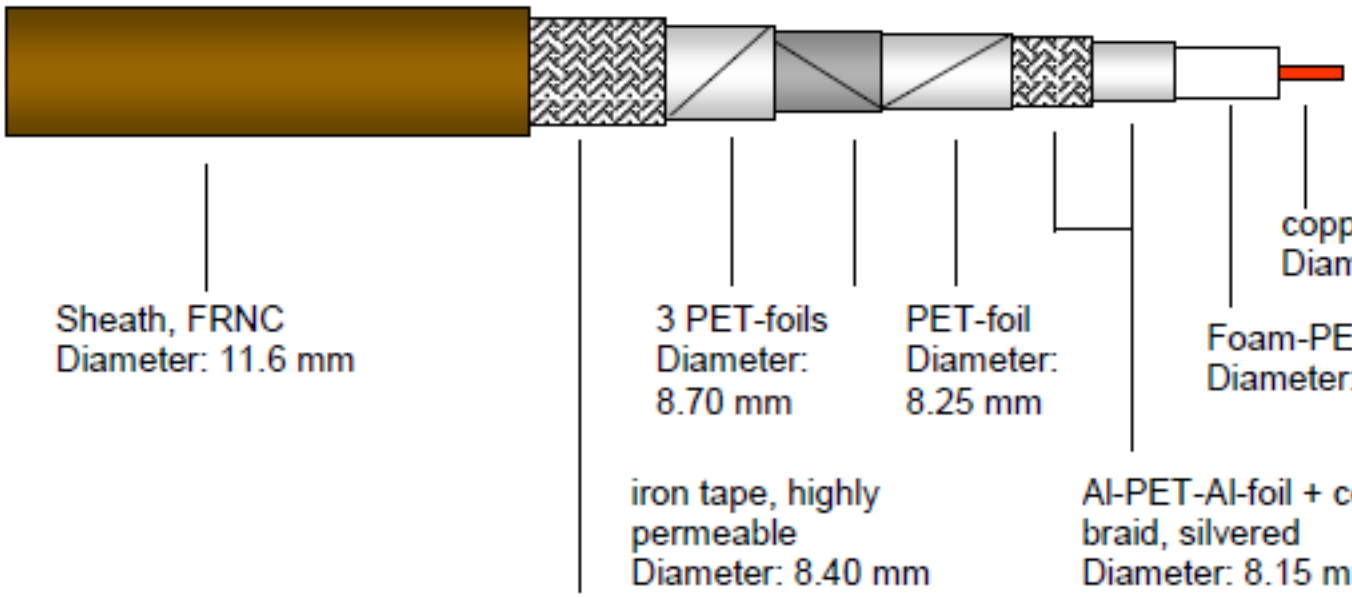
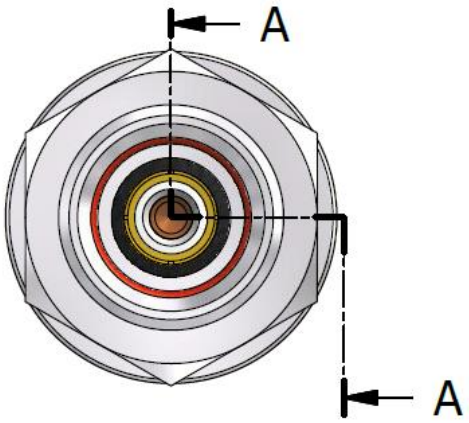
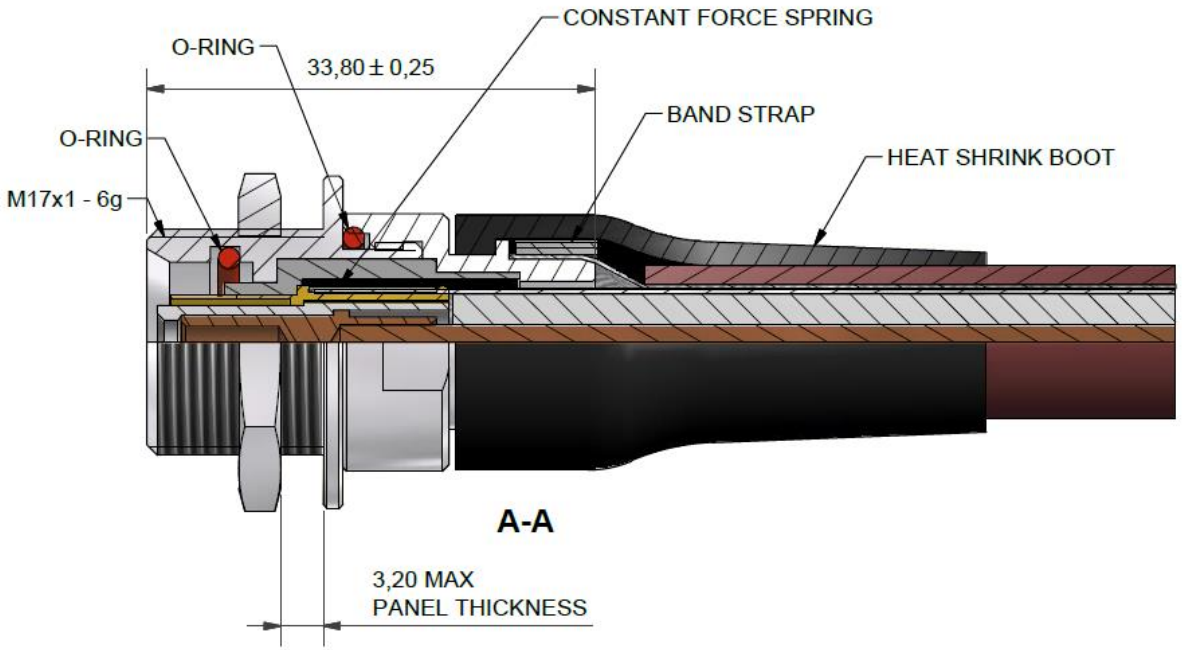
Signal Cable overview

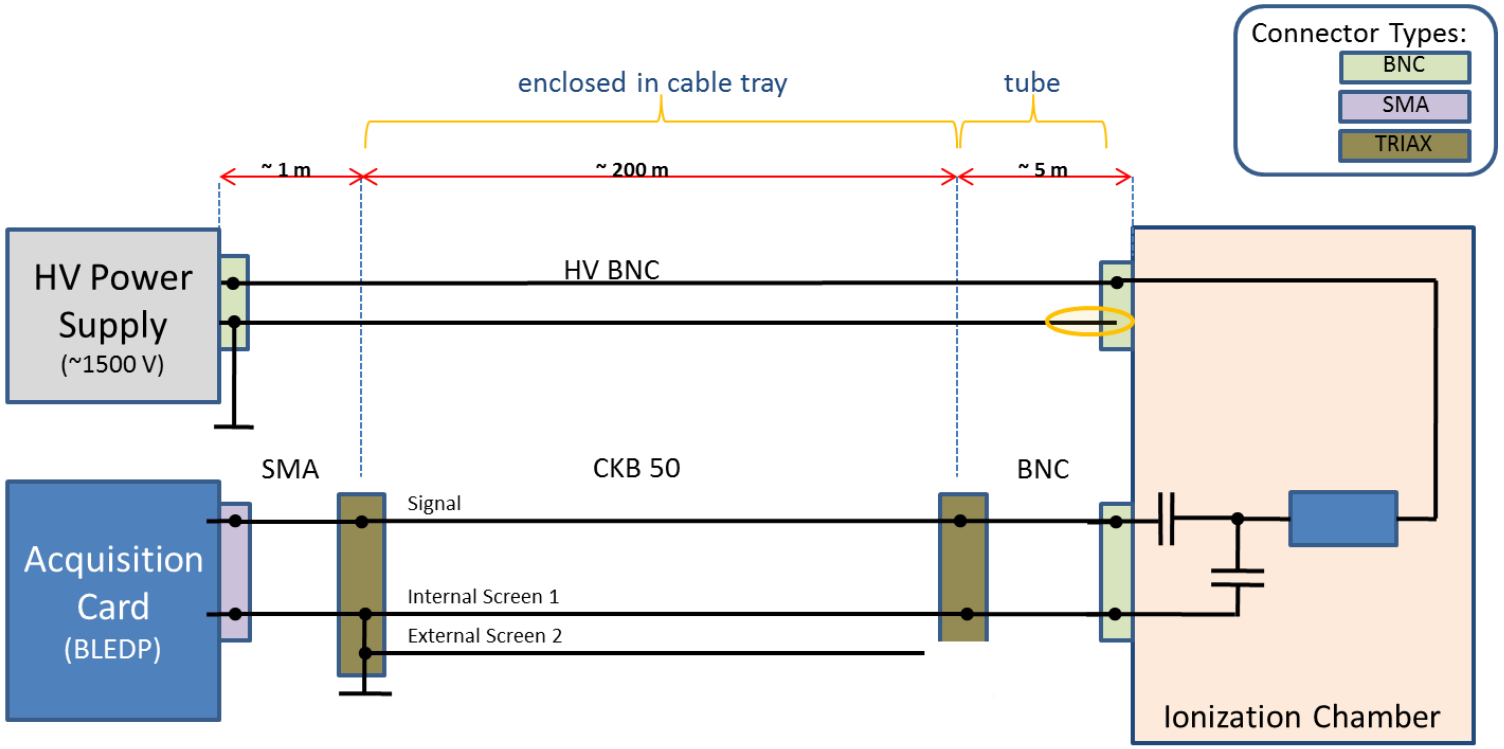


Signal Connector overview



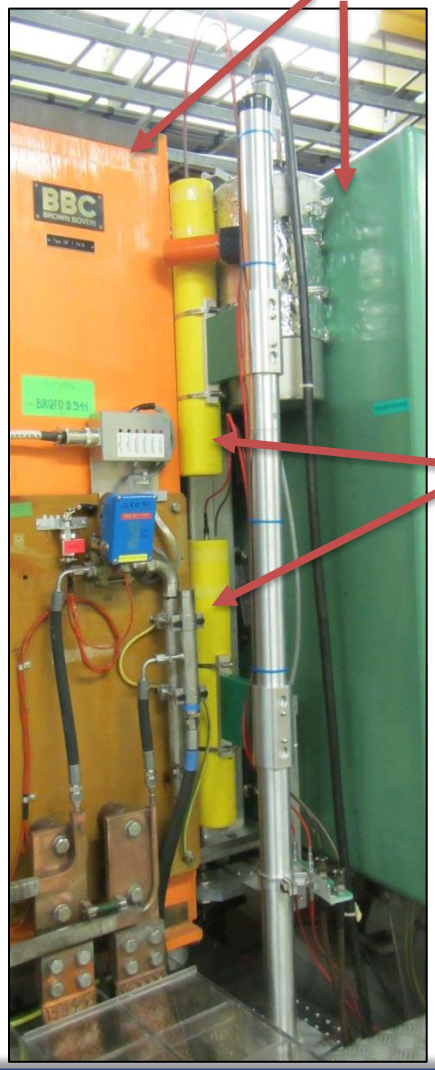


LINAC4 cabling



- External screen to **shield high frequency** noise.
- Internal screen to **shield low frequency** noise (GND only on electronic side, IC is floating).
- Screen of HV BNC is open on the IC side to assure there is **no ground loop**.
- CKB 50 up to 200m, BNC up to 2m

Proton Synchrotron Booster Installation



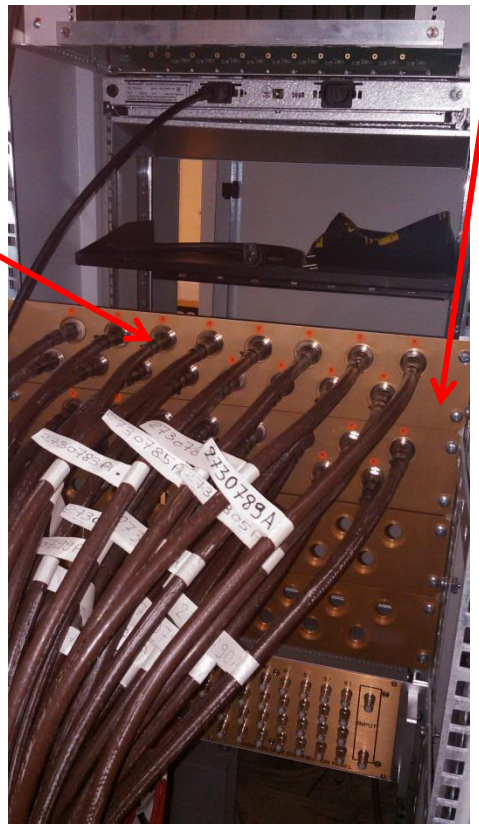
Proton Synchrotron Booster Installation

Patch panels

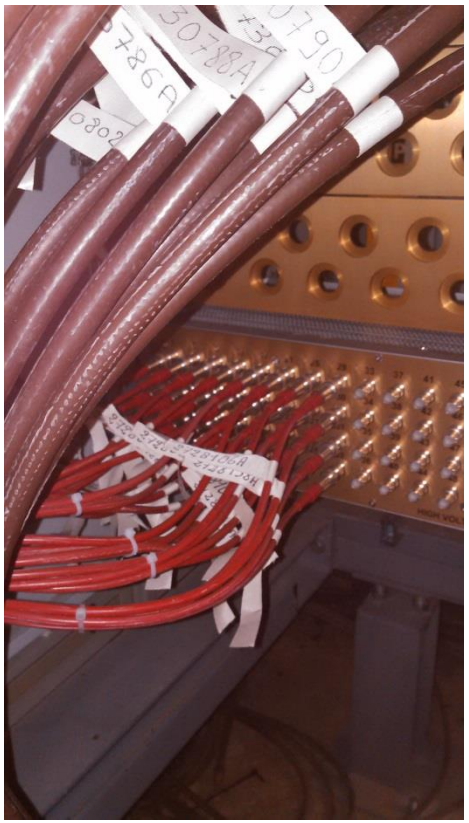
Custom cable CKC50

Patchcords

Signal and HV Patch-Cords



Signal Cables



HV Cables

Questions

Any questions?

THANK YOU

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