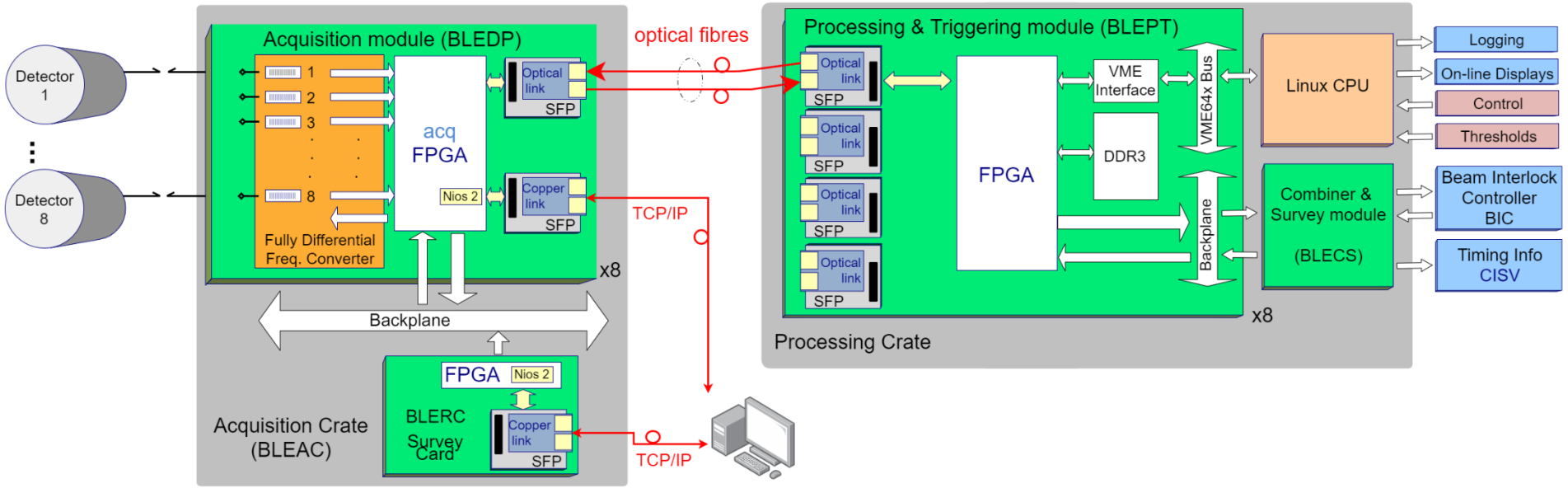
29th May 2020

REAL-TIME FPGA-BASED ALGORITHMS FOR THE BLM SYSTEM USED AT THE LHC INJECTORS COMPLEX

Outline

- Main characteristic of the acquisition card
- Working principle of the Fully Differential Frequency Coverter
- Data combination to increase the resolution of the FDFC method
- Acquisition method switching to increase the dynamic range
- Integration periods and thresholds comparison

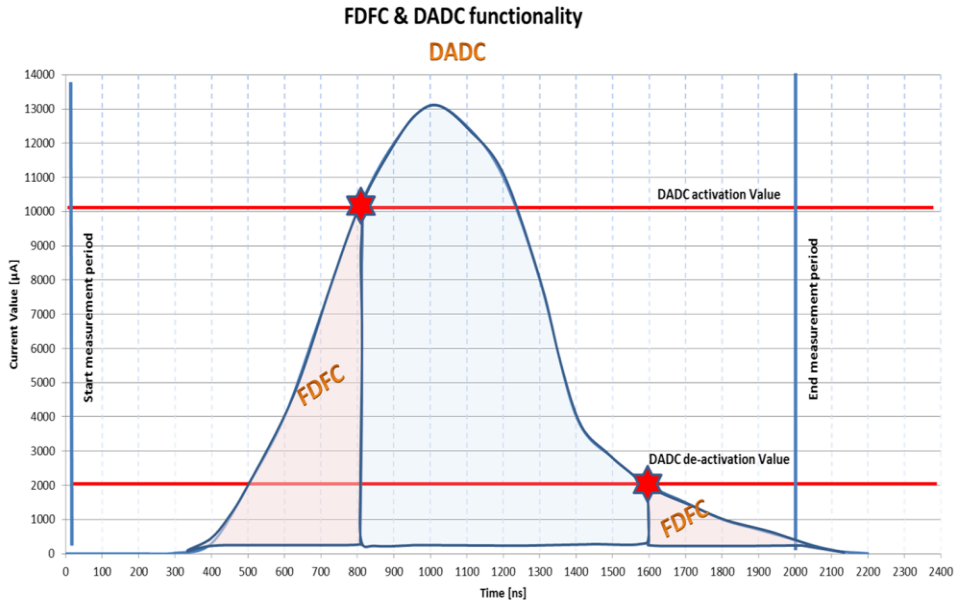
Injector Complex System Overview



Acquisition card: BLEDP card

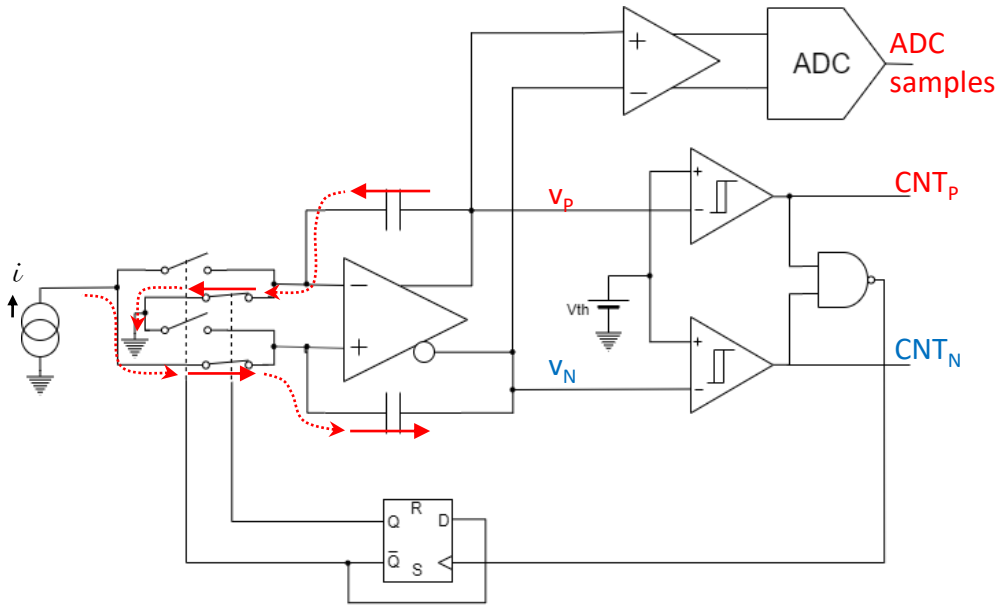
Main characteristics:

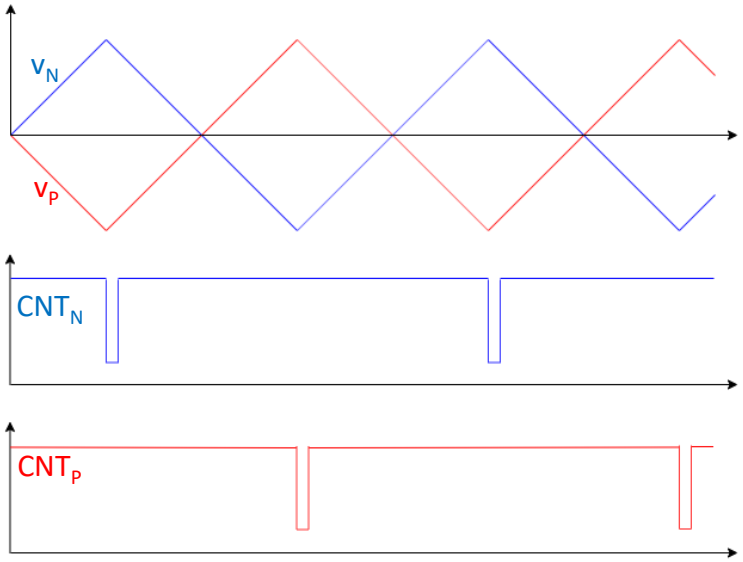
- 8 independent acquisition channels per card
- Measurement range : **10pA to 200 mA** ($2 \cdot 10^{10}$), using 2 acquisition methods with overlapping dynamic ranges:
  - Fully Differential Frequency Coverter **(FDFC) : 10pA-10mA**
  - Direct Digital to Analog Conversion **(DADC)** of the current through a shunt reference: **100uA-200mA**
- Minimum acquisition period is 2 us
- The digitised value is transmitted through optical fiber to the post-processing module or through a Gigabit Ethernet link to a client application (stand-alone mode)



- Both acquisition chains are acquired with the same ADC.
- No gain change required
- The switching between the 2 ranges is managed by the FPGA and is independent to each channel.

Principle of the FDFC acq. method





- A charge-balanced differential integrator circuit integrates the current from the beam loss detector.
- Two comparators check the voltage of each branch against a threshold. Whenever the any of the voltages exceeds the threshold, the signals controlling the switches change to their complementary and the input current is then routed to the other integrator branch.
- A 16-bit ADC periodically samples the differential voltage at the integrator output.

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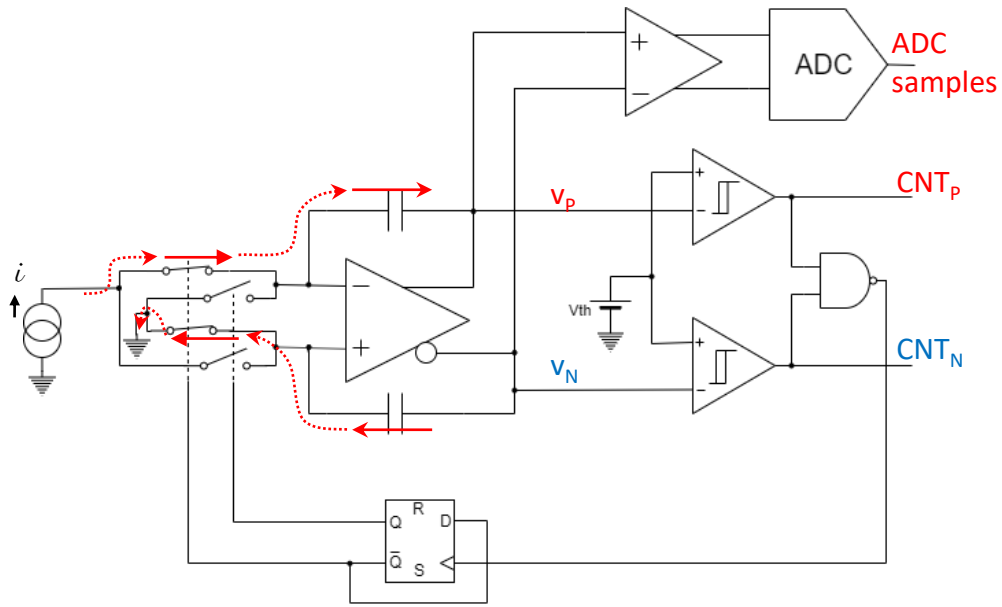

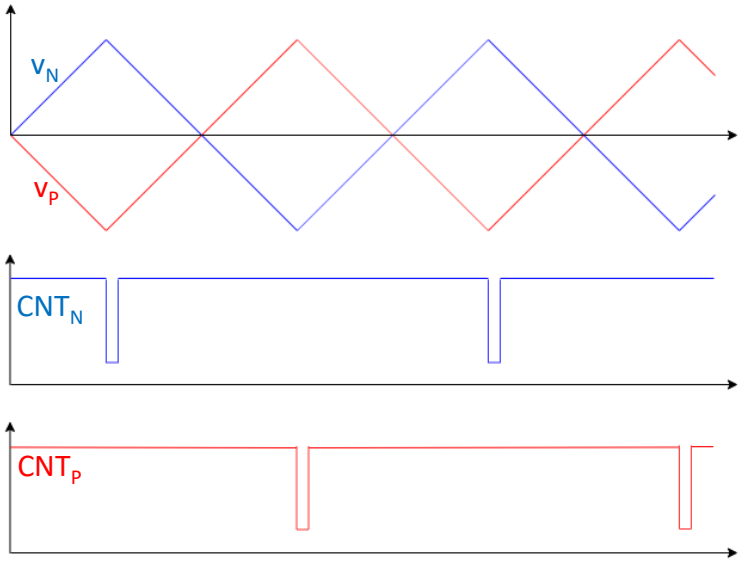

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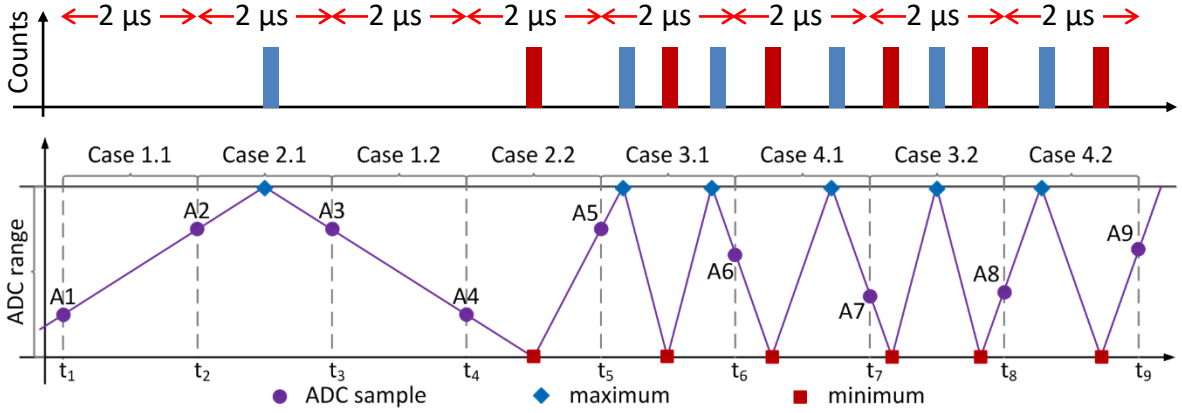
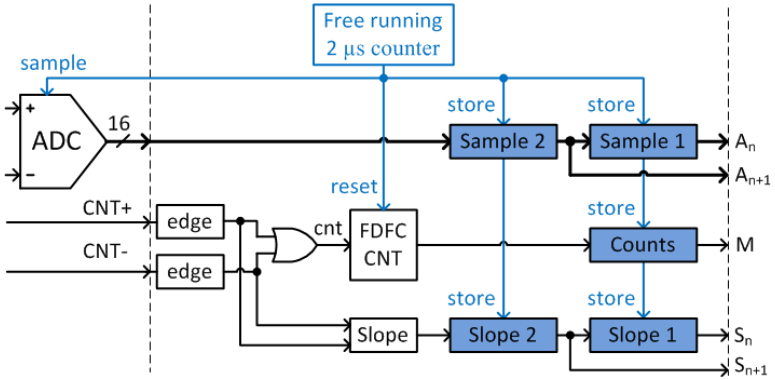
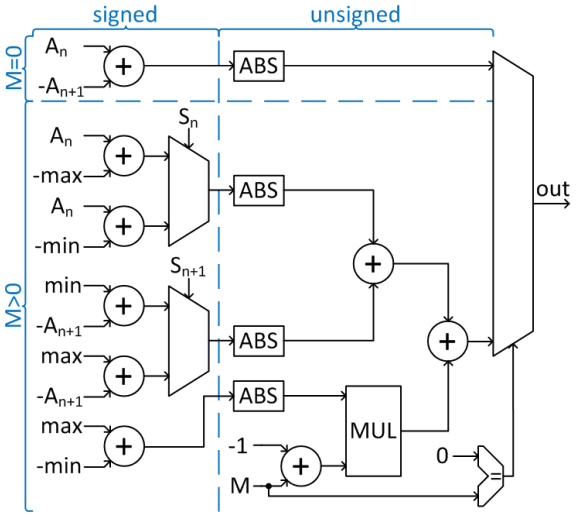
Data combination for the FDFC acq. Mode (II)



Case	Calculation
1.1	A_{n+1}-A_n
1.2	A_n-A_{n+1}
2.1	(max-A_n) + (max-A_{n+1})
2.2	(A_n-min) + (A_{n+1}-min)
3.1	(max-A_n) + (max-A_{n+1}) + (M-1) * (max-min)
3.2	(A_n-min) + (A_{n+1}-min) + (M-1) * (max-min)
4.1	(A_n-min) + (max-A_{n+1}) + (M-1) * (max-min)
4.2	(max-A_n) + (A_{n+1}-min) + (M-1) * (max-min)

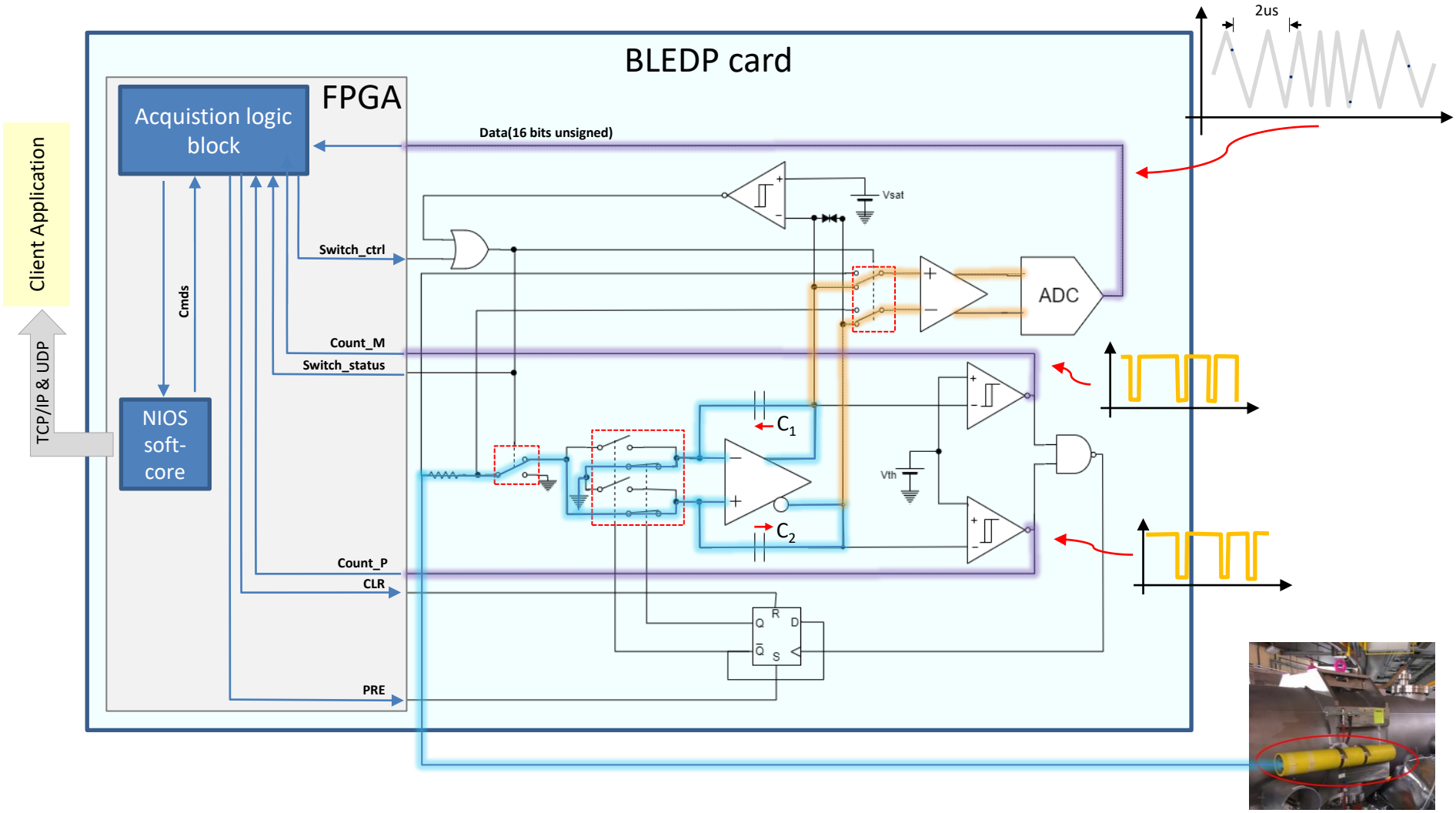
- In order to evaluate the integral between two samples the algorithm needs to cover eight cases.
- By tracking the slope and using the absolute value of the differences the realisation in the FPGA is significantly optimised.



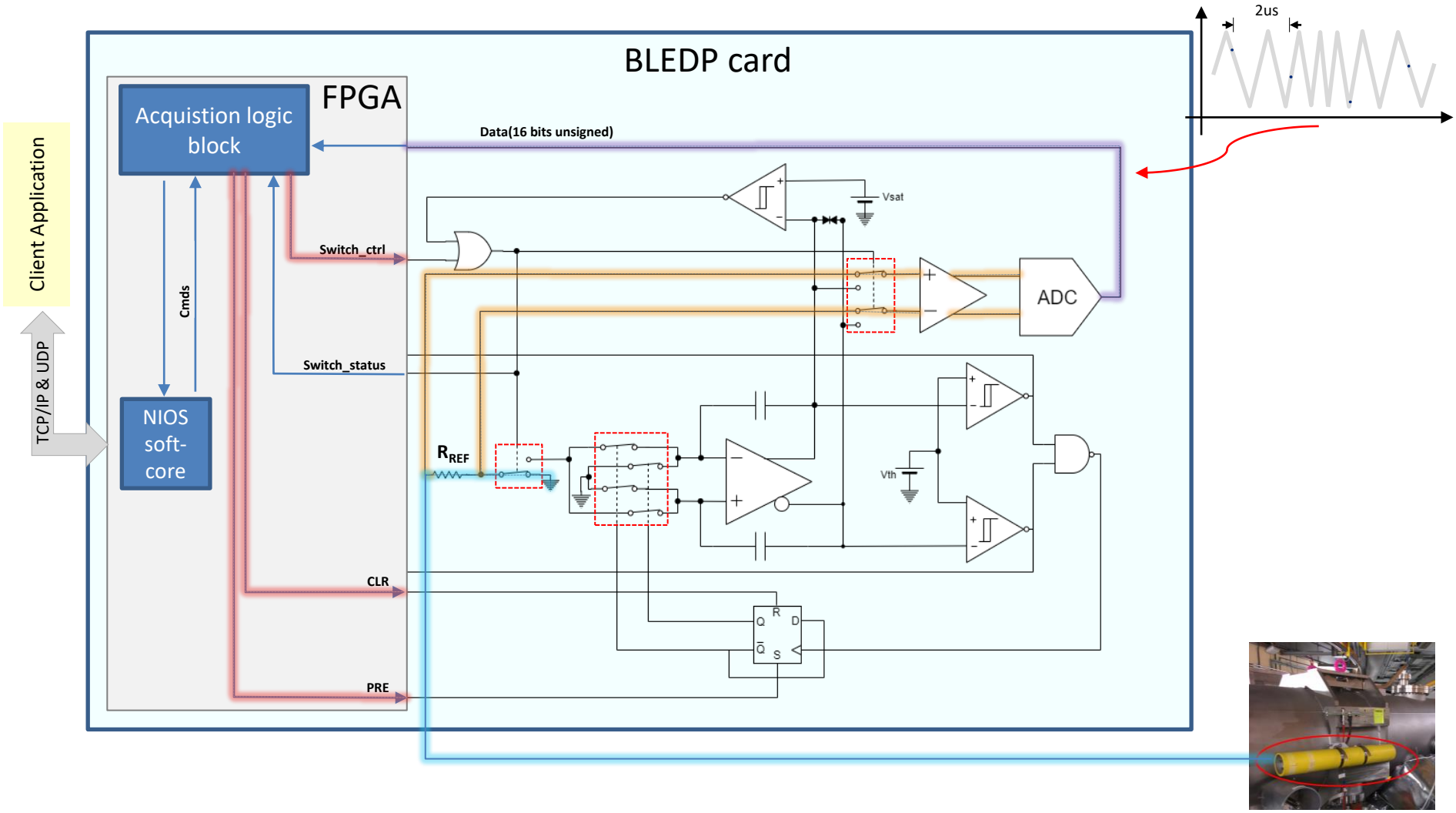


- The above is for an ideal circuit. In reality an additional stage is introduced to compensate for switching delays and other effects.

Acquisition method switching (I)

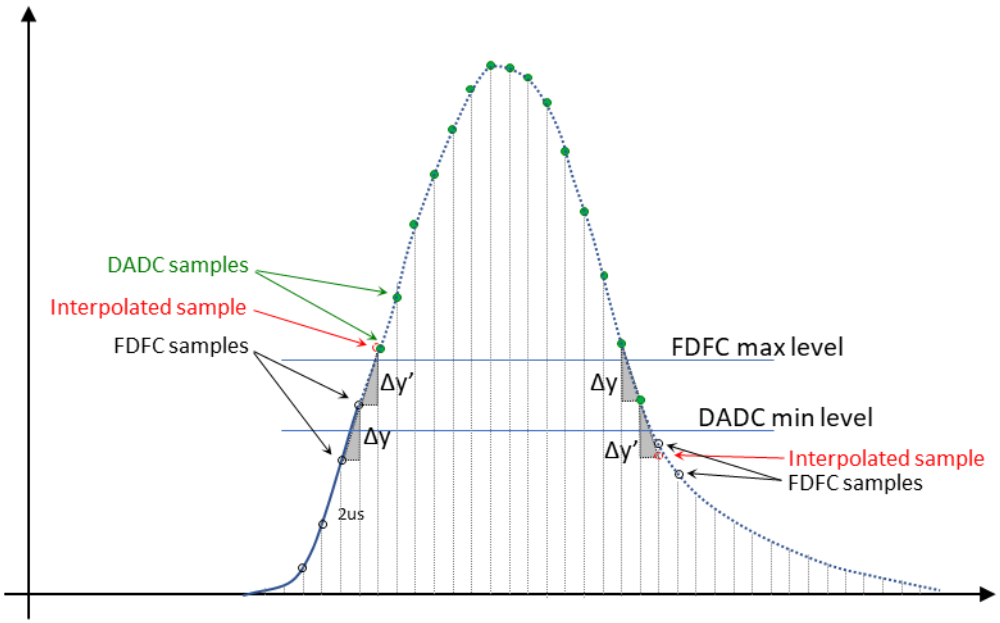


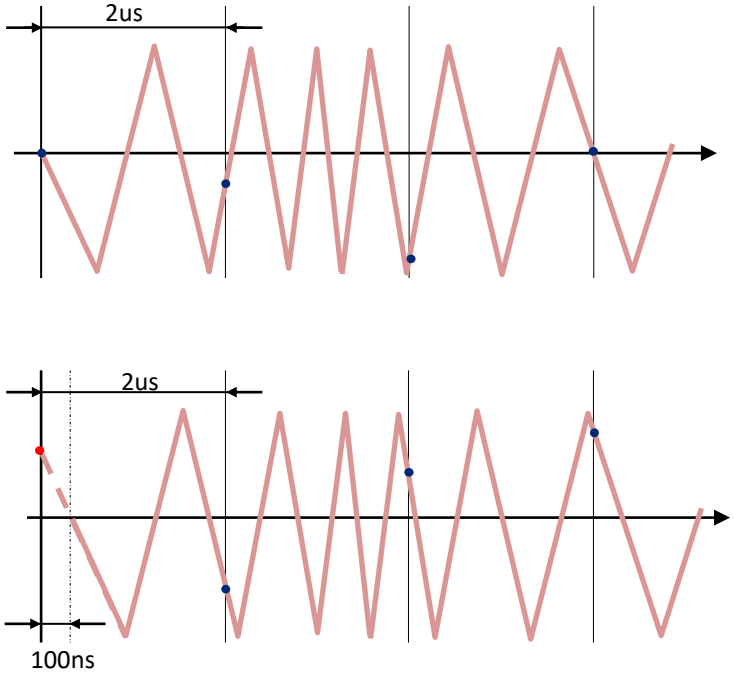
Acquisition method switching (II)



Automatic acq. method switching

FDFC → DADC switch is easier since it only requires one sample
DADC → FDFC is an integration → Every FDFC result requires 2 samples





- Default mode at startup is FDFC
- Every time we receive a new sample, the next sample is estimated based on the increment seen between the last two (using a linear interpolation).
- If the estimated value goes beyond the switching threshold, the command to change switches position is sent.

- Switches are not instantenous. So the first FDFC sample did not integrate all the current.
- After switching, a previous FDFC sample is estimated, assuming that for about ~100ns the last DADC current calculated was constant and integrated.

Integration periods and threshold comparisons

The processing card (BLEPT) continuously calculates 4 **integration period values** per channel and compares them against thresholds

Hardware implementation part:

- All calculated **integration period values (2us, 400us, 1ms and 1.2s)** are constantly checked against their threshold values:
  - 4 threshold values, one for each of the integration periods.
  - Comparisons happen at the refresh period – that is, every 2 μs
  - In the case the measured values exceed those the beam permit signal is removed for **all users**
  - The **blocked** beam permit signal will be **latched** until an operator acknowledges.
- The **threshold values** are set **per channel:**
  - Each card will process 8 channels

Software implementation part:

- All maximum **integration period values** recorded on the cycle will be checked against a second set of threshold values. The outputs are used for **repeated over threshold function**
  - Additional threshold values for the same integration periods.
  - In the case found to be over threshold repeatedly *n* times, **that user's injections** are blocked.
  - The **blocked** beam permit signal is **latched** until an operator acknowledges.
  - The repeat value *n* is be settable per monitor in the range of 1 to 16.
- The **threshold values** are **unique per user and per channel:**
  - Each CPU will process 8 cards x 8 channels
  - The information of the current user is obtained from the telegram per cycle -> dedicated **timing card**
  - Memory for up to 32 users is reserved.

References:

[1] A real-time FPGA based algorithm for the combination of beam loss acquisition methods used for measurement dynamic range expansion. M. Kwiatkowski, C. Zamantzas, M. Alsdorf, B. Dehning, W. Vigano. International Beam Instrumentation Conference, Tsukuba, Japan, Oct 2012.

[2] 10 orders of magnitude current measurement digitisers for the CERN beam loss systems. W. Viganò, M. Alsdorf, B. Dehning, M. Kwiatkowski, G. G. Venturini, C. Zamantzas. TWEPP, Perugia, Italy, Sept 2013.

[3] System Architecture for measuring and monitoring beam losses in the injector complex. C. Zamantzas, M. Alsdorf, B. Dehning, S. Jackson, M. Kwiatkowski, W. Vigano. International Beam Instrumentation Conference, Tsukuba, Japan, Oct 2012.

Any questions?

THANK YOU