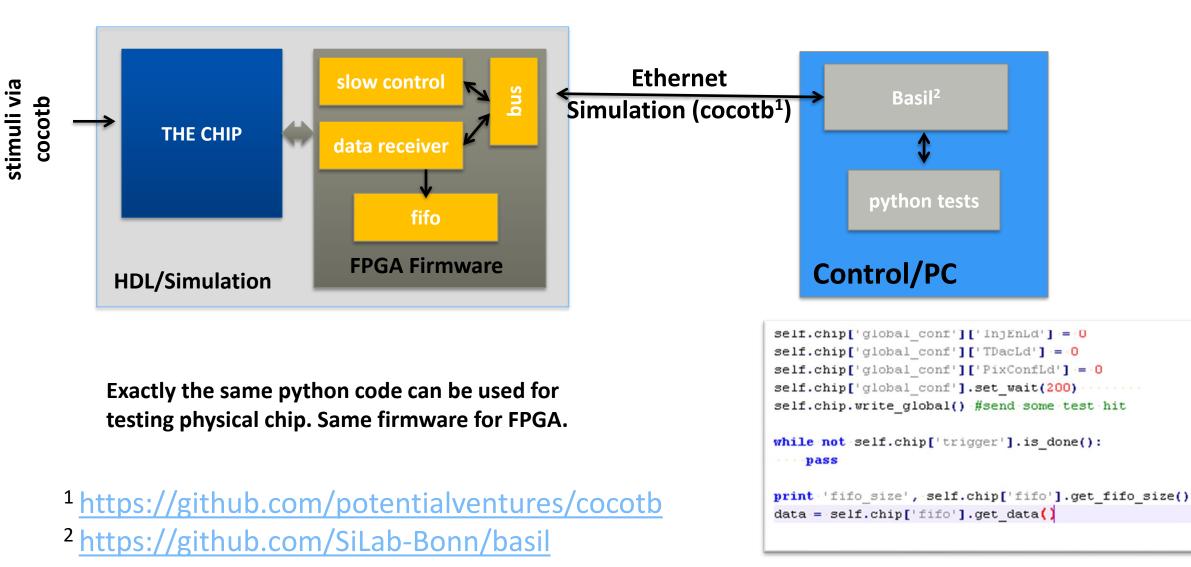




WE USE IN BONN

Tomasz Hemperek

UNIVERSITÄT BONN SI LAB Digital design and Verification



UNIVERSITÄT BONN SI LAB Project organization

Use content management system for everything

file Project Modify Alles Select Tree Devision 1940 Server: ATPLX Project: ATPLX Work Area: Anne-Ansers/Highman/Calesign/ATPDX:Reson/Wesign_wa. + Selected: 0 + Checked Out. 3 Hierarchy ocked CI By CI Time Diarge Sumary Greate 8-0.040 dgnani 2009/10/12 18:14 Automatically checking in directory n21 2009/08/19 13:28 Automatically checking in directory Ok Out ID-Chode. 🖶 🗘 digital 🖶 🗗 thenper 2009/10/13 12:36 Automatically checking in directory 08.8 dgmani 2008/06/03 10:31 Automatically checking in directory B-Odoce B Cos ### amekkan 2009/10/29 12:01 Automatically checking in directory Decard - PETH, ALBONCS nkarago 2009/10/14 02:17 Tag FET4_A_CLROEN ## akruth 2009/10/16 05:32 beccher 2009/10/23 03:16 Automatically checking in directory CITELA, A.DE DAT FET-LALOFFREN nenoun1 2009/10/21 11:40 FELALALOREF vgreeov 2009/10/29 10/22 History FEL4_A_DACS anokkan 2009/10/22 17:14 FET4.A.DODC dgnani 2009/10/01 15:20 autocheckin Set 1st FETALALOC thenper 2009/10/13 05:47 Automatically checking in directory THE - FEE4_A.000 dgnani 2009/09/22 09:05 FET4.A.ETUSE J1fleur 2008/10/22 16:41 Out FEI4_0_EOCH vladiz 2009/10/27 04(22 dgnani 2009/09/22 09:05 FELA A EDDEL **Update** TELLATOO anekkao 2009/10/27 17:48 FETALALIAN # # nkarago 2009/10/27 11:11 FELALOFINE j1/1eur 2009/09/30 13:52 - FET4, A. POR thenper 2009/10/15 17:54 31Flour 2009/10/21 15:49 sutocheckin Cut of sync anekkao 2009/09/21 12:48 PET4, A. 31.00 nkarago 2009/10/27 11:14 FELLATOP anekkas 2009/09/01 09:44 geruole 2009/10/29 11:50 FEIALALTEMPSETELG/CC #- FET4_A_1090 ametikan 2009/08/28 10:35 FEELAN WE F dgmani 2009/10/20 23:43 Automatically checking in directory FETALAL LOOKE dgnani 2009/10/29 10:03 nkaragn 2009/10/21 13:35 testechildet PERCommon out vialed out locally 1/16/08:01 common out vialed custon vias B Ciscricts denatii 008/06/05 10:39 Automatically checking in directory - diff.out - history.out -D sos . log

SoS for OA

all the test GIT

b silab > tj-monopix2							
T tj-monopix2 Project ID: 60467	۵						
û → Unstar 5 💱 F	Fork 1						
🗢 344 Commits 🗜 10 Branches 🖉 0 Tags 🖻 115.8 MB Files 🗟 359.5 MB Storage							
master v tjmonopix2 / + v History Find file Web IDE 🛃 v Clone v							
add 320MHz simulation Toko Hirono authored 6	-	★ f2432c00 f ²					
README CI/CD configu	uration Add LICENSE Add CHANGE	LOG					
Add CONTRIBUTING							
Name	Last commit	Last update					
🖨 data	BUG fix path (again)	7 months ago					
adoc	DOC: Current status of configur	1 year ago					
🖨 firmware/src	add 320MHz simulations	6 months ago					
🖿 src	Fix sdf export	6 months ago					

UNIVERSITÄT BONN SI LABB Continuous Integration

Use pytest* as testing framework



Use GitLab CI* to run test on every code change

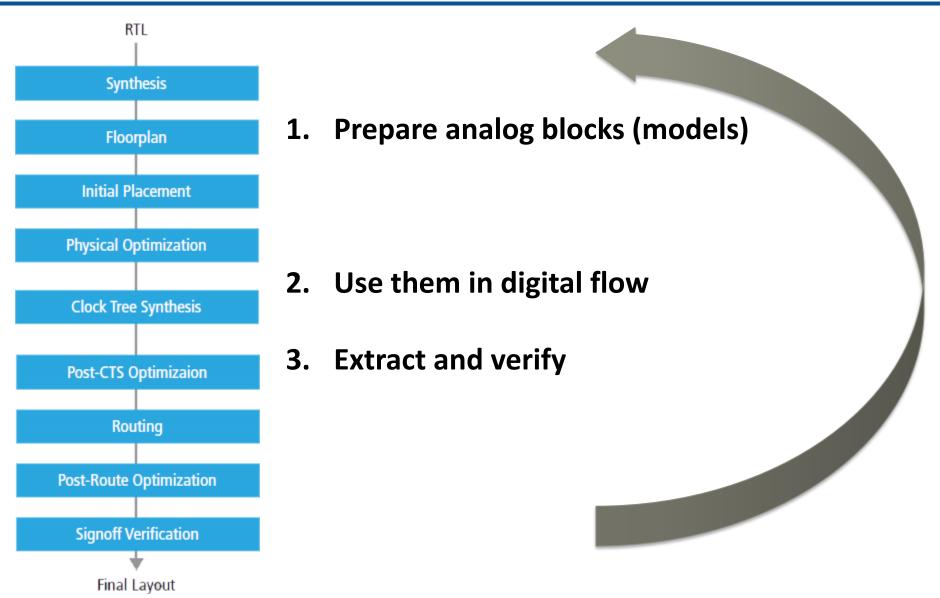
i 🤎 și	ab / bdaq53 🛩		This project	cī Search □. + • [
		Pipelines Jobs Scher	dules Environments	Charts
All 35	Pending (0) Runn	ing (8) Finished (96) Branches	Tags	
tabus	Pipeline	Commit	Stages	
⊘ passed	#233291 by 🍘	P master -> 5447/cc3	\odot	⊕ 00:15:29 ∰ about an hour ago
⊘ passed	#233285 by 🛞	P fife_readout ⇔ 8xbs2x89 Fife readout test now working	\odot	ტ 00:09:45 ∰ about an hour ago
⊗ passed	#232593 by 🛞	P master ⊕ fócc@d7 Merge branch 'Test_Pipeline' into '_	۲	⊕ 00:14:38 about 21 hours ago
© passed	#232559 by 🛞	P Test_Pipeline ← fdbbb217 Merge branch 'master' into 'Test_PL.	\odot	
⊗ passed	#232535 by 🛞	P Text_Pipeline \Rightarrow 2650e414 FDC Foxd Pipeline failure	\odot	6 00:14:21 ∰ about 22 hours ago
⊚ failed	#232494 by 🛞	P Test_Pipeline ← 454af72a FD0 Faxed Pipeline failure	۲	⊚ 00:09:33 ∰ about 23 hours ago
S canceled	#232484 by 🛞	P master + d1da383e	\odot	@ 00:00:45

* or similar

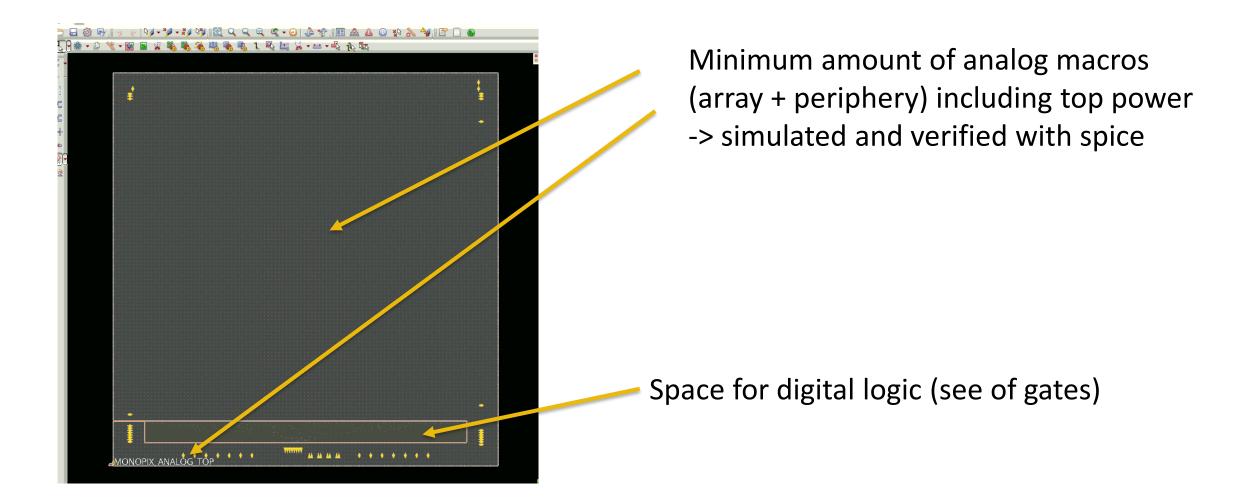


1		1		
2	Task	test name to launch	Notes	Status
3	TRG new feature	switcher_test		done
4	Gated mode	switcher_test		done
5				
6	Behavior during switching of trigger (read-out) modes ? Needs detailed verification	switcher_test	veto triggered several times and the correct behavior was observed	done
7	row data record and send	extended_test		done
8	pedestal update	extended_test		done
9	hit recognition	vszs_test_vsim		done
10	Test on random data	vszs_test_vsim		done
11	include random pedestals	extended_test		done
12	trigger test	extended_test		done
13	check hammming correction on if working	ecc_test		done
14	read_back_erros	ecc_test		done
15	common mode algorythm(+ overflow)	cm overflow test		done

UNIVERSITÄT BONN SI LAB Flow (Digital on Top)









- For all Analog macro
 - Verilog model
 - Liberty file
 - Power grid model (we did not use this yet)
 - Proper netlist for LVS

- Verified in spice



- Timing
- Power
- IR/EM
- Gate level simulation
- FastSpice (with limited pixel array size)



