# Chip layout
# &
# Mechanics/Cooling/Integration

## (ALICE: learnt that lesson)

S. Bettarini - INFN & Univ. Pisa
On behalf of the VTX Mechanical «Team»

# Belle II Vertex Detector Upgrade Spec's

Transparent and precise silicon pixel detector for vertexing in ultra high luminosity:

$\mathcal{L} = 10^{36}$ cm$^{-2}$s$^{-1}$, TID = 100 Mrad, $\phi = 10^{14}$ n-eq

Target:

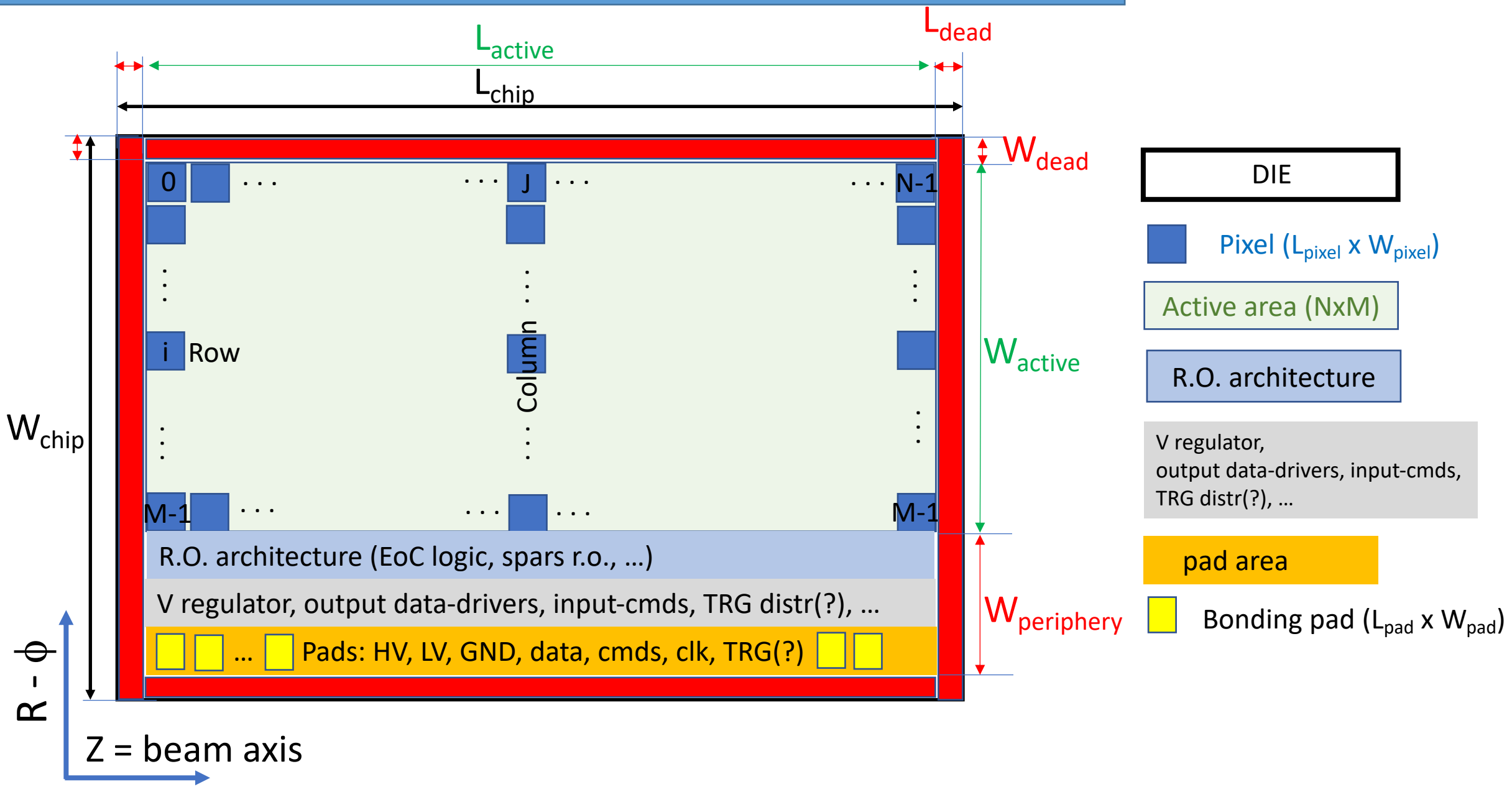
- Fully monolithic vertex detector
- Radius range [14,140] mm
- 30x30 µm$^2$ pixel pitch (single point res. 10-15 µm)
- T ~ 25-100 ns integration time
- Total power budget ~ O(kW)
- 0.1% $X_0$ (inner) – 0.3→0.5% $X_0$ (outer)

The choices on the (1!) chip design have a high IMPACT on the module/ladder mechanics!

After setting the general VTX spec's, their actual implementation in a conceptual detector design depends strongly on the «candidate chip» layout.
VTX mechanics provides some geometrical requirements on the chip dimensions.

To make a (common) step forward in the design of the module/ladder prototypes, it is needed to make hypotesis on the layout of the candidate chip, according to the constraints dictated by the chosen (TJ 180 nm) CMOS process/technology.

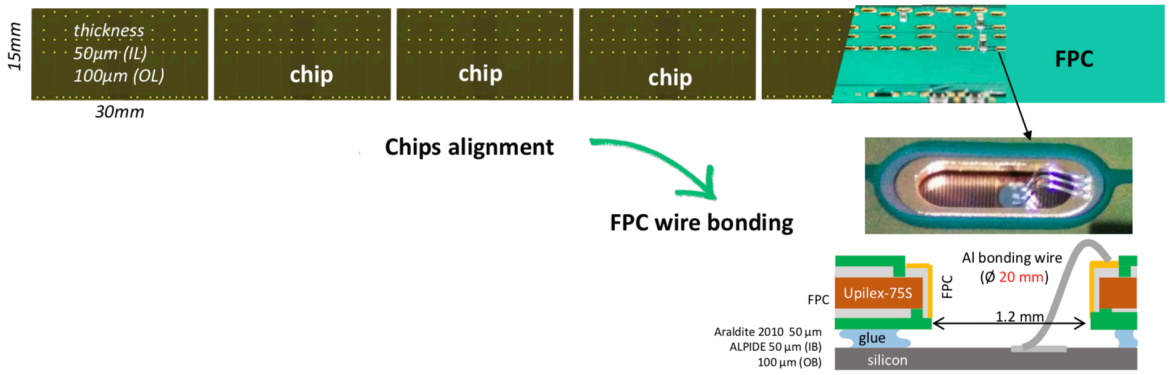
# MY (NAÏVE) IDEA ON the "FINAL CHIP" LAYOUT



# Questions (to the designers of “OBELIX”):

- Consideration on efficiency/cost → 1! Chip for the whole VTX, right?
- Can be all the pads placed only on one side (on the periphery) of the chip, to have dead-region only on one (r-$\phi$) side of the module/ladder? Or power pads to the matrix and to the periphery must be routed/taken separated?

- e.g.: ALPIDE has power/bias pads all over its surface (perhaps to distribute power w/o significant drop). This would always need a flex-circuit on the module, with deep-access bondings, also for the VTX inner layers!




- Identified design: CMOS -process TJ-180 nm:
  - are there limits on the max. $L_{chip}$ / $W_{chip}$?
  - stitching? (the larger the chip, the better for the oVTX ladder).
  - edge-less: do we have idea of $L_{dead}$ / $W_{dead}$? Guard ring(s)?

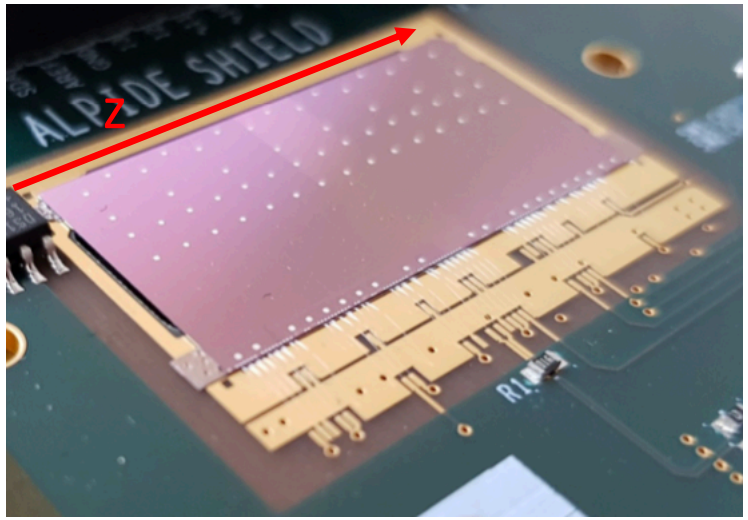
- After implementing all the wanted “feature”
  - estimated $P_{specific}$ < 200 mW/cm$^2$?
  - $W_{periphery}$ / $W_{chip}$ = o (10 %)?

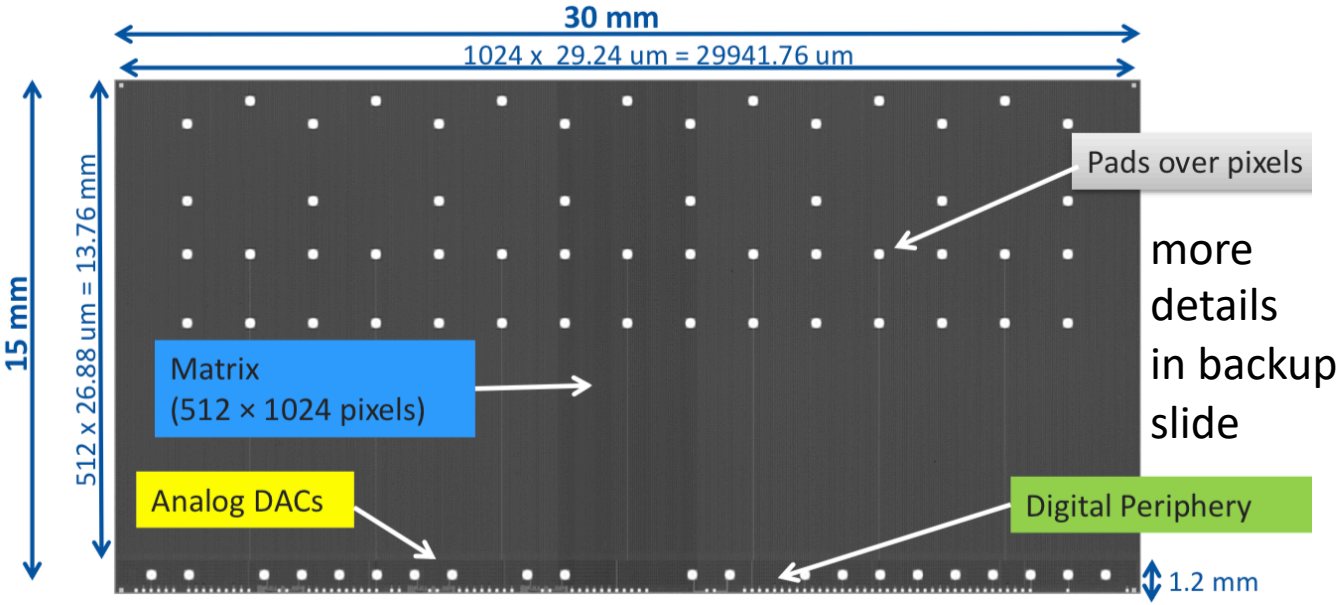
| | TJ-Monopix1 | TJ-Monopix2 |
|---|---|---|
| **Chip Size** | 1x2 cm$^2$ (224x448 pix) | 2x2 cm$^2$ (512x512 pix) |
| **Pixel size** | 36 × 40 µm$^2$ | 33.04 × 33.04 µm$^2$ |
| **Total matrix power** | 130 mW/cm$^2$ | 170 mW/cm$^2$ |
| **Noise** | ≅11 e$^-$ | < 8 e$^-$ (improved FE) |
| **LE/TE time stamp** | 6-bit | 7-bit |
| **Threshold Dispersion** | ≅ 30 e$^-$ rms | < 10 e$^-$ rms (improved FE + tuning) |
| **Minimum threshold** | ≅ 300 - 400 e$^-$ | < 200 e$^-$ |
| **In-time threshold** | ≅ 350 - 450 e$^-$ | < 250 - 300 e$^-$ |
| **Efficiency at $10^{15}$ $n_{eq}$/cm$^2$, 30 µm epi** | ≅ 87 % | > 97 % |
| **Efficiency at $10^{15}$ $n_{eq}$/cm$^2$, Cz** | ≅ 98.6 % | > 99 % |

* Expectations

# TJ 180 nm

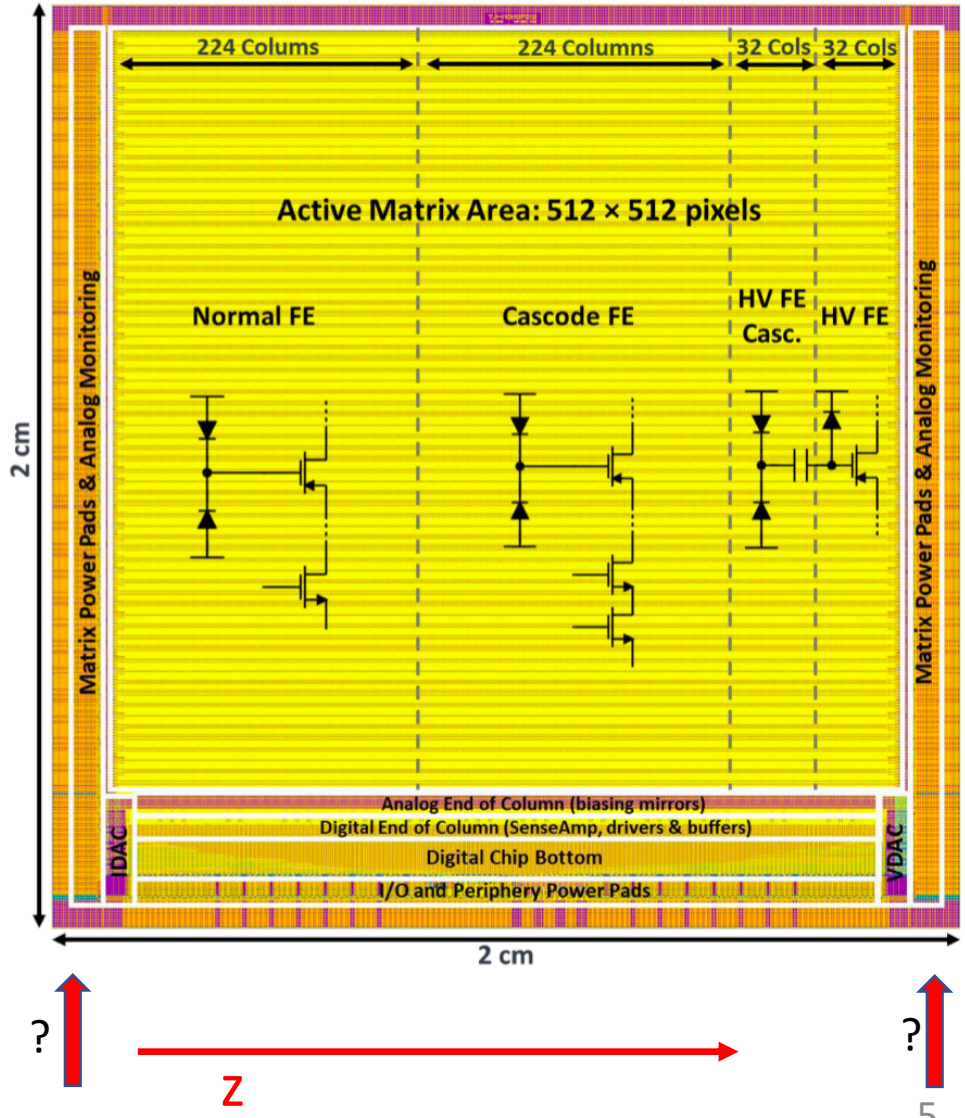
## ALPIDE




more details in backup slide

## Monopix(2)



# Assembly procedures for CHIPs HEAD-TO-HEAD in a Module/Ladder

**Table 3.2:** Dimensional requirements for the Pixel Chips.

| | Target value | Variation |
|---|---|---|
| Thickness | 50 µm | ±5 µm |
| Width | 15 mm | ±30 µm |
| Length | 30 mm | ±30 µm |

ALICE CUT–line & thickness requirements

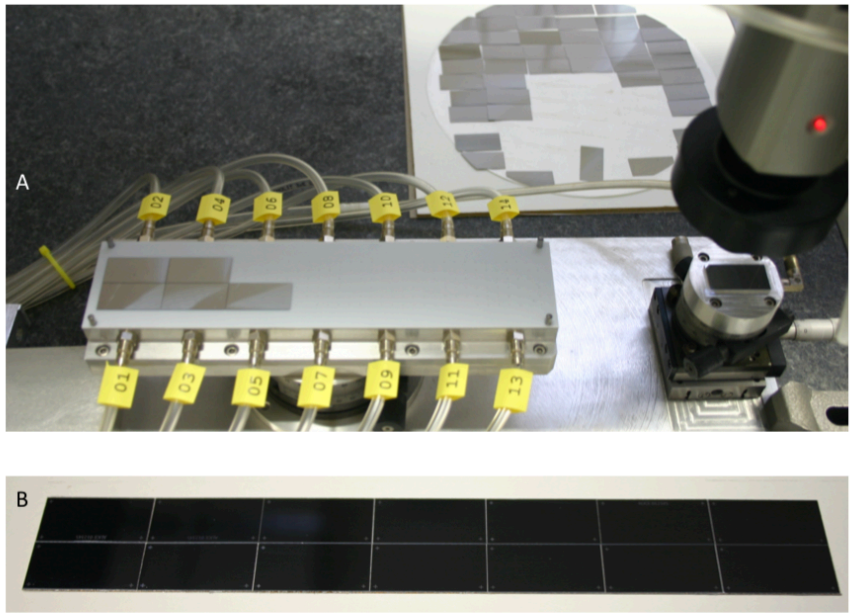



**Figure 4.24:** Development of the assembly procedure for the OB Module: A) the 14 chips are aligned one after the other in two rows of 7 chips each on a vacuum jig, before they are connected to the FPC and then glued to the Module Carbon Plate; B) first assemblies of dummy Module prototypes.

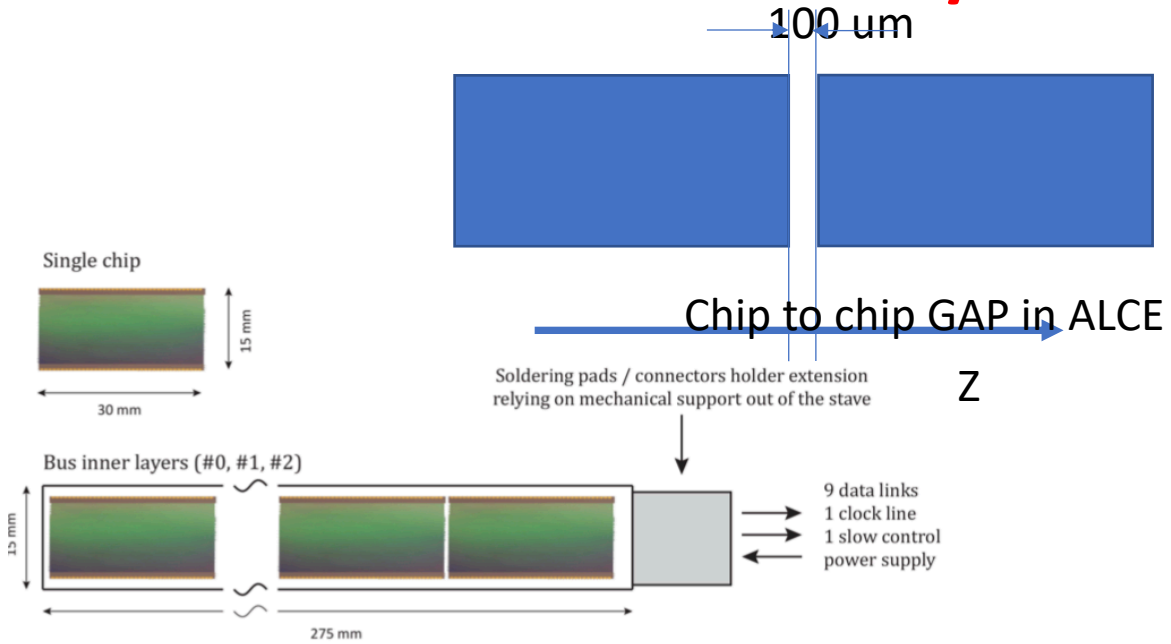



**Figure 6.7:** Connections for an Inner Layer Stave.

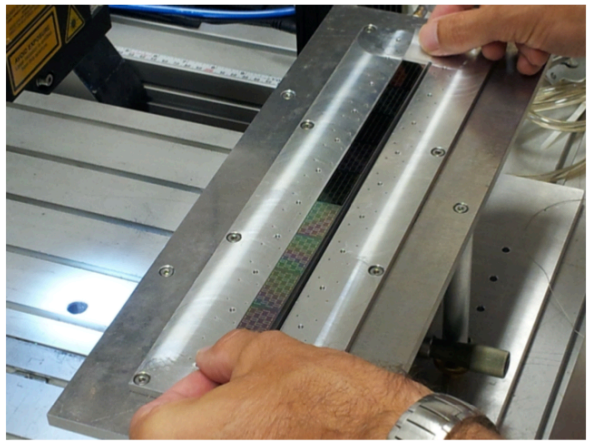


**Figure 4.22:** Placement of nine chips on the vacuum table A.

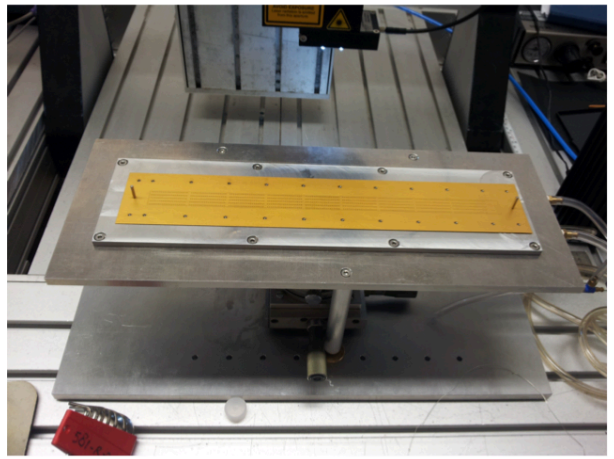
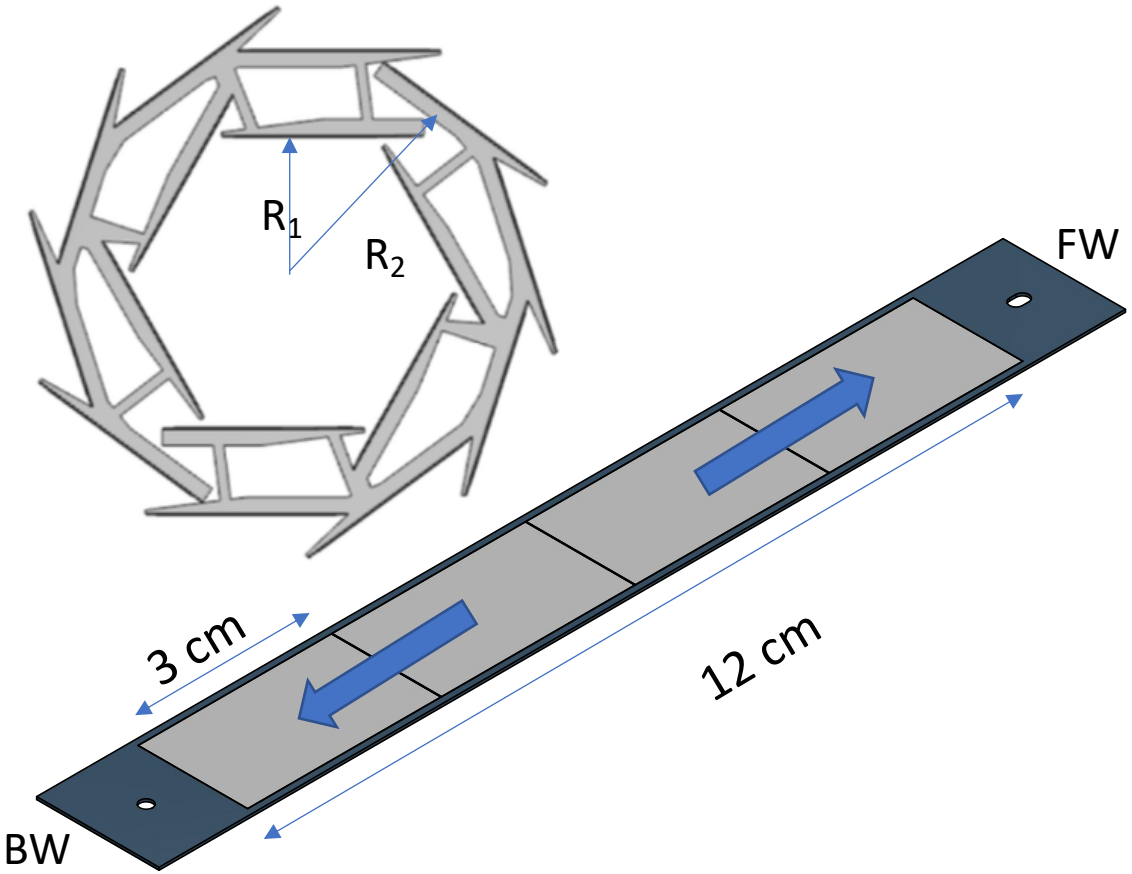


**Figure 4.23:** Placement of FPC on top of a row of nine chips.

# R&D on iVTX ladder: all-silicon-ladder concept

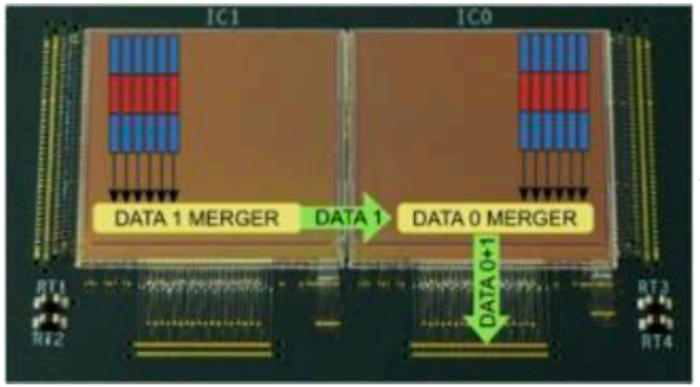
A single piece of silicon, with a slightly thicker silicon frame and a 40 μm-thin central region:

- L1 and L2 modules identical, placed at $R_1$=1.4 cm and $R_2$=2.2 cm
- 500 um active-area overlap
- Material budget: 0.1 % $X_0$/layer
- Cooling: forced air flow ($V_{air}$ ~ m/s ) for the acceptance region(to be simulated/experimentally demostrated!).




To reach the low-material-target: flex-less module.

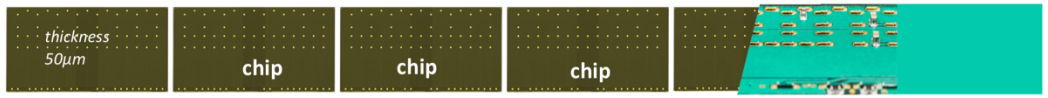
$L_{active}$ and $W_{active}$ o(3 cm) NEEDED!




2 MALTA sensors (TJ-180nm) wire-bonded together

doi-org.in2p3.bib.cnrs.fr/10.1016/j.nima.2020.164895

# oVTX spec's (I)




- oVTX: L3 and L4
  - Material budget: 0.3 % $X_0$ /layer
  - Staves «a la Alice» IB: →
    R=3.9/9.0 Length=20/45 cm
  - Barrel shaped
  - Water cooled sensors
  - Operation at room temperature
  - Specific power consumption:
    ~ 200 mW/cm$^2$

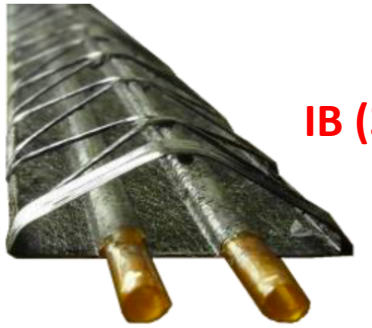
ALICE ITS TDR:

**Figure 4.2:** Prototypes of the Inner Barrel Stave.

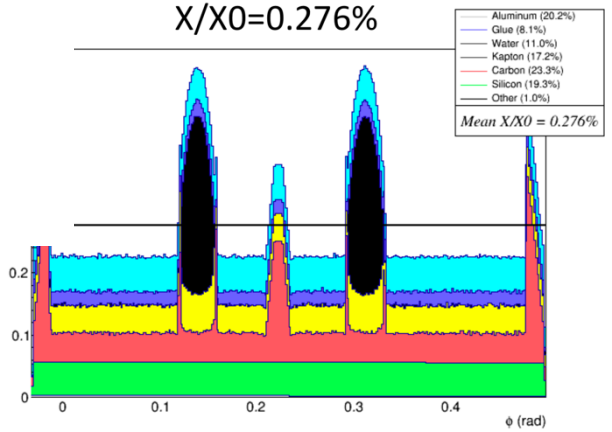
**Table 4.1:** Estimated contributions of the Inner Layer Stave to the material budget.

| Stave element | Component | Material | Thickness (µm) | $X_0$ (cm) | $X_0$ (%) |
|---|---|---|---|---|---|
| **HIC** | FPC Metal layers | Aluminium | 50 | 8.896 | 0.056 |
| | FPC Insulating layers | Polyimide | 100 | 28.41 | 0.035 |
| | Pixel Chip | Silicon | 50 | 9.369 | 0.053 |
| **Cold Plate** | | Carbon fleece | 40 | 106.80 | 0.004 |
| | | Carbon paper | 30 | 26.56 | 0.011 |
| | Cooling tube wall | Polyimide | 25 | 28.41 | 0.003 |
| | Cooling fluid | Water | | 35.76 | 0.032 |
| | Carbon plate | Carbon fibre | 70 | 26.08 | 0.027 |
| | Glue | Eccobond 45 | 100 | 44.37 | 0.023 |
| **Space Frame** | | Carbon rowing | | | 0.018 |
| **Total** | | | | | **0.262** |

$X_0$



IB (30 cm)← ALICE




Single stave,
for perpendicular tracks

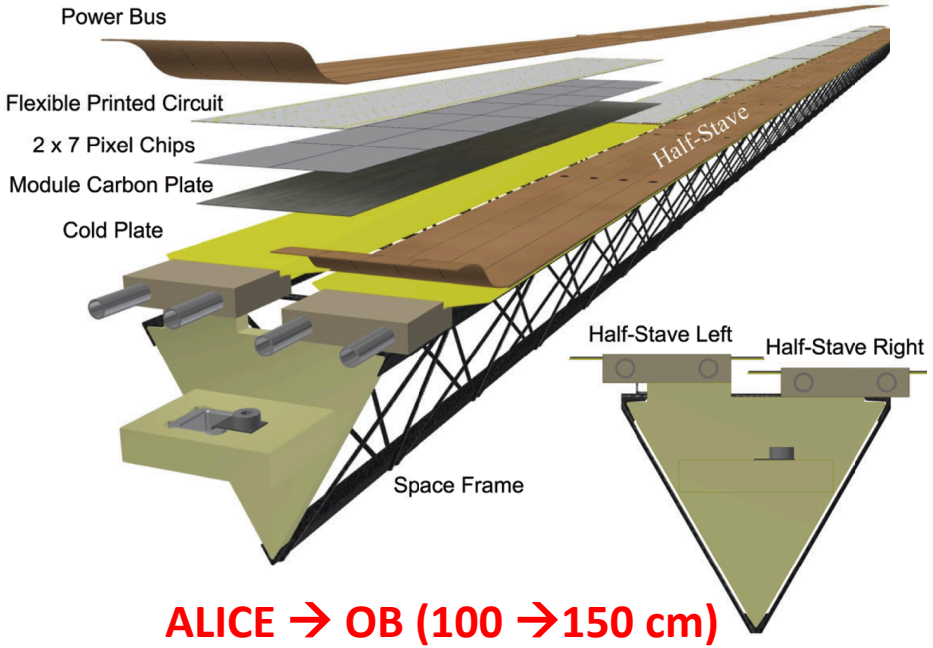
# oVTX spec's (II)

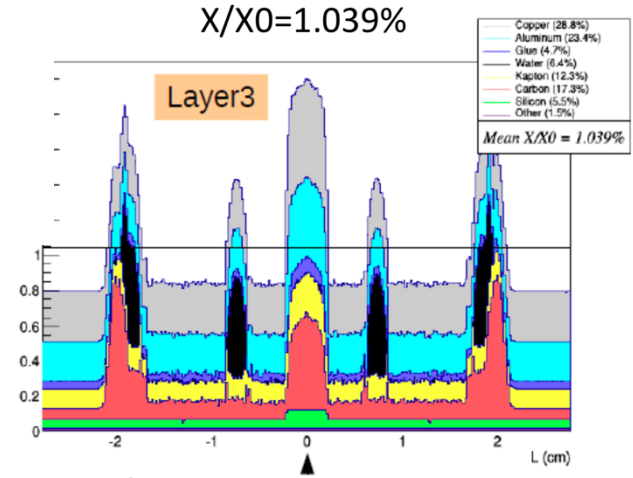
ALICE ITS TDR:


- oVTX: L5
  - Material budget: 0.3-0.5 % $X_0$ /layer
  - Staves «a la Alice» OB: →
    R = 14 cm Length = 70 cm
  - Water cooled sensors
  - Operation at room temperature
  - Specific power consumption:
  ~ 200 mW/cm$^2$
  - Power BUS needed?

**Table 4.2:** Estimated contributions of the Outer Layer Stave to the material budget.

| Stave element | Component | Material | Thickness (µm) | $X_0$ (cm) | $X_0$ (%) |
|---|---|---|---|---|---|
| **Module** | FPC Metal layers | Aluminium | 50 | 8.896 | 0.056 |
| | FPC Insulating layers | Polyimide | 100 | 28.41 | 0.035 |
| | Module plate | Carbon fibre | 120 | 26.08 | 0.046 |
| | Pixel Chip | Silicon | 50 | 9.369 | 0.053 |
| | Glue | Eccobond 45 | 100 | 44.37 | 0.023 |
| **Power Bus** | Metal layers | Aluminium | 200 | 8.896 | 0.225 |
| | Insulating layers | Polyimide | 200 | 28.41 | 0.070 |
| | Glue | Eccobond 45 | 100 | 44.37 | 0.023 |
| **Cold Plate** | | Carbon fleece | 40 | 106.80 | 0.004 |
| | | Carbon paper | 30 | 26.56 | 0.011 |
| | Cooling tube wall | Polyimide | 64 | 28.41 | 0.013 |
| | Cooling fluid | Water | | 35.76 | 0.105 |
| | Carbon plate | Carbon fibre | 120 | 26.08 | 0.046 |
| | Glue | Eccobond 45 | 100 | 44.37 | 0.023 |
| **Space Frame** | | Carbon rowing | | | 0.080 |
| **Total** | | | | | **0.813** |




Single stave,
for perpendicular tracks

**ALICE → OB (100 →150 cm)**

# Input/output pads

(redundancy to be taken into account to cope with chip-failures)

- Power:
  - HV +/- (depletion)
  - LV +/-
  - GND (ref -)
- CMDs: 1 diff. pair?
- CLK: 1 diff. pair?
- Data: 1 diff. pair?
- TRG(?): triggered arch. ?

After Including all the “features”:

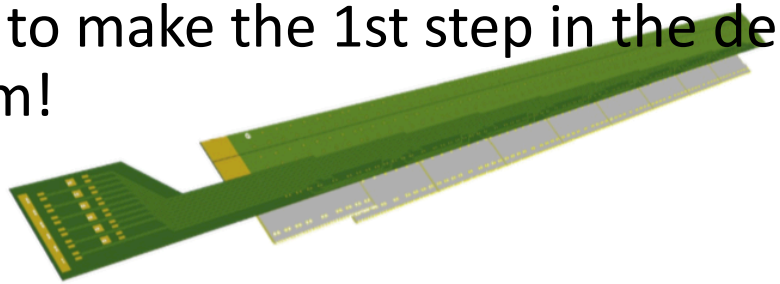
$P_{specific}$ =? (< 200 mW/cm$^2$)

Is serialisation of the powering needed?

# FLEX CIRCUITS DESIGN

- FLEX introduces a great amount of material

  (% $X_0$ ~ comparable to the support structure!)
- For L1&2 (short) modules smart solution under investigation (flex-less)
- For L3→5 ladders, large number of chips need to be connected and power to be distributed to them: FLEX is mandatory!
- Chip/flex connections: u-bonding.
- Need to make the 1st step in the design of the DAT system!



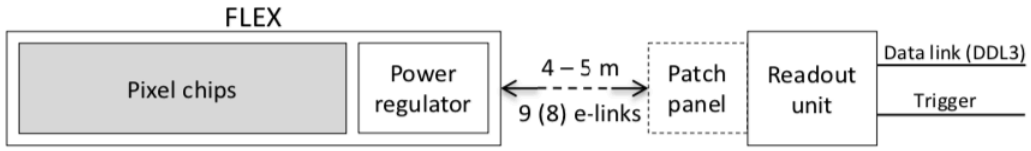
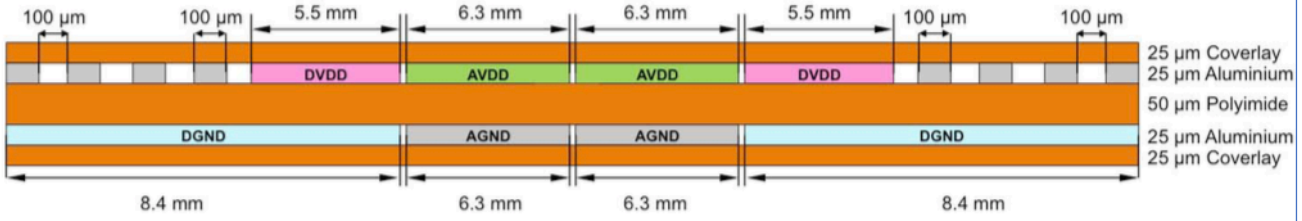



**Figure 6.1:** Schematic representation of the read-out path. The number of e-links per Stave is nine for Inner Layers and eight for Middle and Outer Layers.

# ALICE (Al) FLEX CIRCUIT

## (parallel powering)

OB:



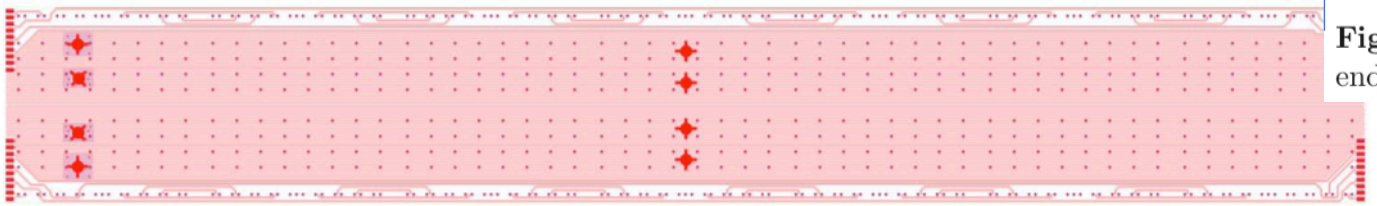
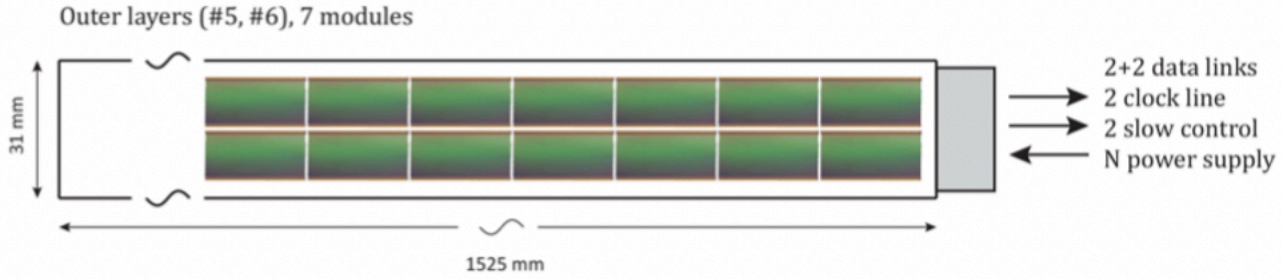
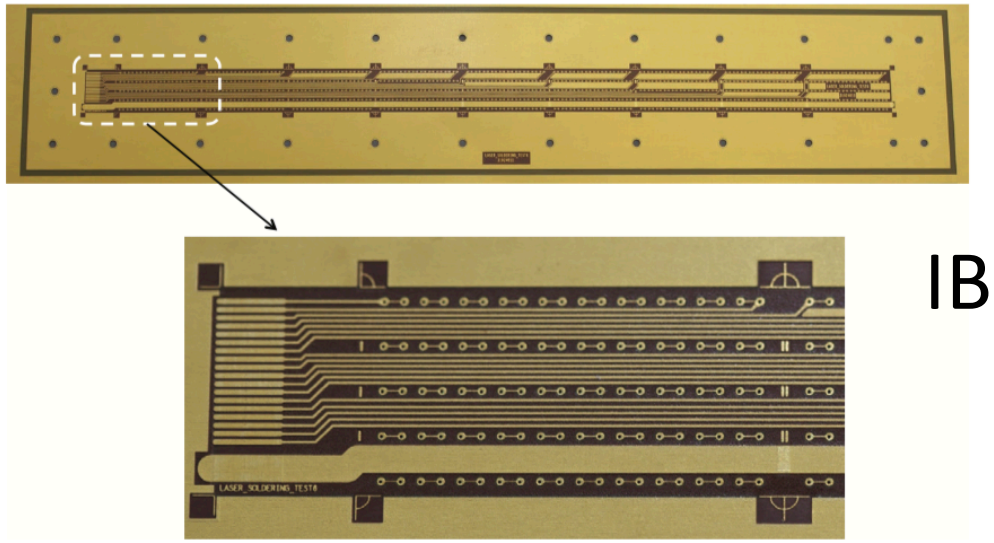



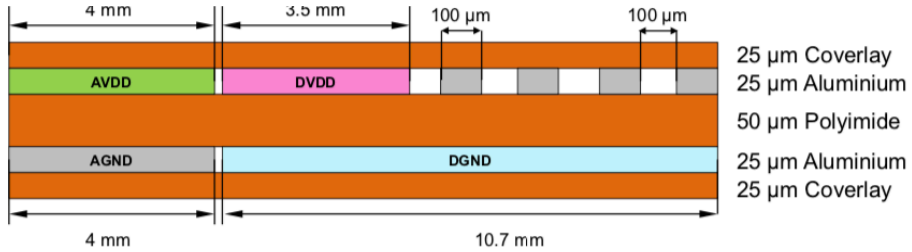
**Figure 4.15:** Schematic view of the cross-section (top) and layout (bottom) of the FPC for the OB Stave. The soldering pads for the connection between adjacent FPCs are visibile at the two edges of the layout, the larger rounded pads allow the connections of the PB to the power and ground planes. A differential pair line for data readout that allows to by-pass a Module is also visible at each side edge of the layout.



IB

**Figure 4.14:** Cu prototype of the FPC for the IB Stave (top) and a close up view of the end-of-Stave section (bottom).



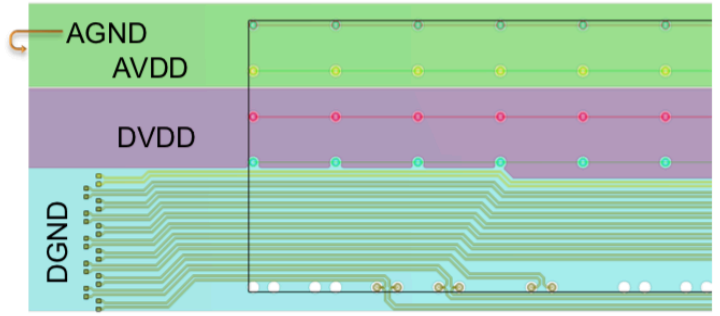
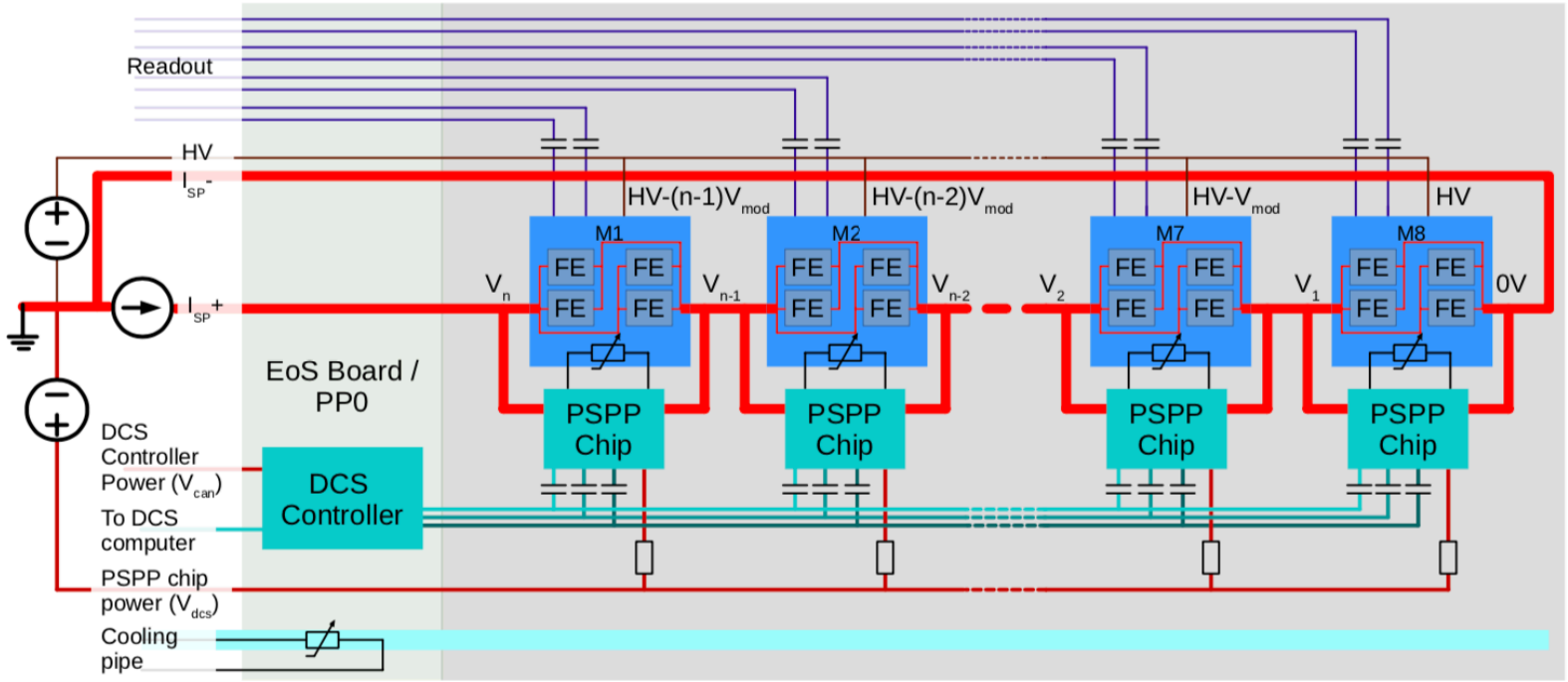




**Figure 4.13:** Schematic view of the stack-up (top) and layout (bottom) of the FPC for the IB Stave.

# ATLAS-ITK approach

(CMOS) Drop-in module concept – able to replace hybrid-pixel in terms of the ATLAS TDAQ scheme (interfaced with data aggregator), regulators for (serial) Power, and mechanical compatibility.

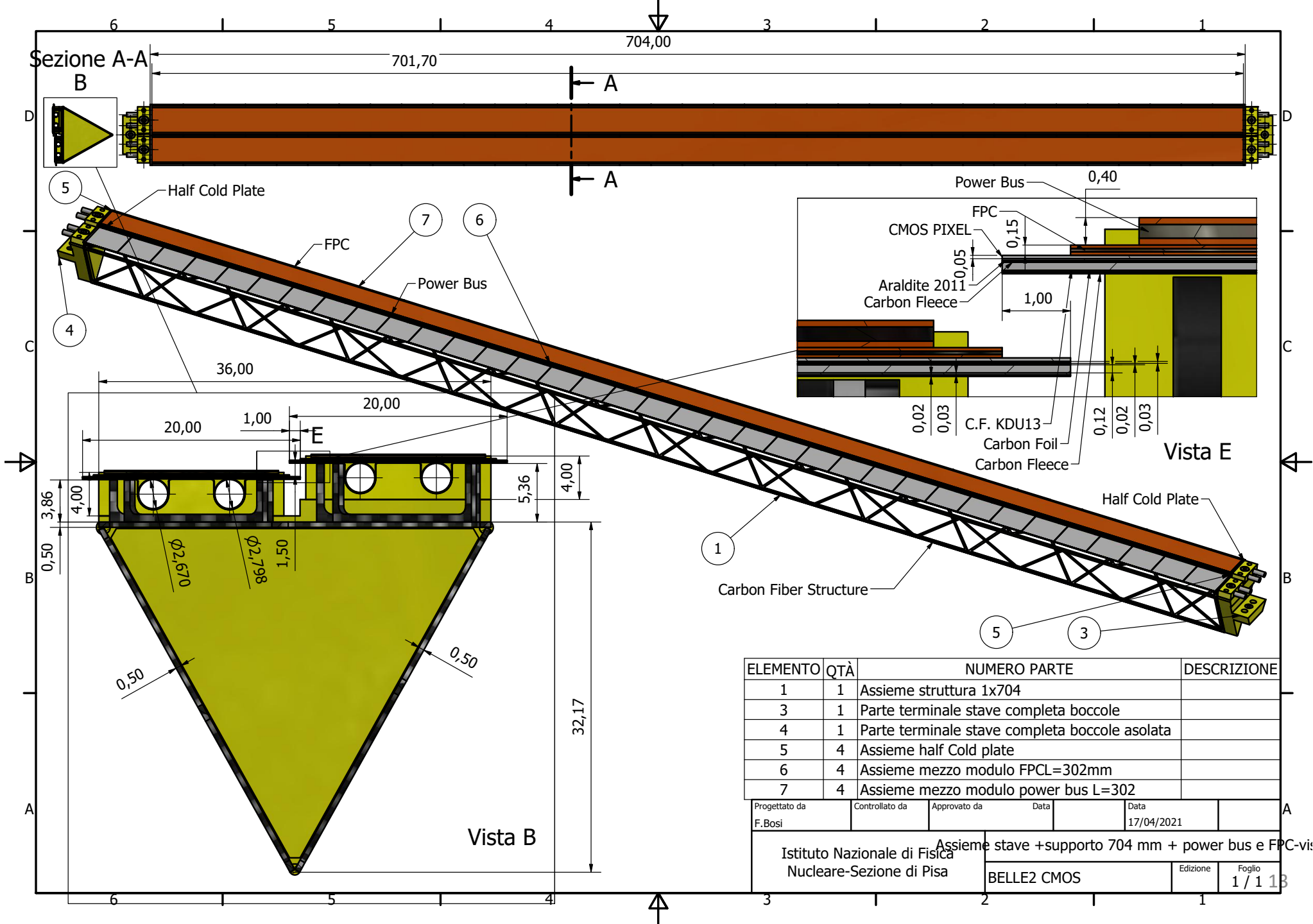



From ATLAS ITK TDR

Figure 11.1: Schematic of the Serial Powering distribution on the local support.

# Current Design of the L5-ladder Prototype:

(1st layout exercise with 2cm x 2cm chip, a-la“monopix”)




| ELEMENTO | QTÀ | NUMERO PARTE | DESCRIZIONE |
|---|---|---|---|
| 1 | 1 | Assieme struttura 1x704 | |
| 3 | 1 | Parte terminale stave completa boccole | |
| 4 | 1 | Parte terminale stave completa boccole asolata | |
| 5 | 4 | Assieme half Cold plate | |
| 6 | 4 | Assieme mezzo modulo FPCL=302mm | |
| 7 | 4 | Assieme mezzo modulo power bus L=302 | |

| Progettato da | Controllato da | Approvato da | Data | Data | |
|---|---|---|---|---|---|
| F.Bosi | | | | 17/04/2021 | |

Istituto Nazionale di Fisica Nucleare-Sezione di Pisa

Assieme stave +supporto 704 mm + power bus e FPC-vis

BELLE2 CMOS

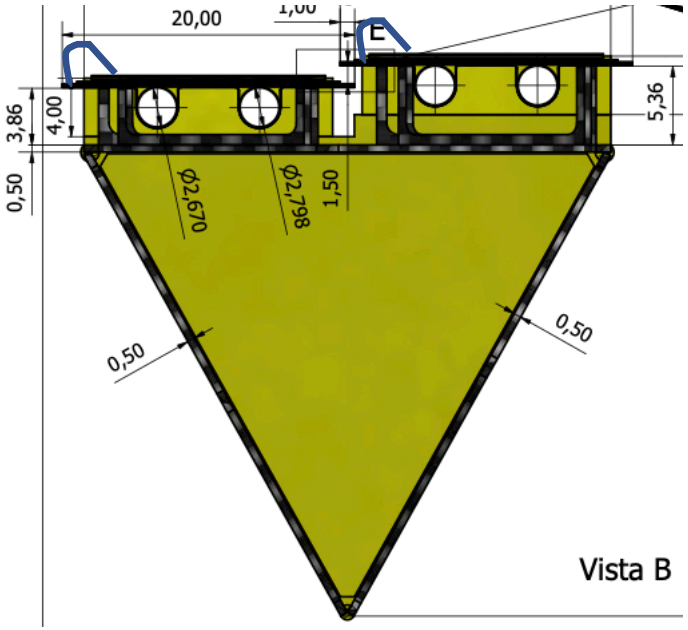
Edizione

Foglio 1 / 1

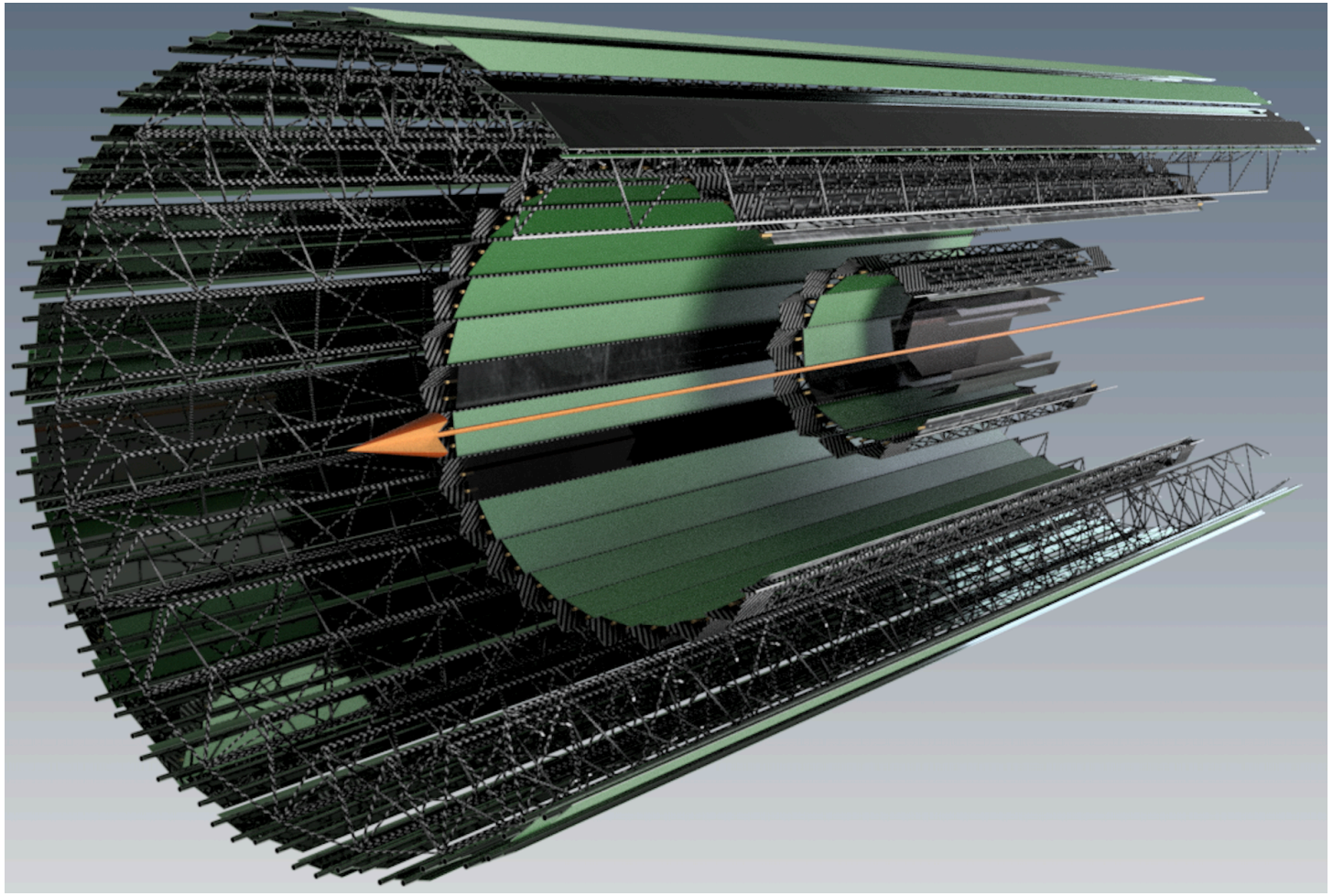
# Mechanics is dressing the chip!

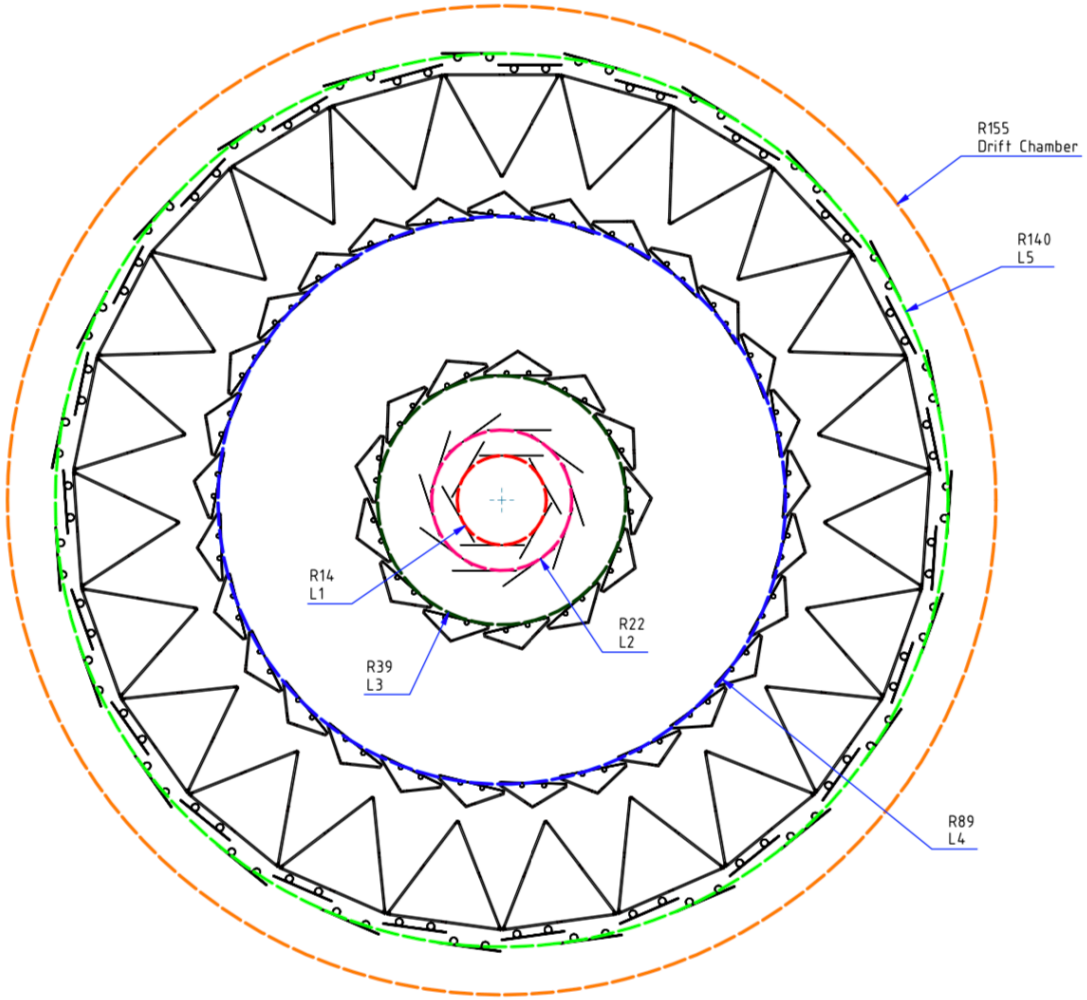
Chip dimensions affects all the mechanical design:

- The functionality of the L1&2 module suggests the chip dimensions.
- We want to refurbish all the VTX with 1! Chip:  then the L3,4 &5 staves are composed/constrained by half-ladders of (chip) width.
- Overlaps between adiacent modules, inside each stave and between adiacent staves must cope with dead-regions ($W_{periphery}$)
- u-bond connections chip/flex are driven by pad location in the dead region of the chip.



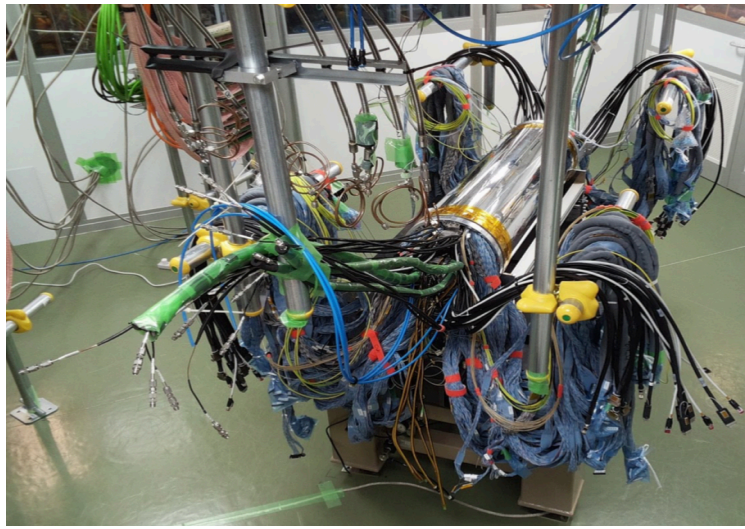
# 5-layer VTX Conceptual Design





# Remind: the Overall Concept on Connections

- Key-point: reduce ALARA (As Low As Reasonable Achievable!) the amount of services (cables/cooling) to be provided to VTX
- Fast readout (25 ns)/ small pixels, translate in tiny occupancy-> low data rates.
- Warm operation: no isolated lines.
- Possible to reduce cables and connections down to 1/10 of the current VXD (PXD+SVD).



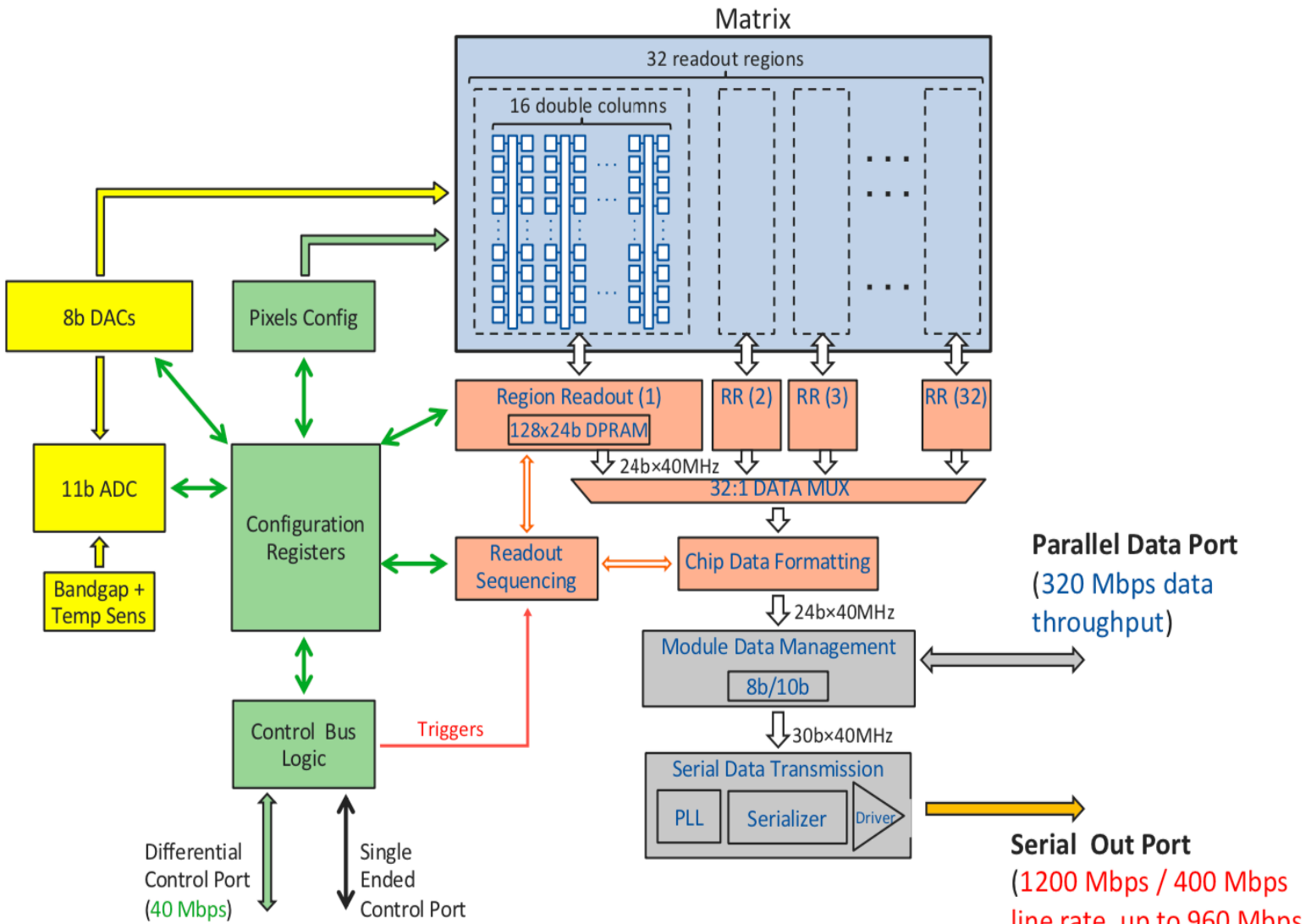
The reduction of services would imply several advantages:

- Simpler integration. Fast exchange if needed;
- Additional room for shielding;
- Less cables in front of the endcaps.

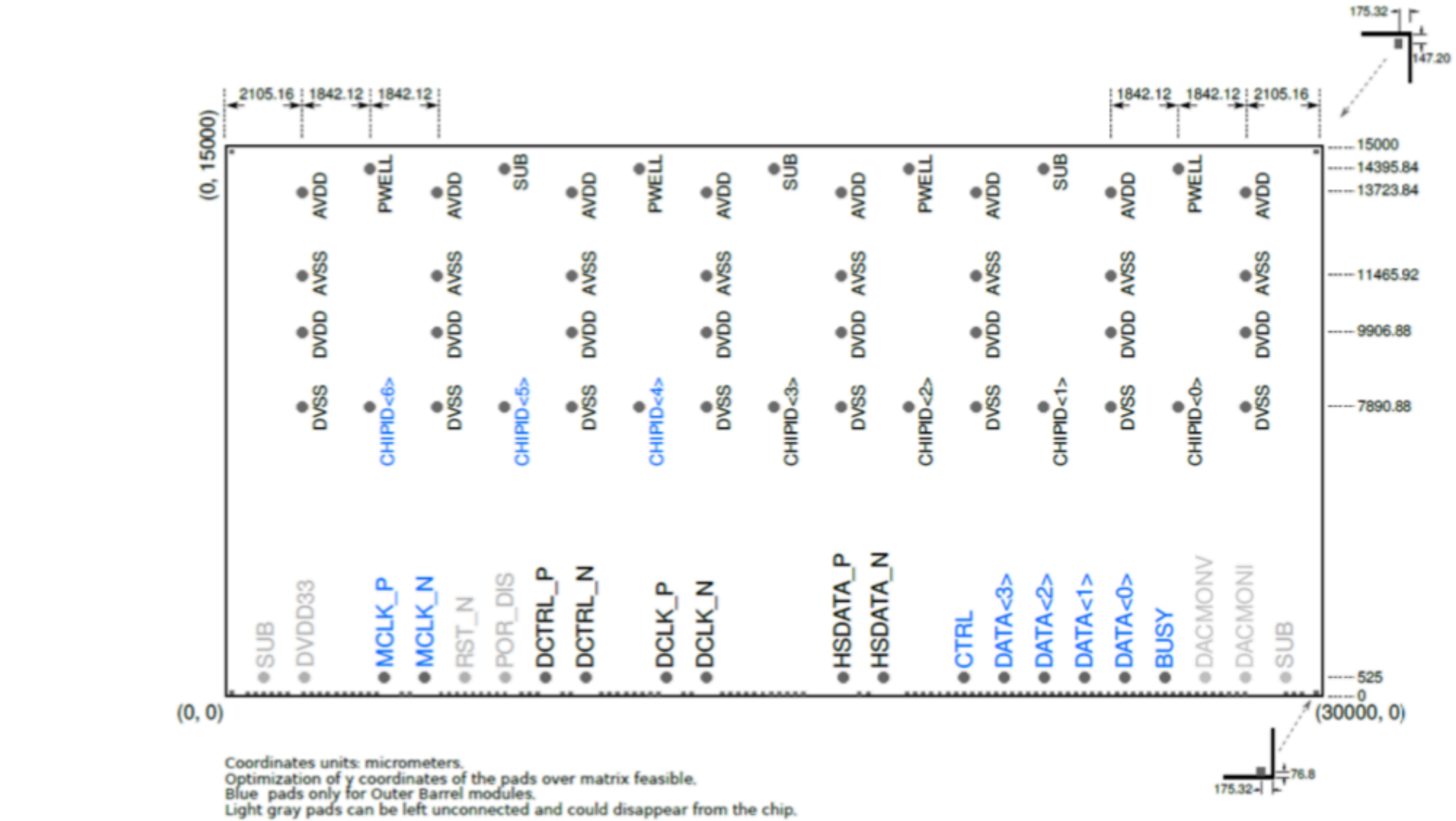
# Backup slides

From the 1st CERN Workshop

# ALPIDE Block Diagram



# ALPIDE Pinout




Coordinates units: micrometers.
Optimization of y coordinates of the pads over matrix feasible.
Blue pads only for Outer Barrel modules.
Light gray pads can be left unconnected and could disappear from the chip.