VTX Design

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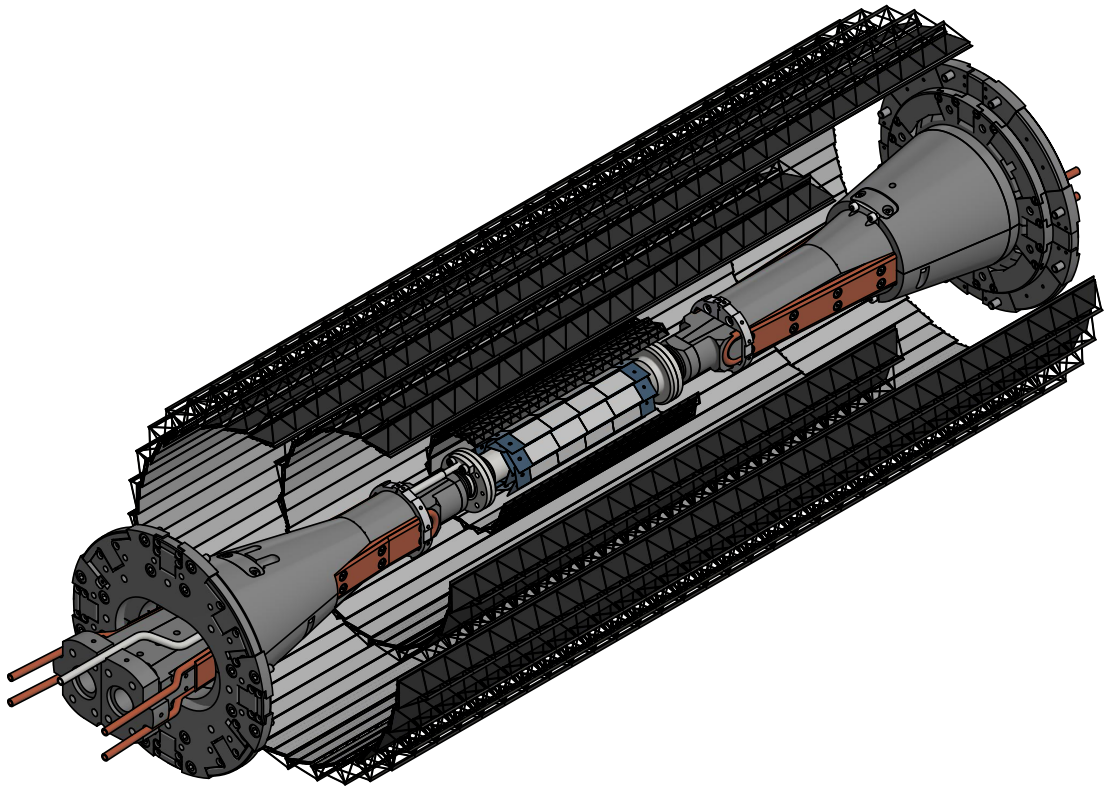
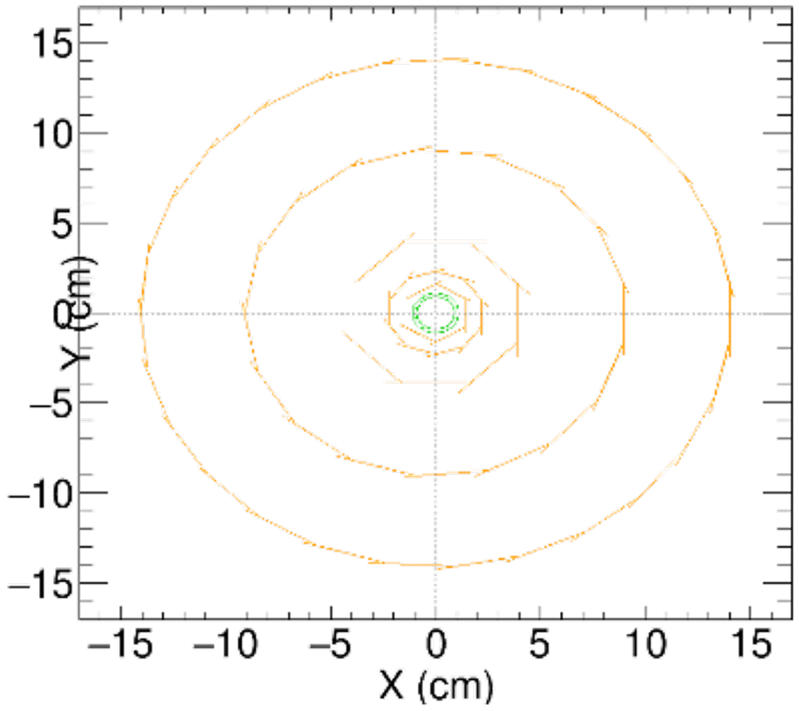
VTX General Concept





The VTX proposal is based on a 5 straight layers filling the volume of the VXD and keeping the current machine-detector boundary conditions

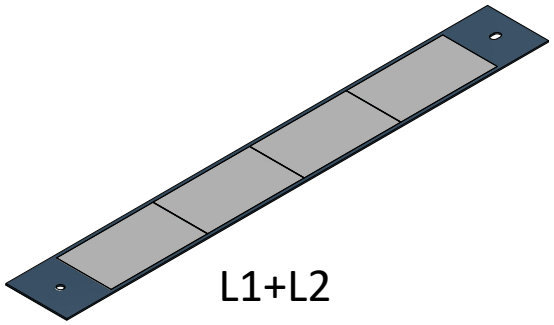
There might be other considerations or constraints, but not so important at this stage

VTX General Ideas

- Low material (~ 50 µm thin sensors) : 0.1% X_0 (L1+L2) - 0.3% (L3) - 0.8% X_0 (L4+L5)
- Moderate pixel pitch ~ 40 µm^2
- Fast integration time 25-100 ns
- Put effort on operation simplicity and reduced services

→ Same chip for all layers, but different integration between inner (L1+L2) (This talk) and outer (L3, L4+L5) (Next talk)

VTX General Ideas

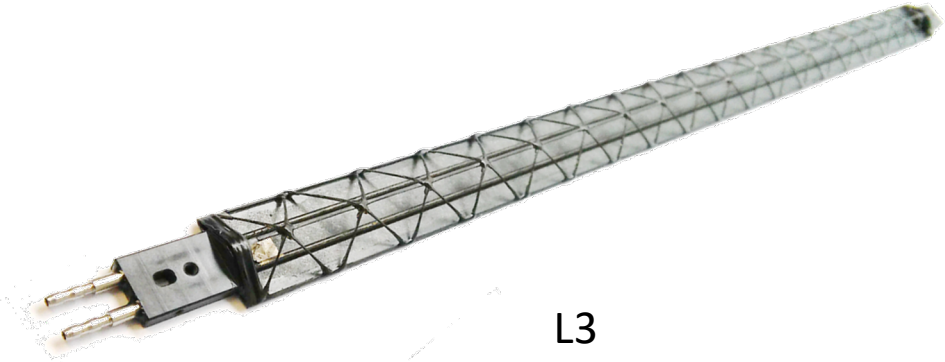


L1+L2

Chips are the same but the ladder/stave concept is different depending on the layer number (L1 is 12 cm long, L5 is 65 cm long)

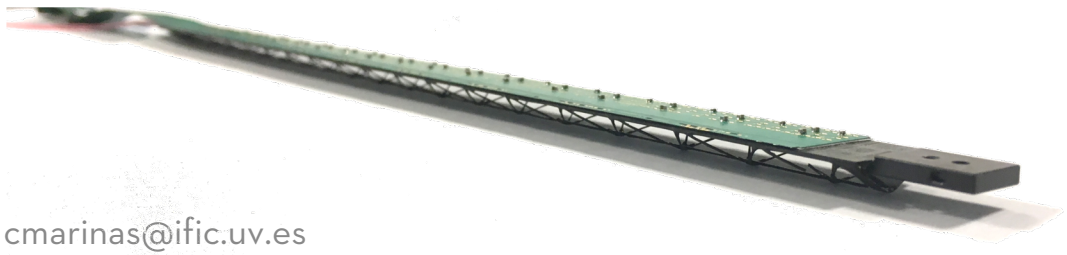
L1+L2: All silicon ladders. Sensors + RDL. Air cooling. Services out of the acceptance

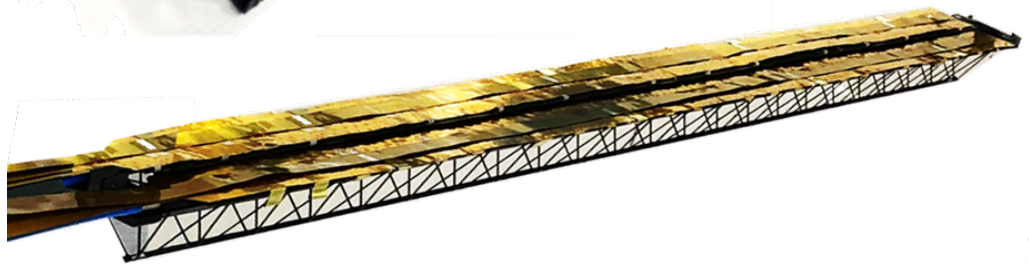
L3-L5: Support frame, cold plate, sensors, flex, power bus. Water cooling.



L3

L4+L5





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iVTX Ladder Design Considerations

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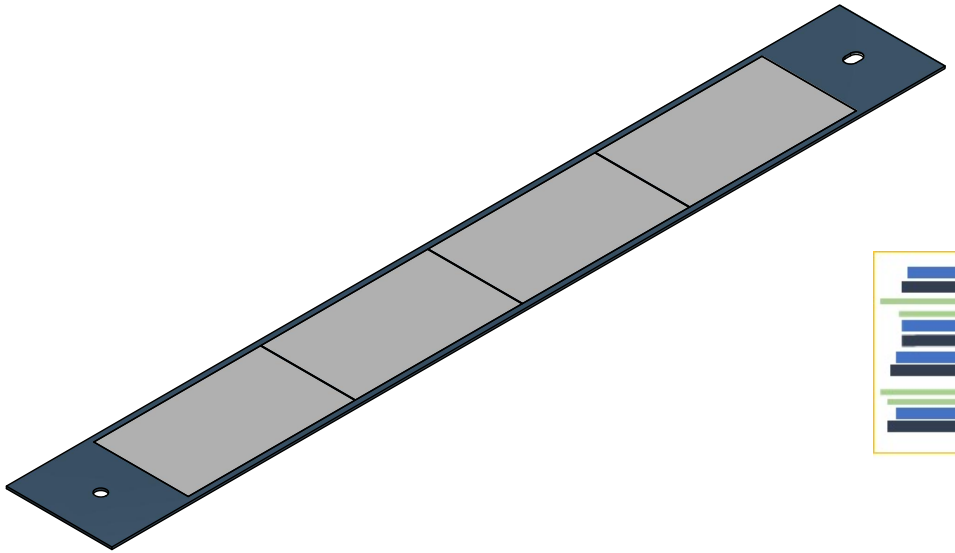
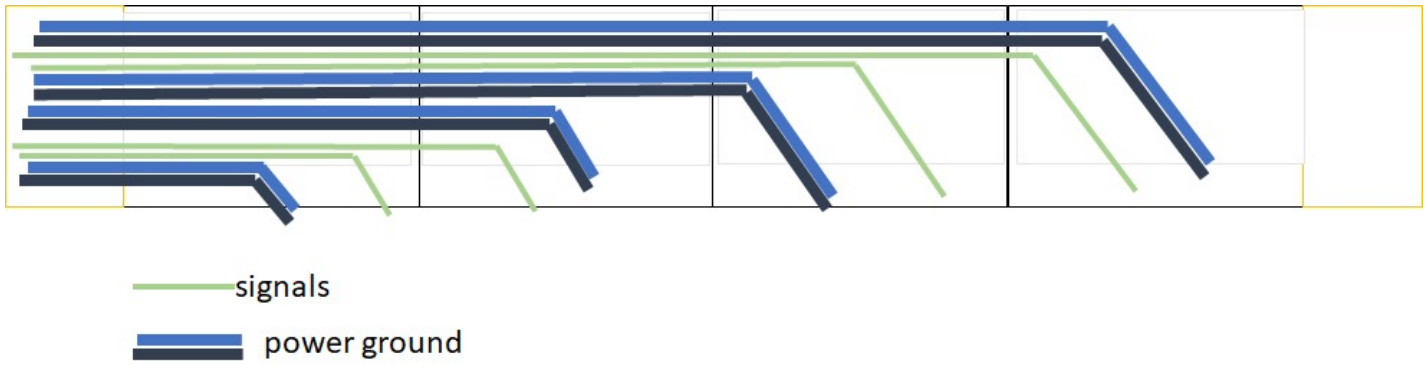
Signal and Power Distribution

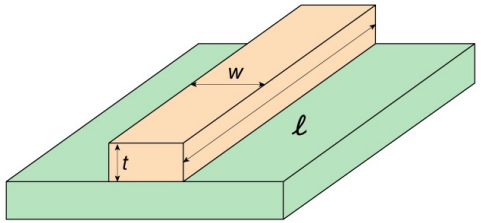




For the inner layers, it would be desirable to have services from one side (BWD) only.
Space in FWD is tight and some machine upgrade options consider moving QCS closer to the IP.

Connections are done at the bottom of the chip with vias between the chip and the RDL

Power Distribution



Q: Characteristics on the RDL to minimize material budget while keeping manageable voltage drop (let say 10%)?

Basic assumptions:

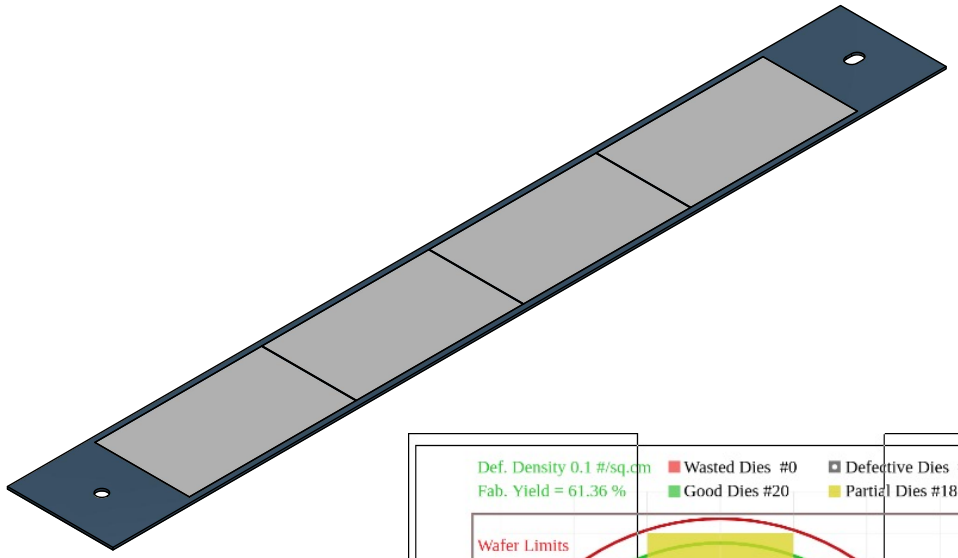
P = 200 mW/cm^2
V = 2 V
I = 0.55 A
Ladder length = 12 cm
ρ_{Cu}=1.68x10^{-8} Ohm·m (at 20 degC)
ρ_{Al}=2.65x10^{-8} Ohm·m (at 20 degC)

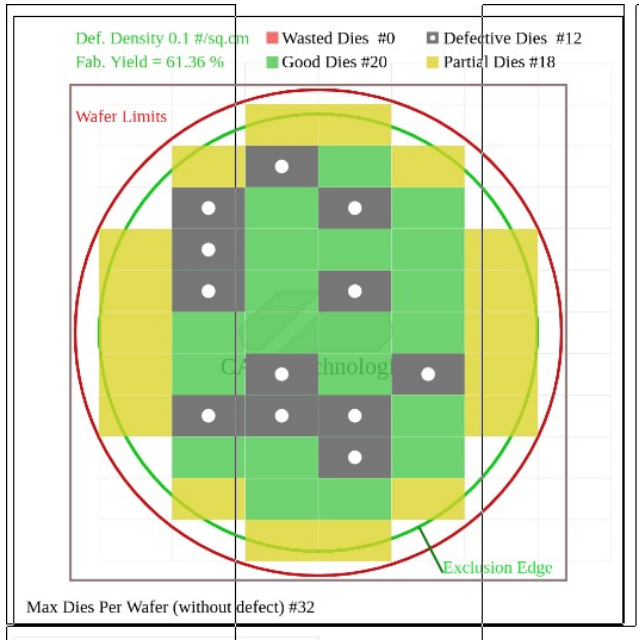
Cu Thickness (Al Thickness)	Cu Width (Al Width)
5 um (5 um)	1,1 mm (1,7 mm)
4 um (4 um)	1,3 mm (2,2 mm)
3 um (3 um)	1,8 mm (2,9 mm)
2 um (2 um)	2,7 mm (4,3 mm)
1 um (1 um)	5,6 mm (8,7 mm)

As a result, the additional burnt power is ~100 mW/chip → total P = 220 mW/cm^2

Note: Neglecting temperature effects on resistivity. Other considerations not taken into account here (routing, coupling, fabrication, …)

Ladder Dimensions





To cover the acceptance at current PXD L2 position, the active area has to be 123 mm

If we go for 4 chips, this defines the length to be 30 mm each

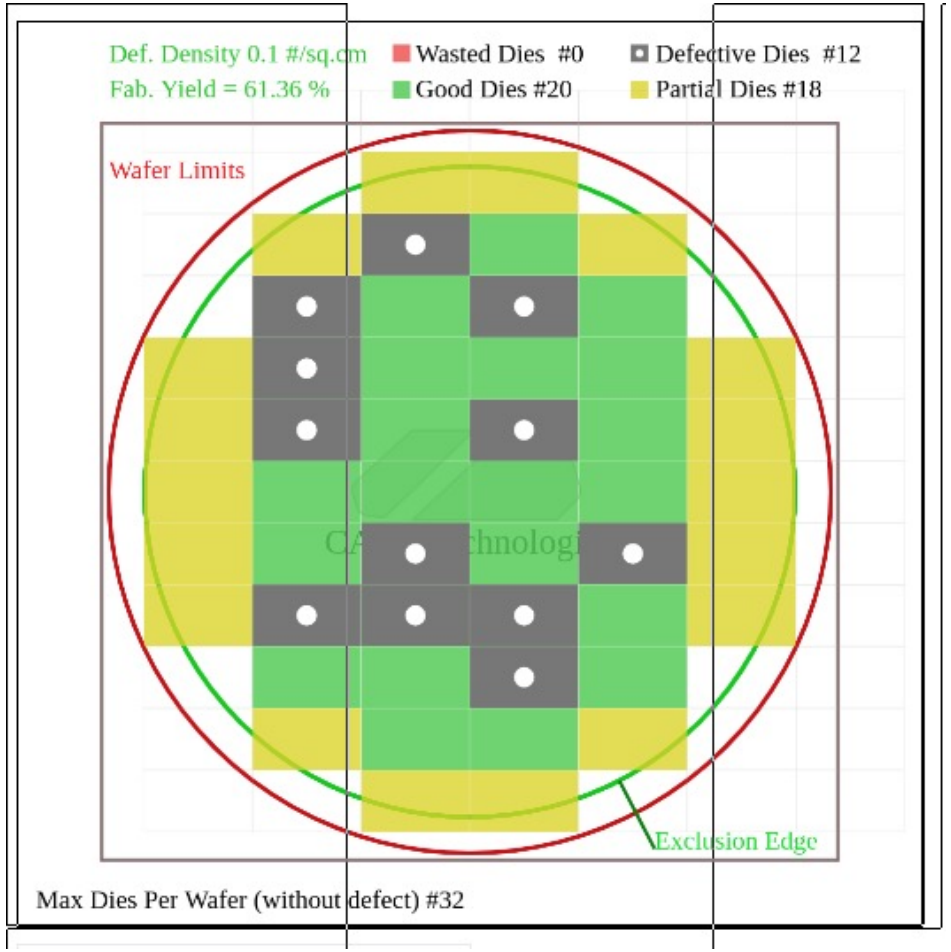
In the actual CAD model, chip width is set to be 20 mm…

But, what is the optimal dimension?

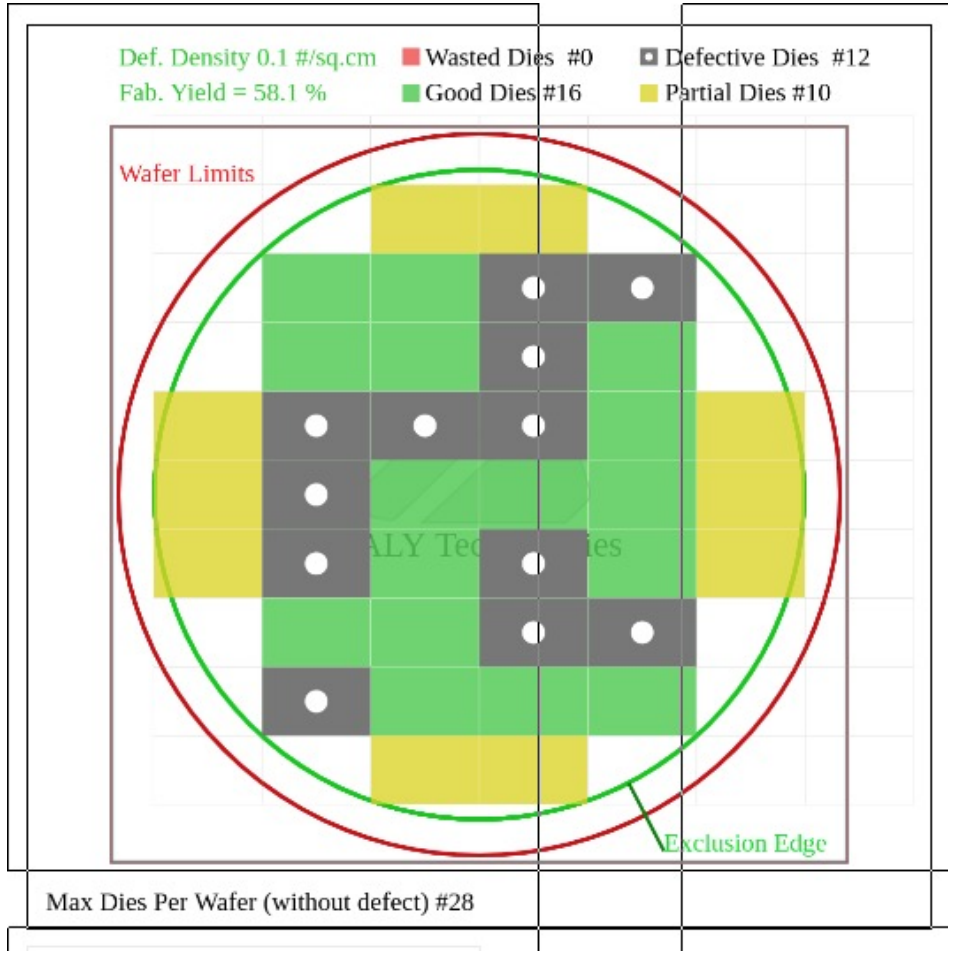
Yield, #ladders/wafer, … have to be taken into consideration…

Wafer Filling

17 mm wide



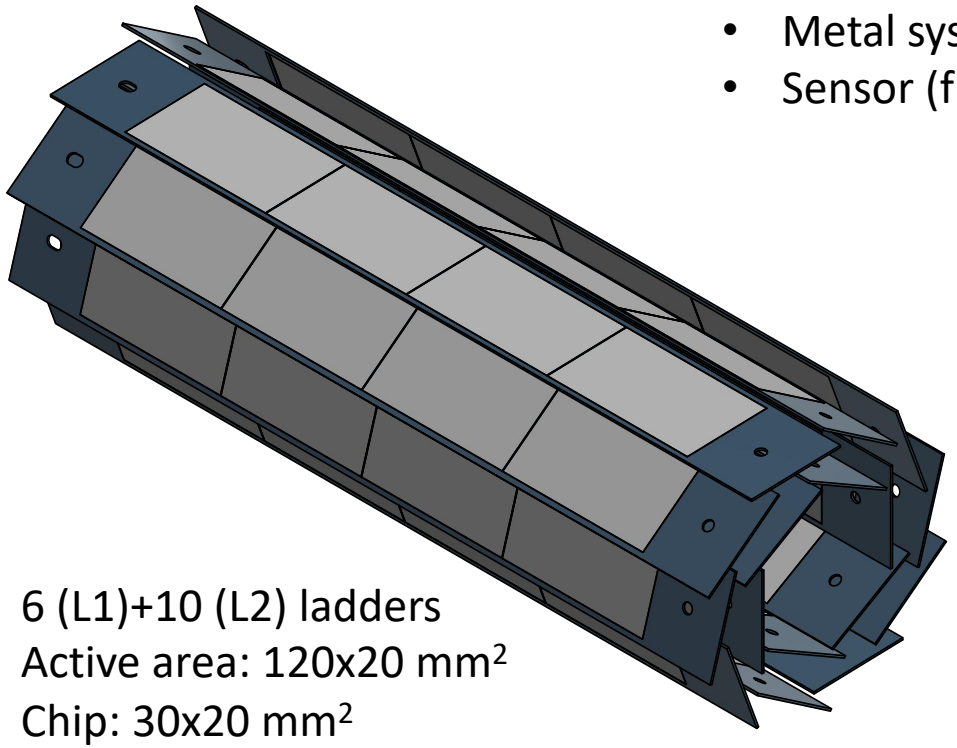
19 mm wide



Material Budget

Target for layers 1 and 2 was 0.1 % X_0… How realistic is this?

- Redistribution layer (only 37% of the area): 3 µm of Cu → 0.02 % X0
- Metal system (1 µm each, 6 metal layers): 6 µm of Al → 0.01 % X0
- Sensor (frame not included): 50 µm of Si → 0.05 % X0



6 (L1)+10 (L2) ladders
Active area: 120x20 mm^2
Chip: 30x20 mm^2

Ladder dimensions are needed to position overlaps and angles
→ This has an impact on material budget too

THANK YOU

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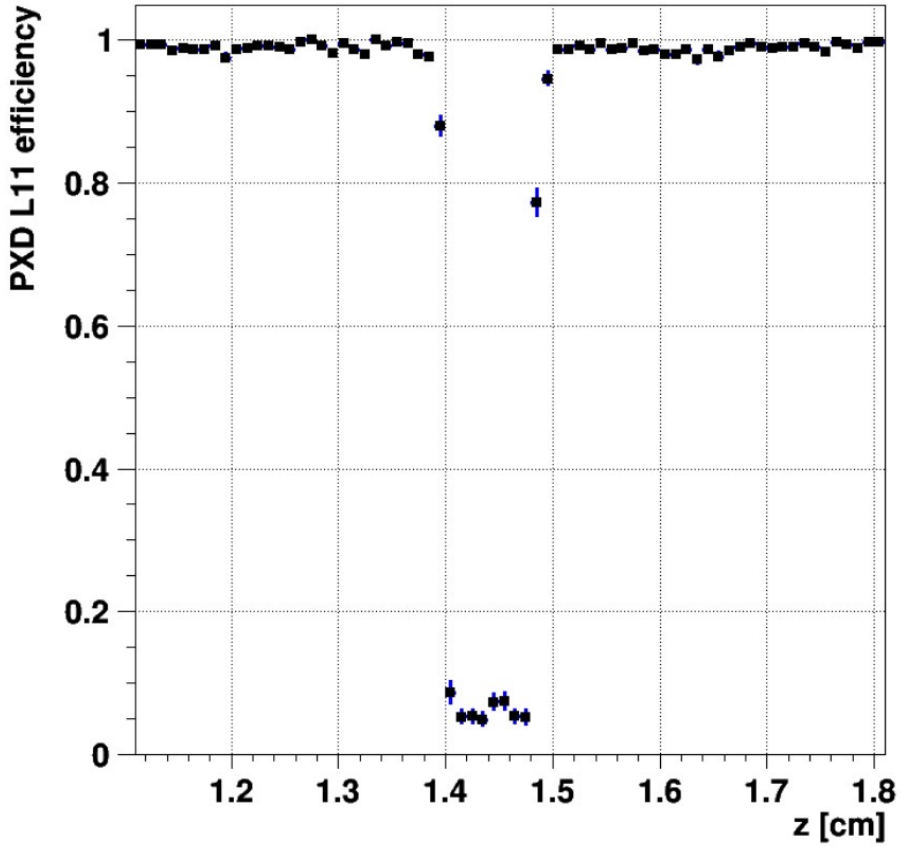
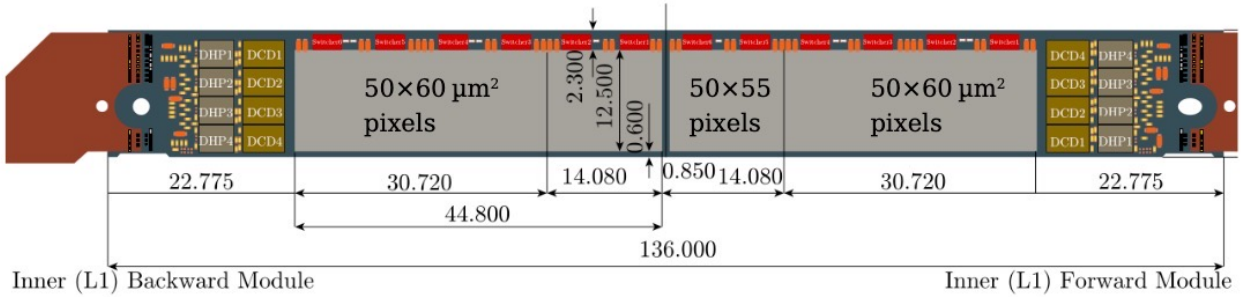
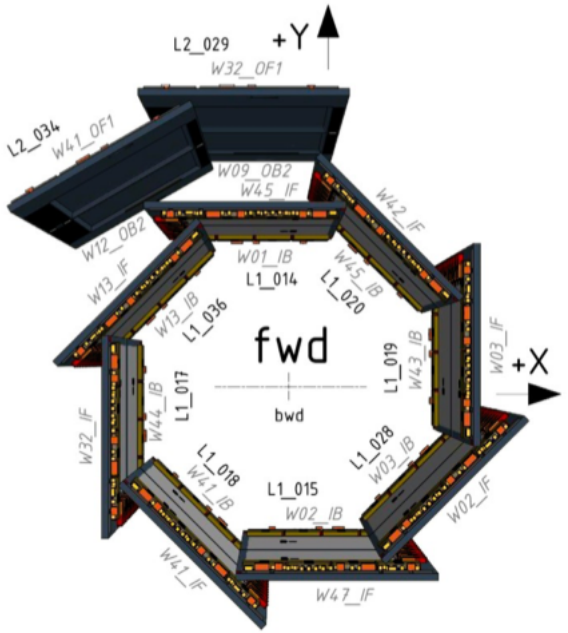
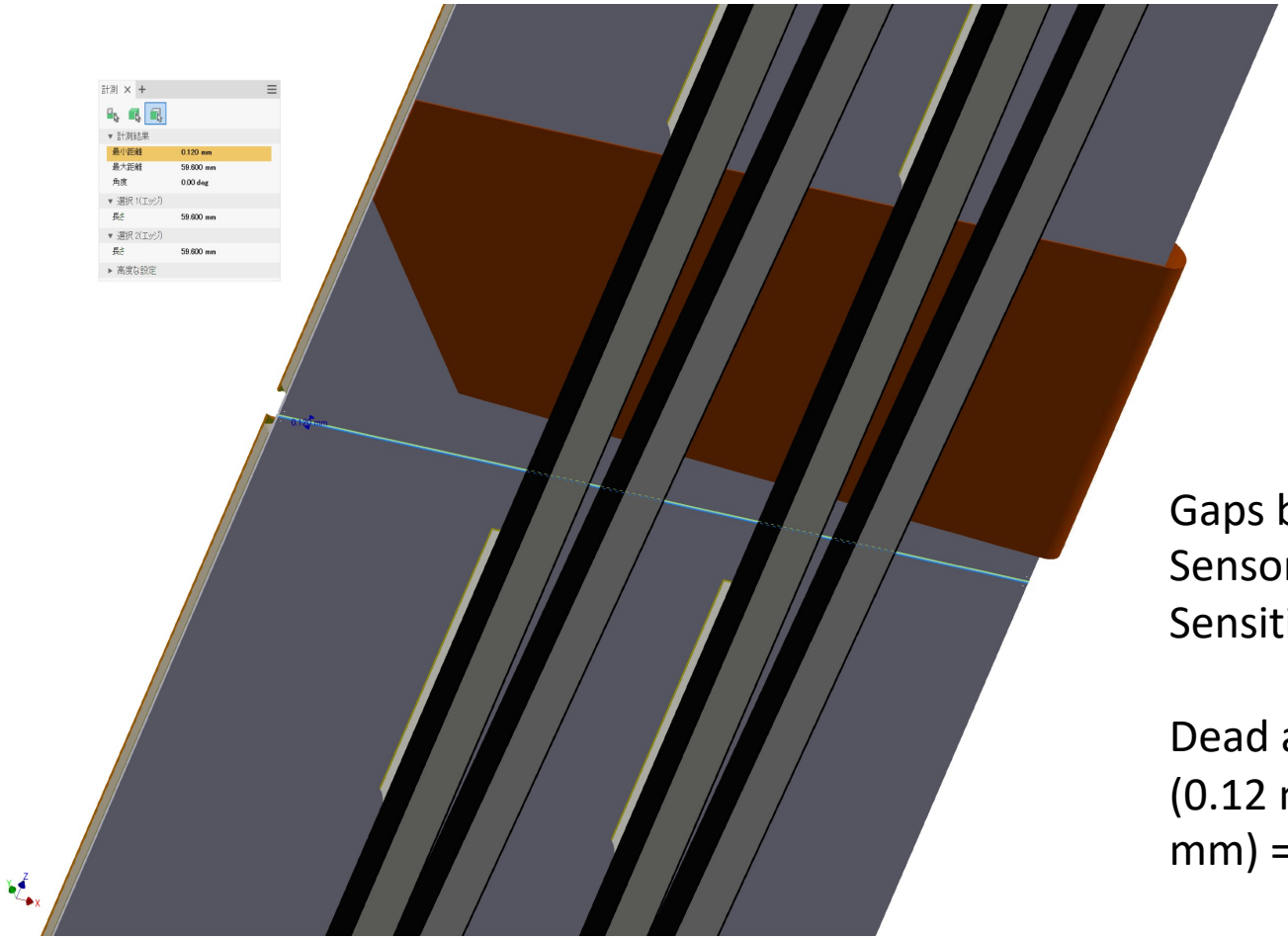
Current PXD Geometry







Current SVD Geometry



Gaps betweens sensors: 120 µm
Sensor length (z-direction): 124.88 mm
Sensitive area length (z-direction): 122.76 mm

Dead area per sensor:
(0.12 mm + (124.88 mm - 122.76 mm)) / (124.88 mm + 0.12 mm) = 1.792%