VTX Upgrade
L5 L4 L3 Flex Analysis

Massimo Minuti
INFN Pisa
massimo.minuti@pi.infn.it

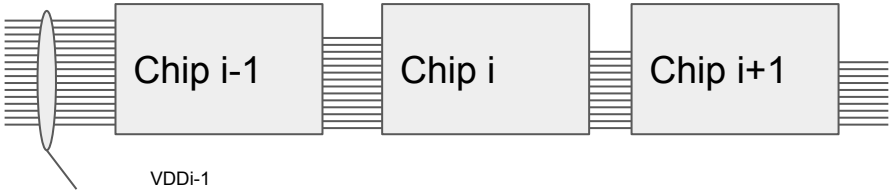
VTX Upgrade L3-L5 Flex Analysis

Power Bus

Chip Power = 200mW/cm^2 @ 3.0cm * 2.0cm
Power Supply Voltage = 2.0V
Max Voltage Drop (per line) = 100mV

Global Rail Power Bus

11 chips share the same VDD and GND lines. Overall Lines width is 2.0 cm (chip short edge).
Rlump = 0.003 Ohms Isum = 33 A maxdropV = 0.100V
Track L = 33.000 cm W= 1.000 cm T = 0.016 mm
0.118%X0 for Copper (L5)
0.053%X0 for Kapton
Pros:
Easy to design
Cons:
Voltage is not the same for every chip, i.e. there might be additional power losses due to extra-voltages at the LDO inputs;

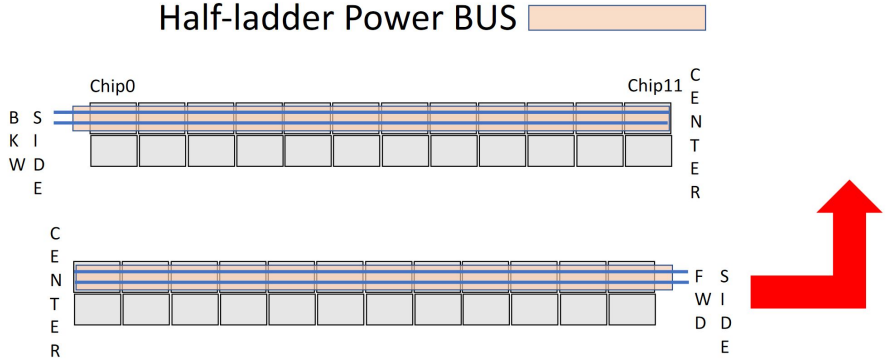


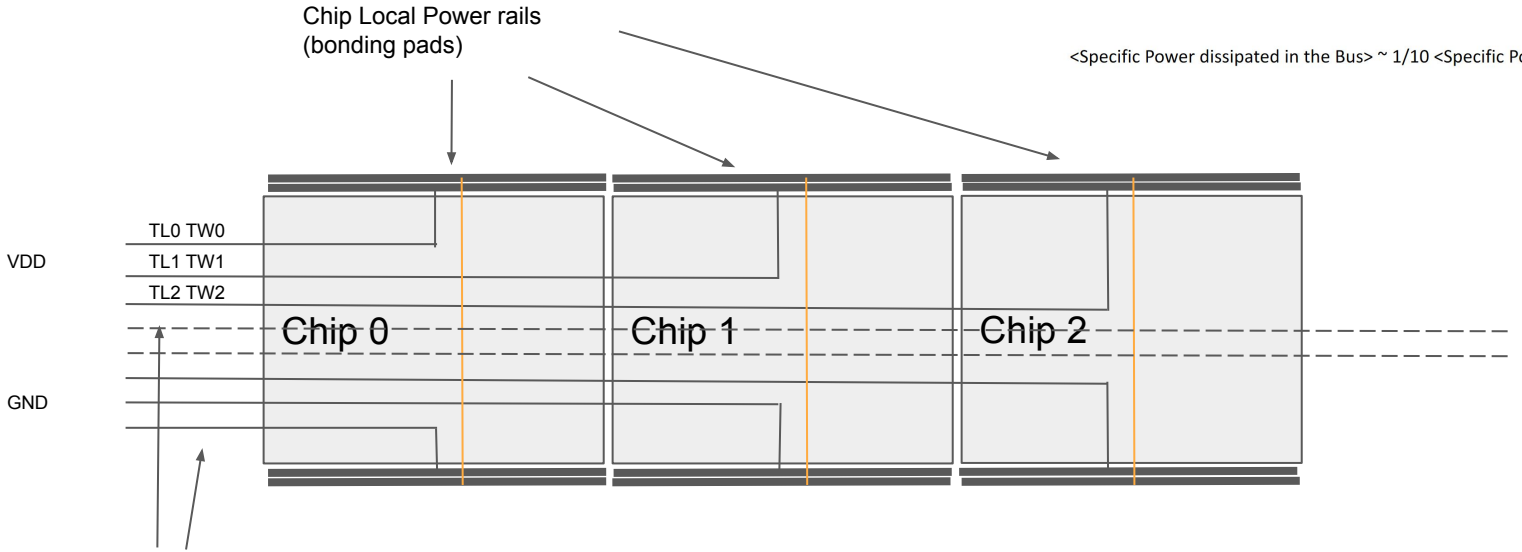
Multiline Power Bus

Each chip is powered by its own VDD and GND pair. Lines widths are calibrated to fulfill the Max Voltage drop requirement depending on the track length (i.e. chip position in the ladder, Z)
Cons:
less easy to design
Pros:
Voltage drop is the same for every chip

VTX Upgrade L3-L5 Flex Analysis

Multiline Power Bus layout Sketch



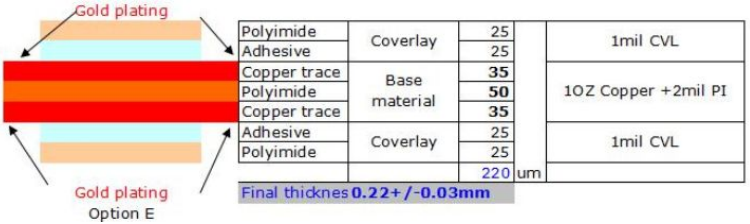


<Specific Power dissipated in the Bus> ~ 1/10 <Specific Power dissipated by the chip>

VTX Upgrade L3-L5 Flex Analysis

L5 Flex Budget breakout (35u Cu, Al)

TW = Track Width
TL = Track Length
TR = Track Resistance
Total #chips@L5 = 23 (69cm)
200mW*cm^-2 Power
100mV(VDD)+100mV(GND) maxVdrop
Both Side Ladder Access
½ L5 Ladder length = 33cm
½ L5 Ladder Width = 2.0cm
FPC with 2 Layers 35u (for both Al and Cu cases)



Multiline Power Bus X/X0 estimation

vxd layer: L5, L=36.000cm, W=2.000cm, nchips = 12
Copper, rho = 1.680e-06 ohmcm, X0 = 1.436 cm
Polyimide, rho = 1.000e+16 ohmcm, X0 = 28.570 cm

chip 0: P=1.20W V=2.00V dV=0.200V VDDTW(GNDTW)=0.386mm TL=3.000cm TR=0.037Ohms Trise=10.0C
chip 1: P=1.20W V=2.00V dV=0.200V VDDTW(GNDTW)=0.386mm TL=6.000cm TR=0.075Ohms Trise=10.0C
chip 2: P=1.20W V=2.00V dV=0.200V VDDTW(GNDTW)=0.386mm TL=9.000cm TR=0.112Ohms Trise=10.0C
chip 3: P=1.20W V=2.00V dV=0.200V VDDTW(GNDTW)=0.386mm TL=12.000cm TR=0.149Ohms Trise=10.0C
.....
chip 10: P=1.20W V=2.00V dV=0.200V VDDTW(GNDTW)=0.950mm TL=33.000cm TR=0.167Ohms Trise=2.3C
chip 11: P=1.20W V=2.00V dV=0.200V VDDTW(GNDTW)=1.037mm TL=36.000cm TR=0.167Ohms Trise=2.0C

Chip Local rail (mm) net VDD L,W,T (14.000,0.108,0.035)mm
Chip Local rail (mm) net GND L,W,T (14.000,0.108,0.035)mm
Copper VDD Bus Budget 0.058 % X0 (0.239 fill fraction)
Copper GND Bus Budget 0.058 % X0 (0.239 fill fraction)
Copper local rails Budget 0.002 % X0 (0.010 fill fraction)
Copper Data Bus Budget 0.005 % X0 (0.020 fill fraction)
Polyimide FPC Substrate Budget 0.053 % X0 (1.000 fill fraction)

Copper FPC Total Budget 0.176 % X0 -> 0.174%X0 for 17u Copper Thickness

vxd layer: L5, L=36.000cm, W=2.000cm, nchips = 12
Aluminum, rho = 2.650e-06 ohmcm, X0 = 8.897 cm
Polyimide, rho = 1.000e+16 ohmcm, X0 = 28.570 cm
chip 0: P=1.20W V=2.00V dV=0.200V VDDTW(GNDTW)=0.386mm TL=3.000cm TR=0.059Ohms Trise=10.0C
chip 1: P=1.20W V=2.00V dV=0.200V VDDTW(GNDTW)=0.386mm TL=6.000cm TR=0.118Ohms Trise=10.0C
chip 2: P=1.20W V=2.00V dV=0.200V VDDTW(GNDTW)=0.409mm TL=9.000cm TR=0.167Ohms Trise=9.1C
.....
chip 10: P=1.20W V=2.00V dV=0.200V VDDTW(GNDTW)=1.499mm TL=33.000cm TR=0.167Ohms Trise=1.1C
chip 11: P=1.20W V=2.00V dV=0.200V VDDTW(GNDTW)=1.635mm TL=36.000cm TR=0.167Ohms Trise=0.9C

Chip Local rail (mm) net VDD L,W,T (14.000,0.170,0.035)mm
Chip Local rail (mm) net GND L,W,T (14.000,0.170,0.035)mm
Aluminum VDD Bus Budget 0.015 % X0 (0.371 fill fraction)
Aluminum GND Bus Budget 0.015 % X0 (0.371 fill fraction)
Aluminum local rails Budget 0.001 % X0 (0.016 fill fraction)
Aluminum Data Bus Budget 0.001 % X0 (0.020 fill fraction)
Polyimide FPC Substrate Budget 0.053 % X0 (1.000 fill fraction)

Aluminum FPC Total Budget 0.083 % X0

VTX Upgrade L3-L5 Flex Analysis

L3, L4, L5 Flex material budget Summary

	Full (L, W, #chips)	Analysis (L/2, W, #chips)	Cu	Al	Conditions
L5	(70.041cm, 2.0cm, 24)	(36cm, 2.0cm, 12)	0.176%X0	0.083%X0	200mV, 200mWcm-2
L4	(44.526cm,2.0cm, 15)	(24cm, 2.0cm, 8)	0.117%X0	0.068%X0	
L3	(19.511cm,2.0cm, 7)	(12cm, 2.0cm, 4)	0.083%X0	0.058%X0	
L3	(19.511cm,2.0cm, 7)	(19.511cm,2.0cm, 7) One side access	0.106%X0	0.068%X0	

VTX Upgrade L3-L5 Flex Analysis

needs some additional inputs

Remarks

R1:10% of voltage drop translates in a 10% power loss on Flex lines
R2: Flex Data lines still to be modeled

Questions

Q1: In order to start data lines budget estimation, additional info about the OBELIX data lines would be needed: number of I/0 “wires”, termination scheme, max frequency, Z0…

Q2:is there any VDD and GND pads layout available?

Q3: A breakout of the OBELIX power consumption, especially with regards of the Power Supply Voltage levels and data throughput (Pdynamic, Pstatic), would be very useful so that layer dependent optimization could be evaluated

Q4: Bypass capacitors, capacitance, ESR and max distance?

Thanks!