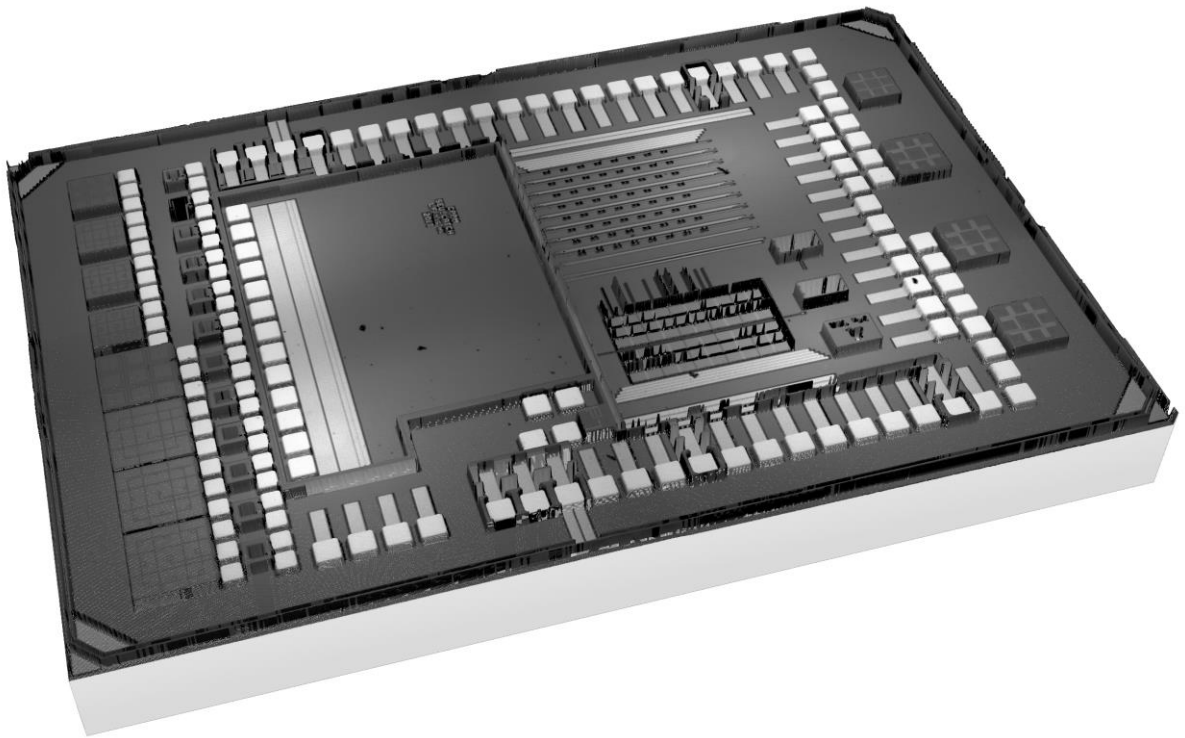


HEPHY Contribution Plans

Overview HEPHY

- Contributions to Belle II
  - HEPHY was and still is deeply involved in construction and operation of the Belle II SVD
  - Overall concept, mechanics, front- and backend electronics, DSSD design, module production, online software, FADC firmware, etc.
- Moderate experience in ASIC design
  - Training period at CERN in TJ-MALTA project
    - Christian Irmler, Patrick Sieberer
  - Heavily involved in **digital design** of RD50-MPW3 chip
    - Full digital part (periphery like EOC and control unit)
    - Still in starting phase (**RTL-level**)
  - Lots of testing / characterization experiments for RD50-MPW2 chip (probestation, Sr90, laser, testbeams)
  - Software + Licenses
    - CADENCE IC package licenses available
    - LFoundry PDK/NDA available
    - **No TowerJazz PDK/NDA yet**

Features of EOC

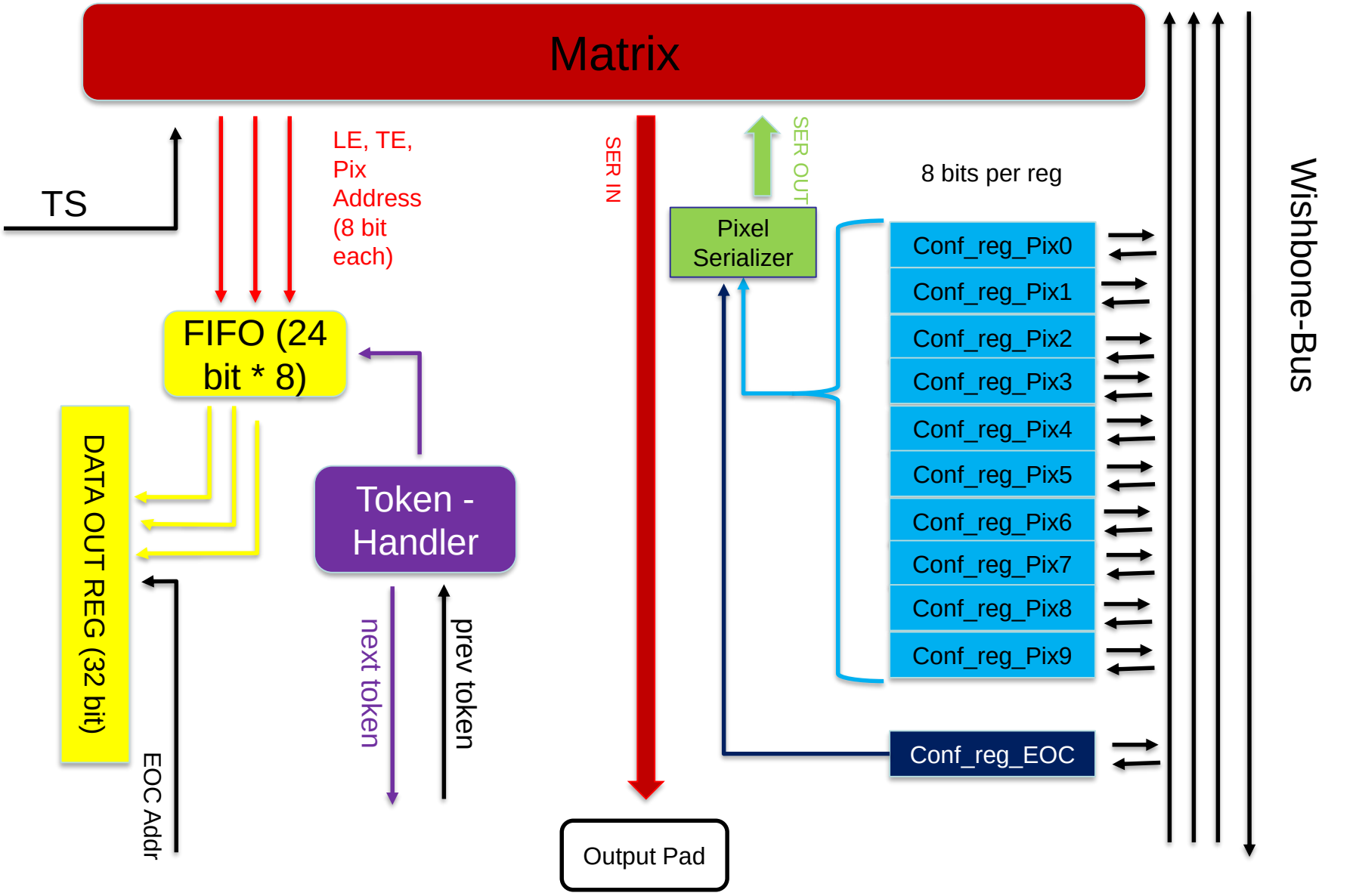
General

- Designed for RD50-MPW3
  - Target technology: LF15A (150nm)
- **RTL-Level**
  - Written in SystemVerilog
  - Currently tested in FPGA
  - Simple testbench available
- Documentation available in a few weeks
- Property of Hephy/RD50
  - RD50 okay with sharing
  - Using some CADENCE chip ware (CW) components (License/NDA?)

Technical

- Fully working **Wishbone interface** + config-regs
  - Simple R/W only
  - Block R/W planned
  - Broadcasting planned
- **Serializer** (40MHz) to shift data to pixels
  - Similar block used in CMS pixels
- **Double Column Architecture**
  - FIFO capturing data from pixels
  - Simple priority Token-handler
- Parallel (32bit) Data output
  - 40MHz rate => 1.280 GHz single transmission line needed
  - Planned to split in 2x 640MHz

Schematic of EOC



Manpower

- **Christoph Schwanda:** Belle II PI at HEPHY
- **Thomas Bergauer:** Detector Development Leader

- **Christian Irmler:** senior engineer, digital design (ASIC)
- **Helmut Steininger:** senior engineer, digital design expert (FPGA)
- **Patrick Sieberer:** PhD Student, digital design (ASIC)
- **Currently hiring additional PostDoc**, analog / digital Design (ASIC)

- Above listed personnel is also involved in other projects, thus only partially available for OBELIX

Interests

- HEPHY is interested to contribute to OBELIX in the following fields
  - Design and verification of digital periphery (e.g. EOC)
  - Verification and evaluation of functional blocks in an FPGA
  - Characterization and testing of OBELIX
    (probably also already Monopix2)