



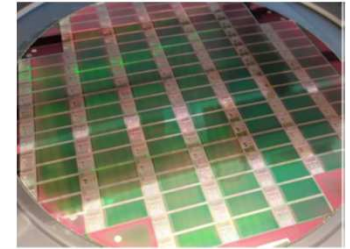
CPPM DepCMOS dvp -interests in OBELIX design-

May 12th 2021

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LF150 project



LF-FOUNDRY 150nm technology

CPPM: Implication since 2012

LF-MONOPIX2 circuit (Bonn, CPPM, IRFU)

Sent for fabrication June 2020 (tests started Feb.2021) : 12 wafers

- will request for 2 wafers with standard passivation with polyimide
- remaining 10 wafers with "special" passivation, in order to have higher temperature tolerance for backside processing

+ Test Structures :

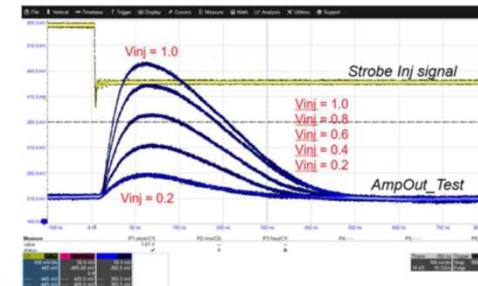
Small pixel pixels ($50\mu \times 50\mu$), Bandgap, Guard Ring tests, APD

PCB done and produced.



On-going:

- LF-Monopix2 Card dvp by Bonn (2 setups in CPPM).
- LF-Monopix2 tests have started, Bonn and CPPM.
- 1st positive tests on LF-Monopix2 (CPPM/Bonn).
- Wirebonding of tests structures on-going → 1st tests soon.



TJ180 project

TJ 180nm CIS technology

CPPM: Implication since 2016

TJ-MONOPIX₂ (CERN, Bonn)

Sent for fab Nov 2020 (tests started in March)

Bonn test bench (firmware, carte, software).

CPPM:

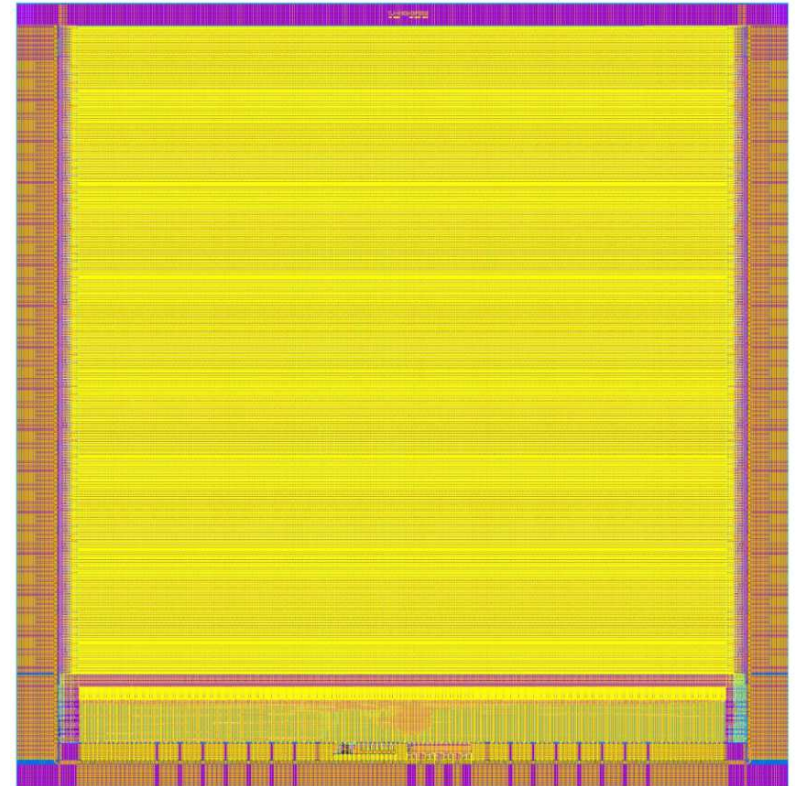
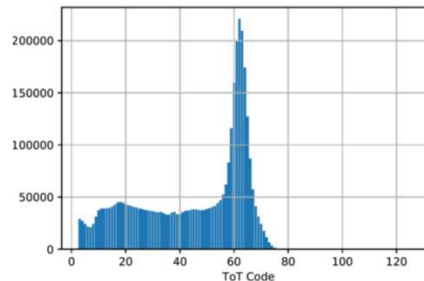
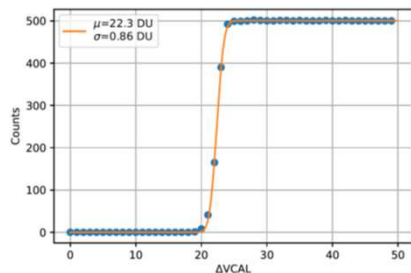
Getting ready for testing the circuit

Test bench mounting on-going

(synergies LF150 and TJ180 testing)

Wire-bonding tries with local compagny

1st positive tests (Bonn):



CPPM also has a TJ 65 nm implication ...
1st designs done in 2020

Team plans / support

- DepCMOS: developped in CPPM for ATLAS L4, interest for Future Colliders and BelleII upgrade.
- Support from DICE IN2P3 master project + AIDAinnova.
- Team:



- Manpower:
 - Testing TJ / LF / test structures: ~1.5-2 FTE
 - Experience with: Monopix series, tests in lab, tests under radiation, SEU test...
 - Design TJ180 OBELIX: ~1-1.5 FTE
 - Experience with: TJ technology ; design ShuntLDO / SEU hard cells (DICE, TRL...)
- Interests in OBELIX:
 - LDO, SEU-hard cells + analog FE, Bias DACs...
 - ClioSoft management, participation to integration, floorplanning, simulation ...