FTSW version 4 for CDC FEE upgrade

Mikihiko Nakao (KEK)

mikihiko.nakao@kek.jp

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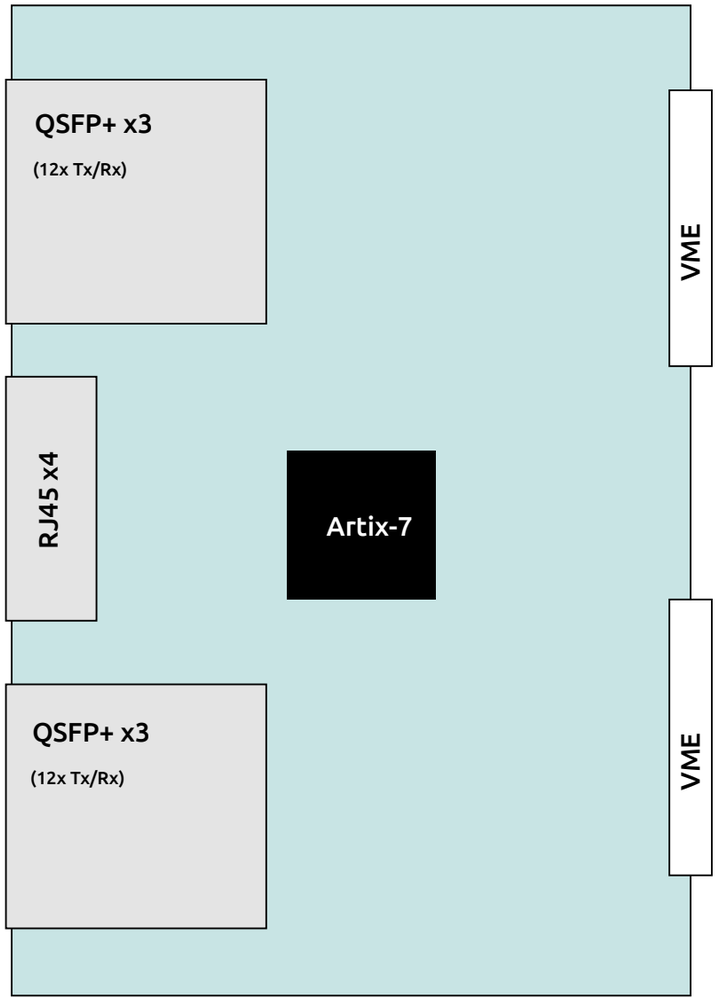
DAQ meeting

Motivations

- **CDC FEE upgrade project has just started**
  - To improve radiation tolerance
  - No change in the channel density per board
- **Current b2tt / jtag could be more troublesome**
  - Clock jitter cleaner may improve b2tt / b2link, but radiation tolerance is unclear
  - Noise margin of b2tt lines is also very small
  - Larger FPGA requires bf too long programming time
- **Small Kakenhi grant to work on “self-recoverable” FEE design**
  - Sevaral new ideas to improve the reliablility of the FEE
  - Some of them may be applicable to the new CDC FEE
- **Basic ideas**
  - Fully optical connections between FTSW and FEE
  - JTAG is also encoded into AC-coupled optical line

FTSW version 4 (baseline)

- **Form factor**
  - VME 6U, 1 slot width
- **Components**
  - Artix-7 FPGA
  - QSFP+ x6 (24-pair fibers)
  - RJ-45 x4
  - Same jitter cleaner
- **Protocol**
  - Same b2tt as used in the optical connections between E-hut and on-detector FTSWs
  - No more jtag-over-b2tt, feed JTAG from outside as done by TOP (faster!)



Possible Technology Choices

- **FPGA**
  - Artix-7 with sufficient number of I/O pin and logic cells will be enough
- **Optical Transceiver**
  - Minipod or Micropod was a candidate, but they are “not recommended for new design”
  - SAMTEC Firefly is a new generation multi-port transceiver, but very expensive and very limited info (I heard it’s popular in LHC nowadays)
  - QSFP+ has only 4 ports, but easy to procure at a reasonable price
- **More ideas?**
  - Clock data recovery? — if clock can be extracted from b2tt data, we can save clock lines
  - Optical splitter for clocks? — clock lines may be just split inside the detector
  - RJ-45 version of FTSW4? — for FTSW3 replacement
  - Multi-gigabit transceiver for the next generation b2tt for >30kHz?

Configuration for CDC

- **300 FEEs, 4 FTSW crates**
  - Each crate should cover up to 80 FEEs
  - Now: Up to 9 FTSW version 3 (18 slots)
- **How to connect to 80 FEEs?**
  - Each FTSW4 has 20x optical Tx
  - 4x FTSW4 for b2tt, 4x FTSW4 for clock, 4x FTSW4 for JTAG
  - 1x FTSW3 to receive from E-hut, distribute to 4+4x FTSW4 for b2tt/clock
  - JTAG cannot be connected to FTSW3, but can be behind FTSW4
  - In total, 14 VME6U slots are needed

JTAG over fiber

- **Idea**
  - Clock duty cycle modulation to send JTAG data over clock
  - Decoder can't be an FPGA or CPLD, need a discrete logic
- **Design** (see backup)
  - Line delay, 10-bit shift register and NOT/AND/OR logic
  - Can be built with about 10 TSSOP chips
  - Clock frequency can be 63MHz, to encode 8MHz JTAG signal, using SN74ALVC and SN74LVC chips
- **Implementation**
  - Need to make a test board to find any surprise

FTSW4 in E-hut?

- **FTSW4 can be also used in E-hut**
  - PCIe40 can receive b2tt in one of the optical line?
  - If yes, we can get rid of intermediate FTSW for PCIe40
- **All optical connections**
  - FTSW to on-detector via optical fibers (as it is now)
  - FTSW to PCIe40 via optical fibers
  - Intermediate FTSW for ARICH will be no more needed (but we still need it for KLM)

Plan

- **Urgent work**
  - Chip selection for CDC FEE (radiation tolerance)
  - JTAG logic confirmation
- **Board design**
  - No technical challenge, unless clock-data-recovery is attempted
  - Not urgent, target is 2026 LS2
  - Chance to consider b2tt upgrade for a higher trigger rate
- **Firmware design**
  - Baseline: just a variant of FTSW3 firmware
  - JTAG encoding/decoding should be newly developed, but not a big work
  - Small size Artix-7 evaluation boards are in hand

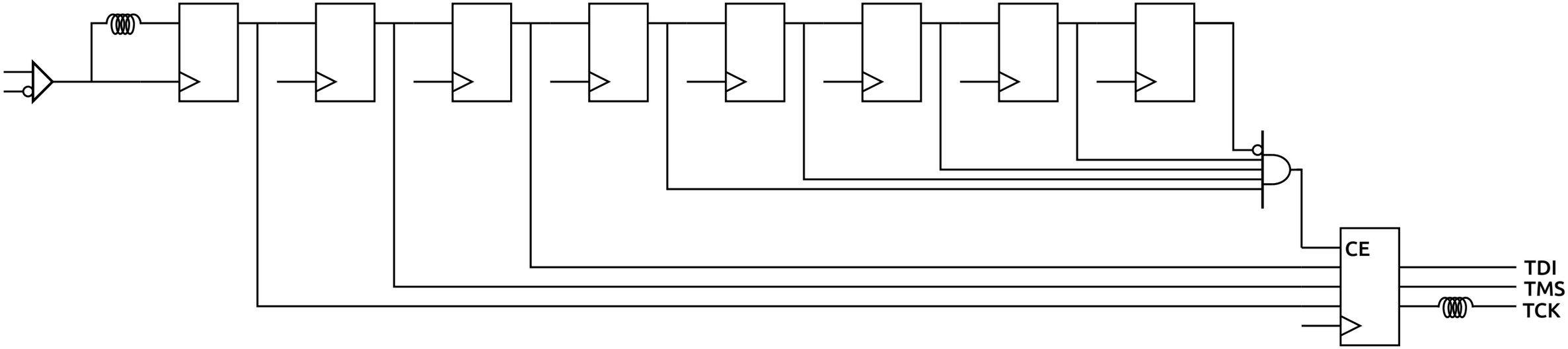
Backup

JTAG

- **1-bit Clock duty cycle modulation** (Idea from Honda-san)
  - (e.g.) 75:25 duty cycle for H, 25:75 duty cycle for L
  - Clock jitter does not matter much for JTAG
  - 8-bit/clock sequence: 0 1 1 1 1 a b c → TDI=a TMS=b TCK=c
  - 127 MHz clock → 16 MHz TCK (fast enough), or 63 MHz → 8 MHz TCK (still fast)
- **A similar variant for 1-bit TDO return**
- **How to implement?**
  - Line-delay (4ns for 127MHz) + D-FF would be enough
  - 8-bit shift register to catch the sequence
  - Discrete circuit of 74-series ICs for radiation tolerance (EEPROM device is probably dangerous)
  - 74LVC / 74ALVC series may be capable to handle 127 MHz, need to test
  - Around 10 TSSOP(?) chips are needed, a bit of area (is it acceptable?)

Possible design

- 8-bit/clock sequence: 0 1 1 1 1 a b c → TDI=a TMS=b TCK=c



- Delay-line: DS1110LZ-20+ (4ns)
- 8-bit D-FF: SN74LVC377 (max freq. >150 MHz)
- Fast 2-input AND/NAND gates: SN74ALVC08/00 (1–3ns per gate)
- 5-input AND has to be done in 3 steps and may take more than 1 clock if 127 MHz
  (I'm not sure also that the delay-line part works with 127 MHz)
- Any other/better idea?