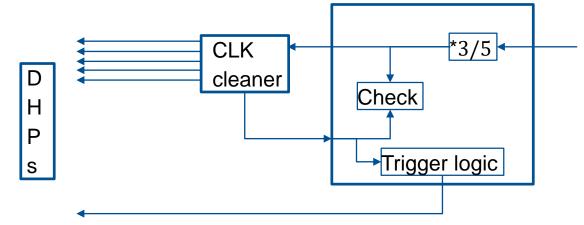
DHI clock issue

- Instabilities first observed during testing the gated mode
 - Certain internal counters behaved strangely and lost synchronization
 - Added capacitors to fix pickup of noise induced by the power lines to the clock-recovery chip
 - Implemented PVs to monitor if this problem occurs
 - Check if revo signal arrives at a calculated time (Only checked for one output)
 - Check if counters with different clocks run synchronously
 - \Rightarrow Both things seem not to be the case on DHI58

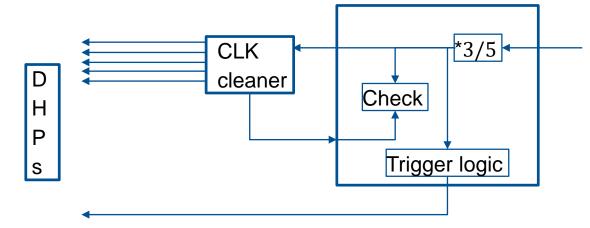
Current Scheme



DHI clock issue

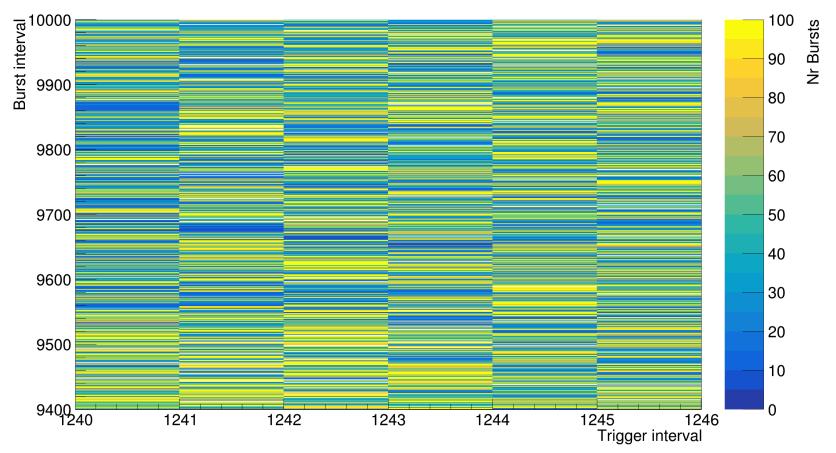
- Instabilities first observed during testing the gated mode
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New Scheme => deployed 27.5 => fixed occupancy drops on 1051



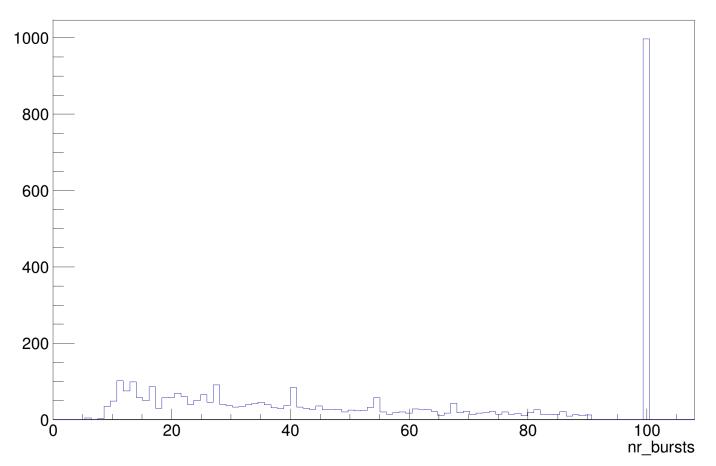
Occupancy drop: Parameter scan

burst_dist:trg_dist {nr_bursts*(nr_bursts<700)}</pre>

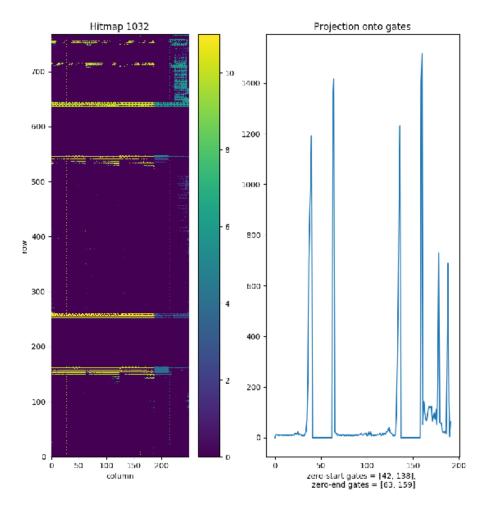


Occupancy drop: parameter scan (Nr bursts)

nr_bursts



Gated mode tests at DESY



Gated mode tests at DESY

Local gated mode emulation

- Testpattern /standby
 - Scan of trigger inhibit length and offset parameters
 - Check effect of DHP latency
 - Check effect of kicksub parameter
- Peak, noise with timing pixels
 - Scan of gate_length, gate_offset
 - Scan of relative phase of trigger inhibit to pedestal fluctuations
 - => DHP latency + ~8 gates from online monitor, exact values from detailed analysis
- External pulse generator
 - Asynchronous to FTSW, set length of gated mode to 1800 revo cycles (~18us)
 - Kick signal with 50Hz, 25Hz => gated mode visible in 90%, 45% of the events

DHC features

- 1. DHC_20190520_1038 (deployed 30.5.2019)
 - Generate local triggers while frames are synchronized by FTSW√
 - Local trigger generation synchronized over all 4 DHCs (due to 2 revo-cycles per frame)
 Using revo9 signal from FTSW ✓
 - Backpressure test to DHE (needed for future firmware) \checkmark
 - Counters for link losses from FTSW \checkmark
 - Gated mode implementation (still with length information from FTSW) ✓
- 2. Currently being tested at DESY
 - Configurable DHE order in data stream ✓
 - Gate mode length information from slow control \checkmark
 - Data being analyzed by Varghese
 - DHP resynchronization during a run×
 Intermediate version showed some instabilities during tests at KEK ×