Tests of DHH firmware for gated-mode operation

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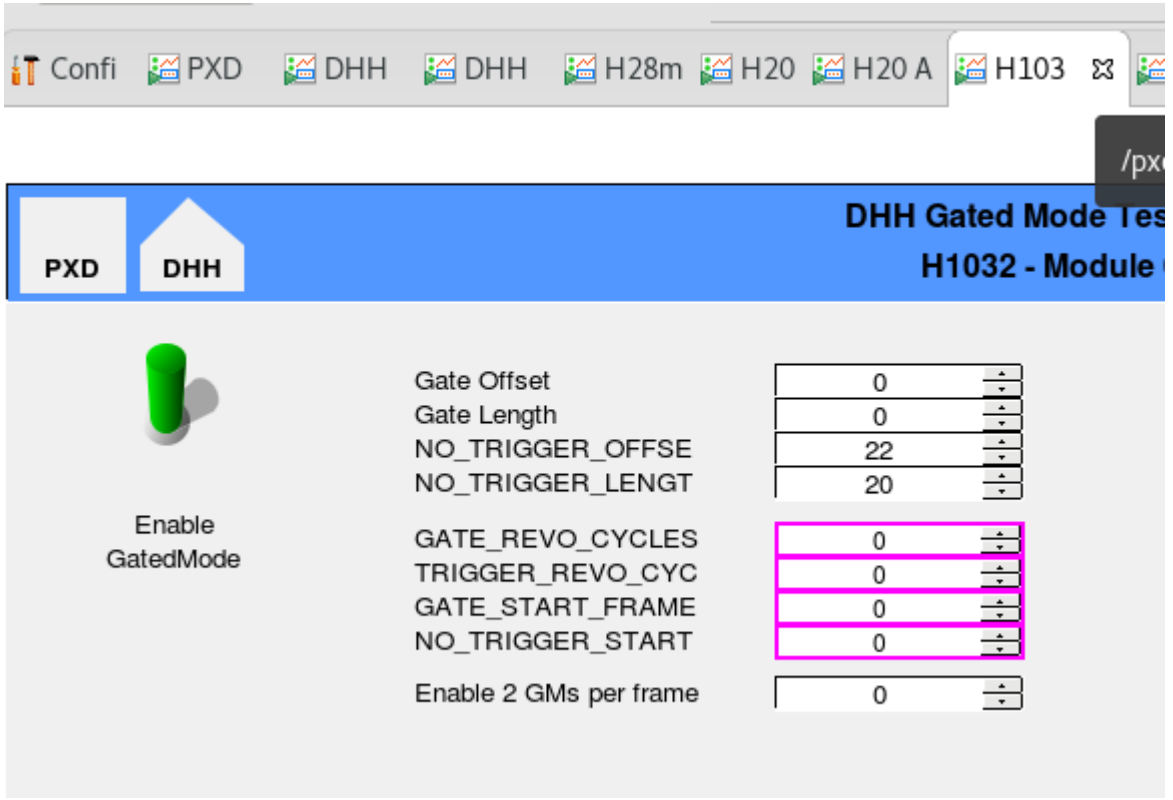
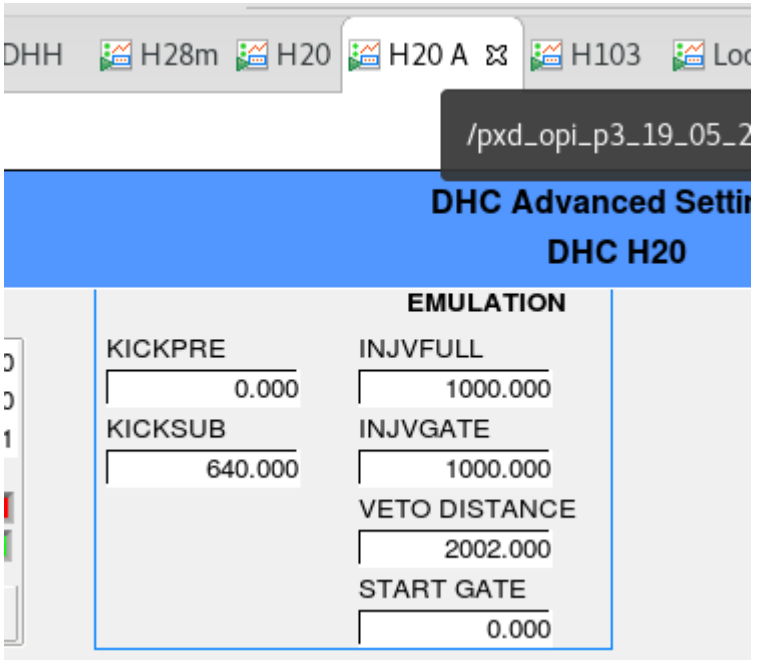
Performed for firmware versions:
DHI: 20190525_0948
DHC: 20190531_2114
DHE: 20190511_1446





- **Test 1 :** Test of no-trigger-veto

➔ Power H1032 to STANDBY and upload test pattern

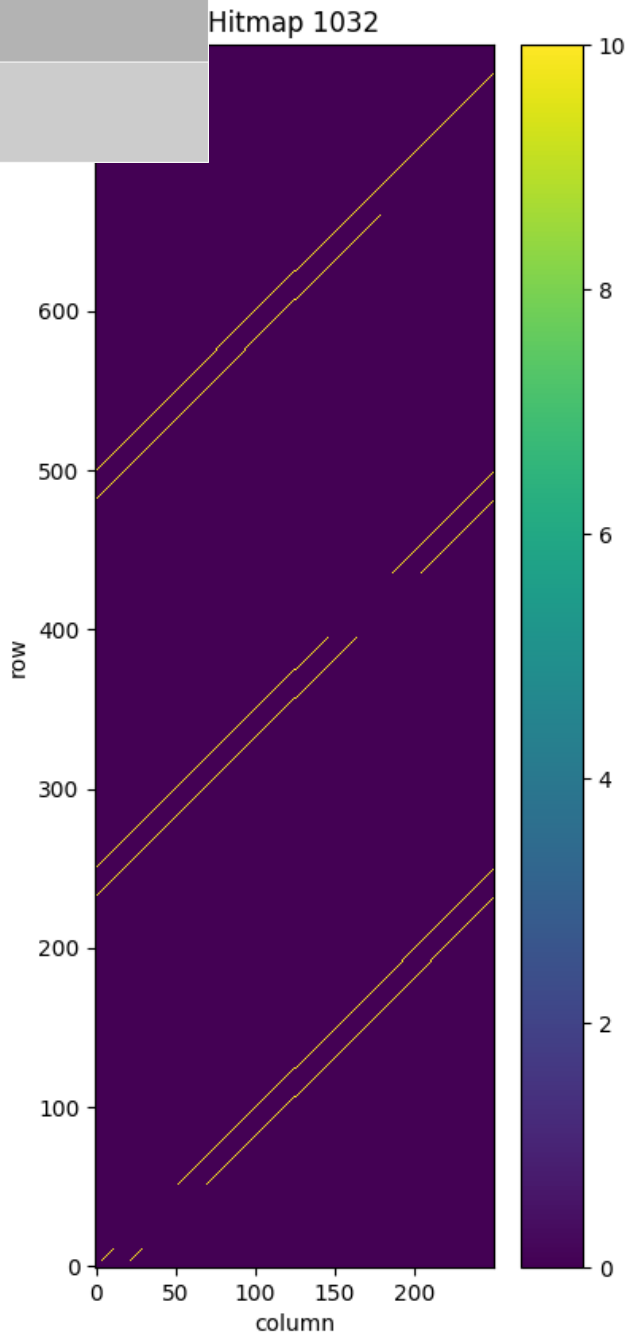
➔ Change parameters no-trigger-offset and no-trigger-length and look changed settings are reflected in data.

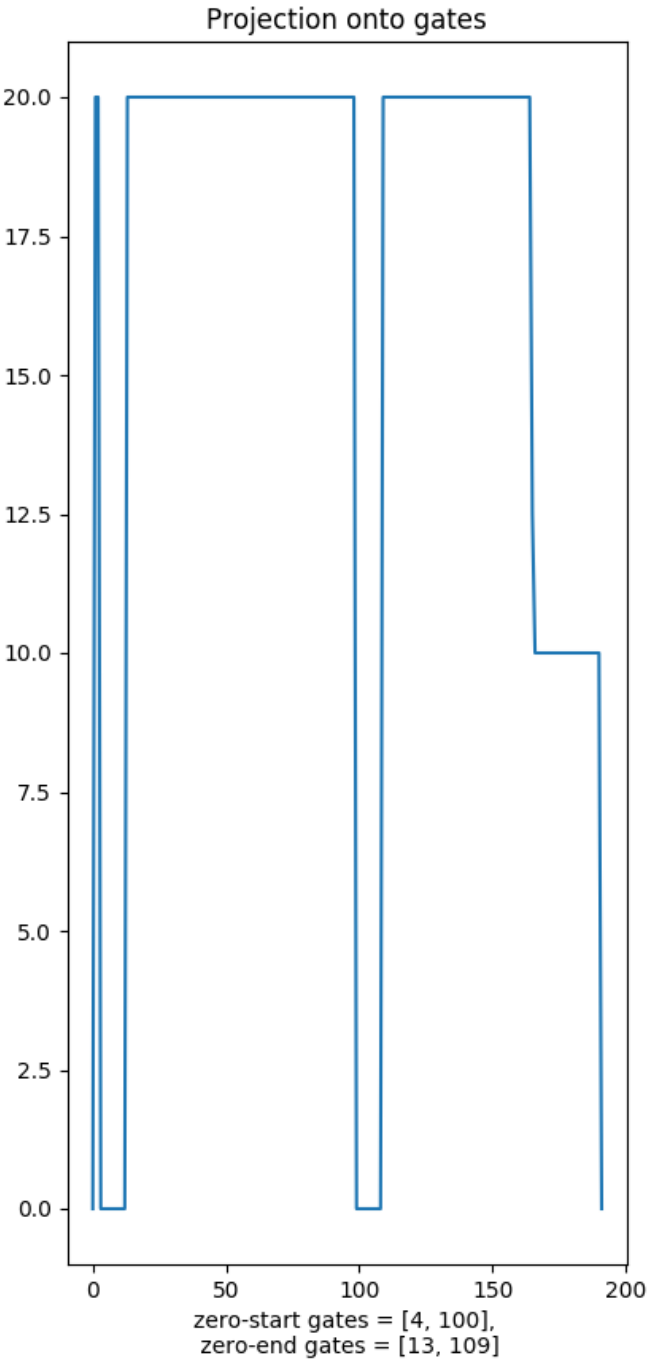
➔ Data recorded with internal triggers and DHC emulated inj-kick signal.

Input Gate-offset	Input Gate-length	DHP-latency	kicksub
0	10		

Note:

1032 is an IB module, hence rolling shutter starts at gate-192 and ends at gate-1. (Backwards with respect to the geometrical row ordering)





No-trig-length = 10

Input Gate-offset	Input Gate-length	Input DHP-latency	Input kicksub	First no-trig window seen in data	Second no-trig window seen in data	No-trigger length seen in data
0	10	5	0	4-13	100-109	10
20	10	5	0	80-89	176-185	10
40	10	5	0	60-69	156-165	10
60	10	5	0	40-49	136-145	10
80	10	5	0	20-29	116-125	10
0	20	5	0	90-109	186-13	20
20	20	5	0	70-89	166-185	20
40	20	5	0	50-69	146-165	20
60	20	5	0	30-49	126-145	20
80	20	5	0	10-29	106-125	20
22	10	5	0	78-87	174-183	10
22	10	10	0	83-92	179-188	10
22	20	10	0	169-188		20
22	20	10	640	121-140		20

1-GM per frame

Input No-trig-offset	Input No-trig-length	Input DHP-latency	Input kicksub	First no-trig window seen in data	Second no-trig window seen in data	No-trigger length seen in data
0	10	5	0	4-13	100-109	10
20	10	5	0	80-89	176-185	10
40	10	5	0	60-69	156-165	10
60	10	5	0	40-49	136-145	10
80	10	5	0	20-29	116-125	10
0	20	5	0	90-109	186-13	20
20	20	5	0	70-89	166-185	20
40	20	5	0	50-69	146-165	20
60	20	5	0	30-49	126-145	20
80	20	5	0	10-29	106-125	20
22	10	5	0	78-87	174-183	10
22	10	10	0	83-92	179-188	10
22	20	10	0	169-188		20
22	20	10	640	121-140		20

No-trig-length = 20

1-GM per frame

Input Gate-offset	Input Gate-length	Input DHP-latency	Input kicksub	First no-trig window seen in data	Second no-trig window seen in data	No-trigger length seen in data
0	10	5	0	4-13	100-109	10
20	10	5	0	80-89	176-185	10
40	10	5	0	60-69	156-165	10
60	10	5	0	40-49	136-145	10
80	10	5	0	20-29	116-125	10
0	20	5	0	90-109	186-13	20
20	20	5	0	70-89	166-185	20
40	20	5	0	50-69	146-165	20
60	20	5	0	30-49	126-145	20
80	20	5	0	10-29	106-125	20
22	10	5	0	78-87	174-183	10
22	10	10	0	83-92	179-188	10
22	20	10	0	169-188		20
22	20	10	640	121-140		20

DHP-latency Produces 1:1 change in no-trig-offset

1-GM per frame

Input Gate-offset	Input Gate-length	Input DHP-latency	Input kicksub	First no-trig window seen in data	Second no-trig window seen in data	No-trigger length seen in data
0	10	5	0	4-13	100-109	10
20	10	5	0	80-89	176-185	10
40	10	5	0	60-69	156-165	10
60	10	5	0	40-49	136-145	10
80	10	5	0	20-29	116-125	10
0	20	5	0	90-109	186-13	20
20	20	5	0	70-89	166-185	20
40	20	5	0	50-69	146-165	20
60	20	5	0	30-49	126-145	20
80	20	5	0	10-29	106-125	20
22	10	5	0	78-87	174-183	10
22	10	10	0	83-92	179-188	10
22	20	10	0	169-188		20
22	20	10	640	121-140		20

Kicksub = 640 leads to a change of 48 gates for the no-trig-offset

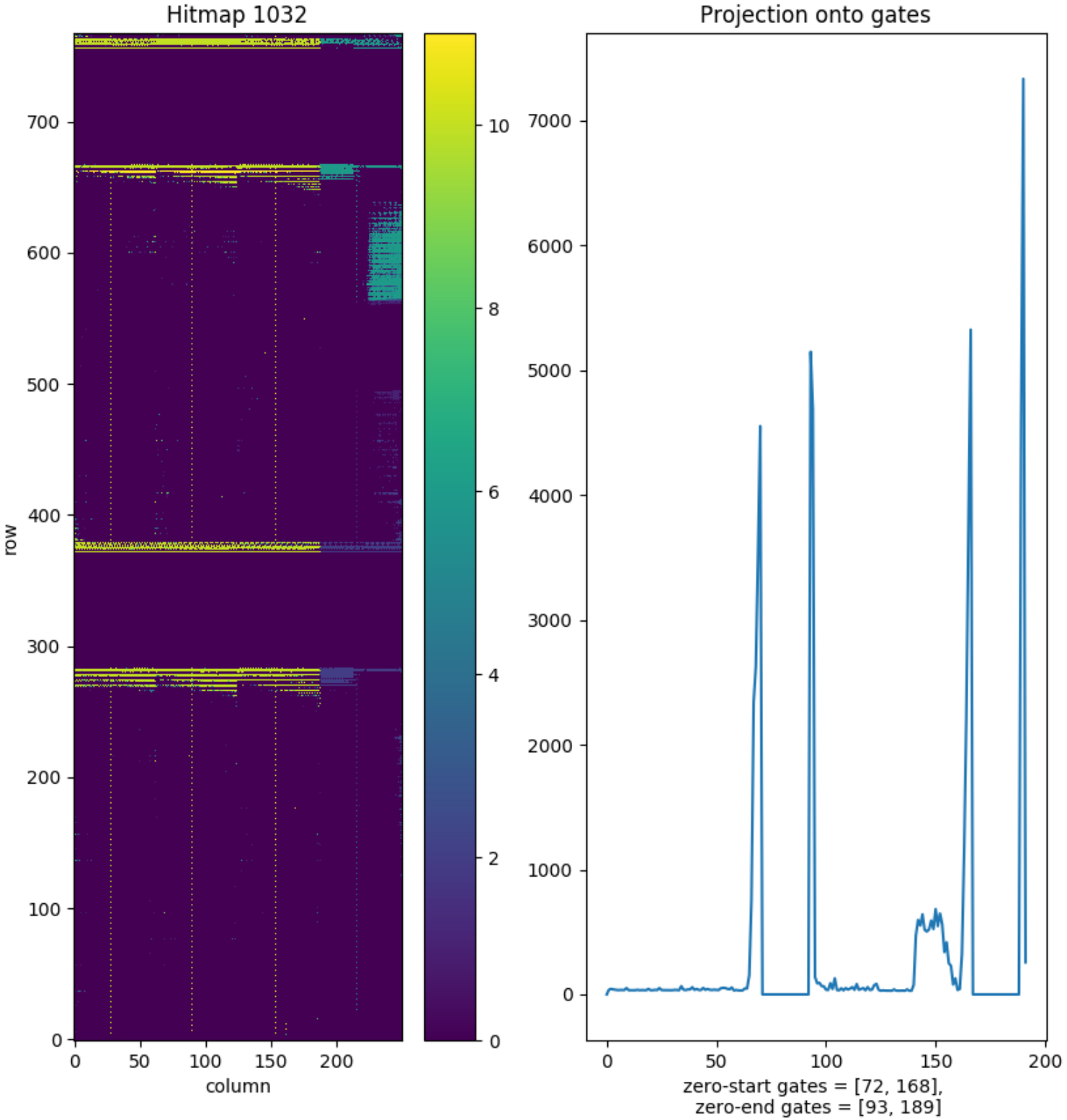
1-GM per frame

- **Test 2 :** Test of no-trigger-veto and gating

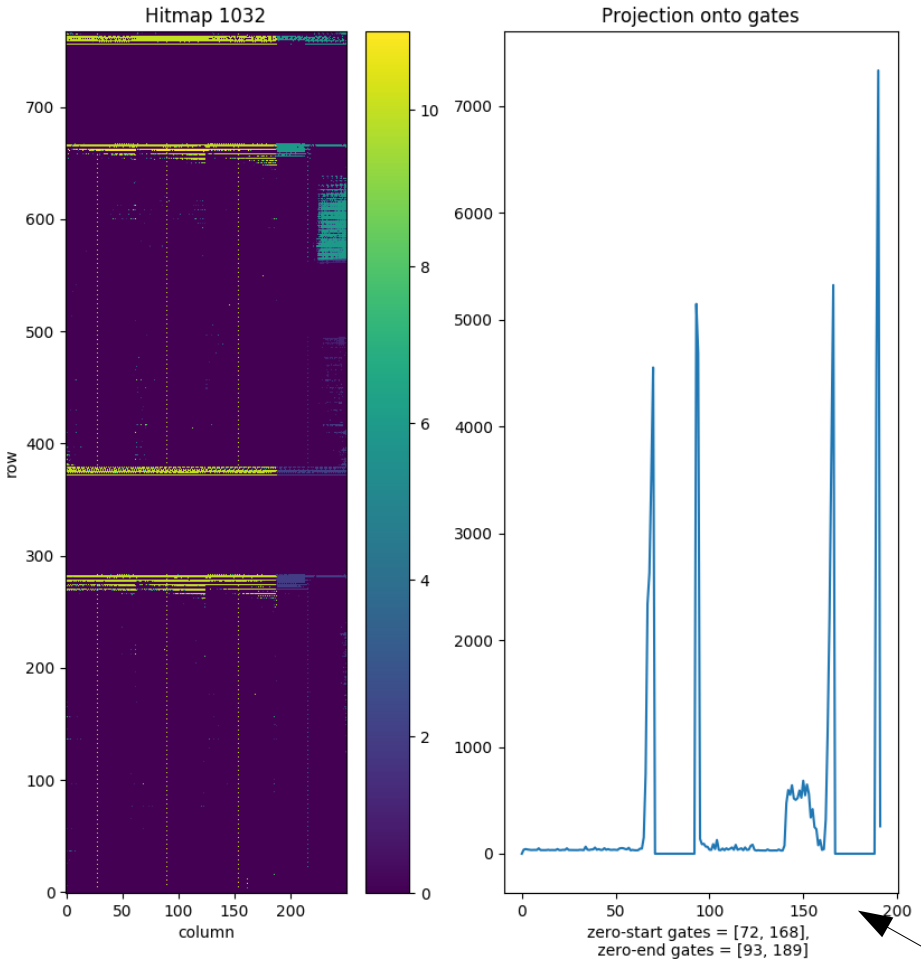
➔ Power H1032 to PEAK, upload pedestals to DHP with constantly-firing-pixels (1 per gate for each ASIC pair)

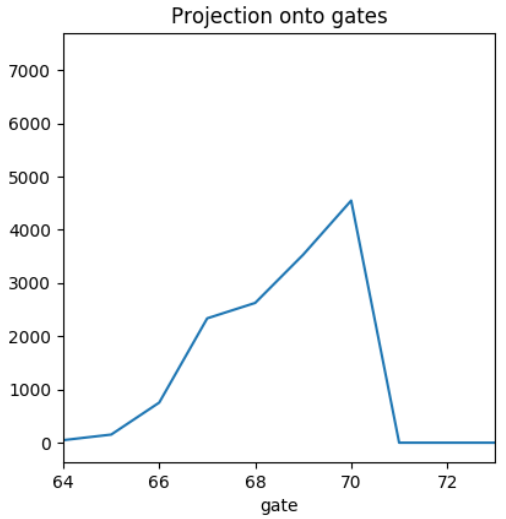
➔ Change parameters no-trigger-offset, no-trigger-length, gate-offset and gate-length and look changed settings are reflected in data.

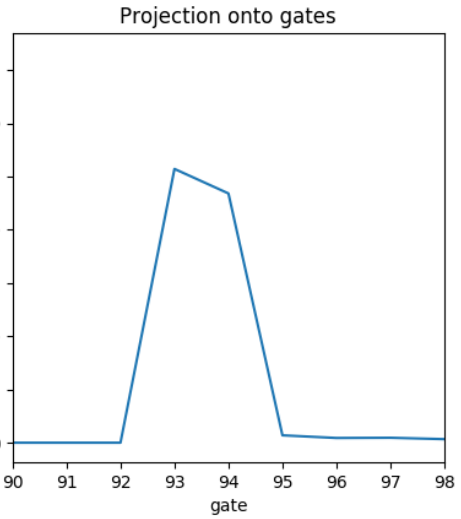
➔ Data recorded with internal triggers and DHC emulated inj-kick signal.

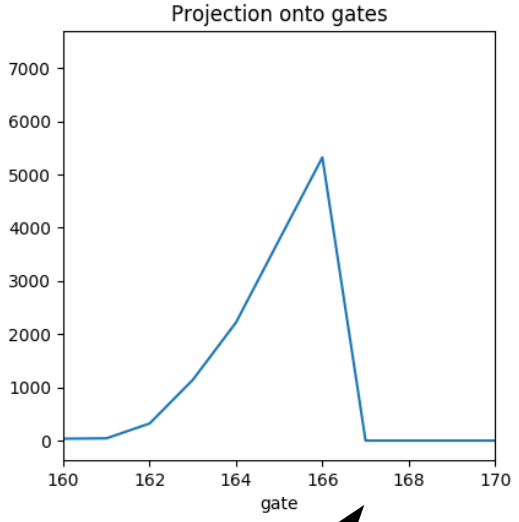

Hitmap 1032
row
column
0
100
200
300
400
500
600
700
0
50
100
150
200
0
2
4
6
8
10
Projection onto gates
0
1000
2000
3000
4000
5000
6000
7000
0
50
100
150
200
zero-start gates = [72, 168],
zero-end gates = [93, 189]

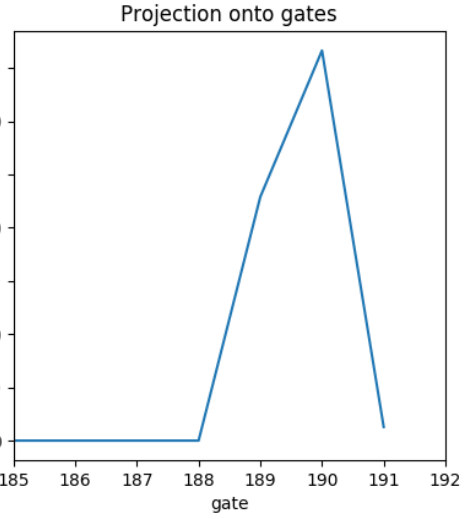
Gate lenght cannot be verified by looking at noisy pixels in data. Assuming gate-length is set correctly, we can estimate oscillation period.







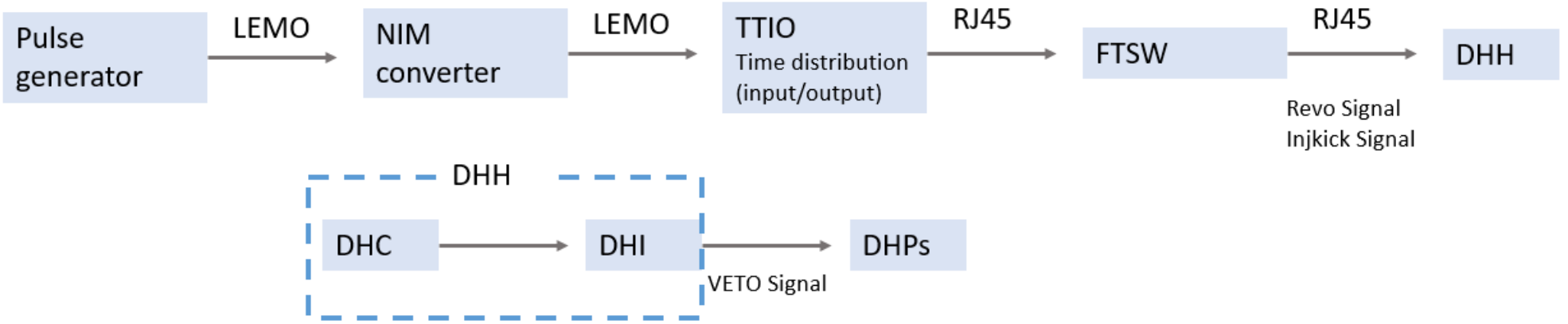




Actually x-axis is (gate-1)

Input Gate-offset	Input Gate-length	Input No-trigger-offset	Input No-trigger-length	Start of no trigger seen in	No-trigger length seen in data	Start of gating	Estimated oscillation period (gates)
0	10	12	12	189, 93	12	191, 95	~11, 10 **(?)**
30	10	42	12				
60	10	72	12				
90	10	102	12				
90	10	6	12				
0	20	12	22				
30	20	42	22				
60	20	72	22				
90	20	102	22				
90	20	6	22				
10	10	18	12				
10	10	19	12				
10	10	20	12				
10	10	21	12				
10	10	22	12				
10	10	23	12				

- **Test 3 :** Supply inj-kick signal externally toDHH via FTSW to mimic real inj-kick signal from Machine group

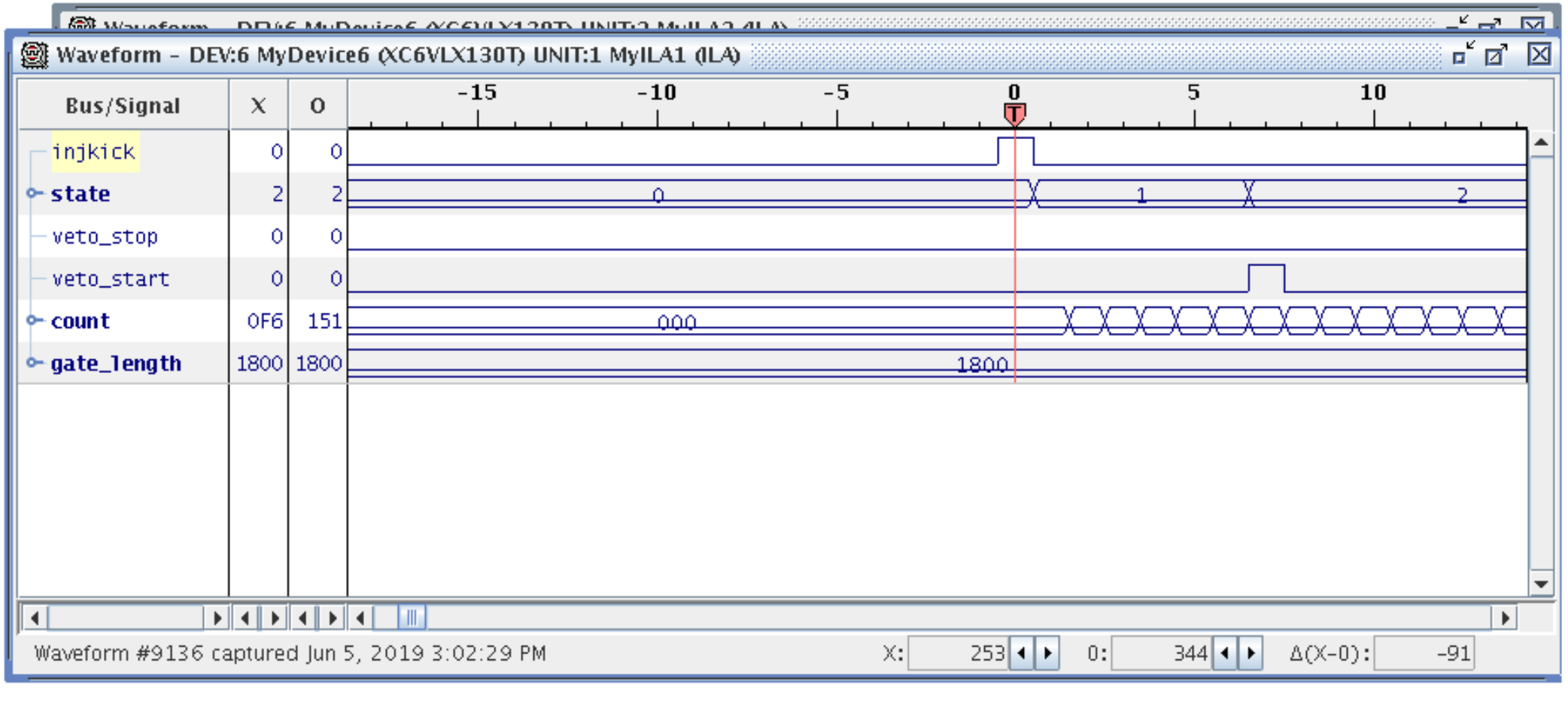


- ➔ Look at signal wave form using chipscope-software
- ➔ Power module 1032 to STANDBY, upload test-pattern.
- ➔ Vary inj-kick signal frequency: 50Hz, 25 Hz

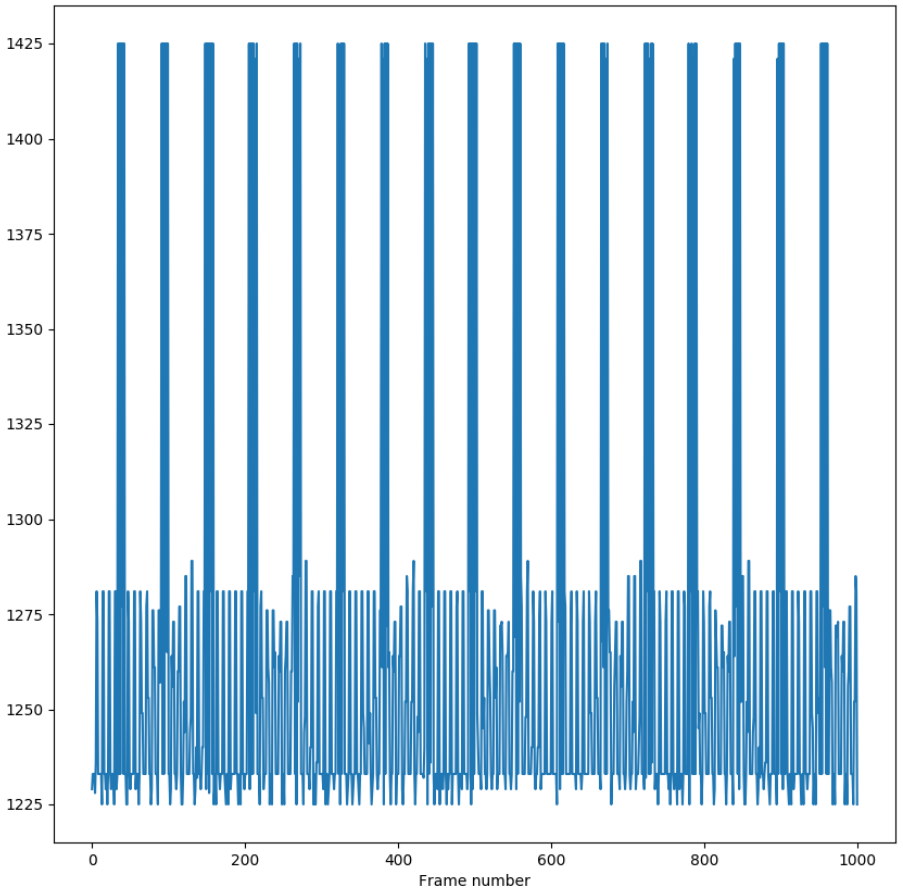
  Trigger frequency: 100 Hz (internal) and apply no-trigger veto

Chipscope view

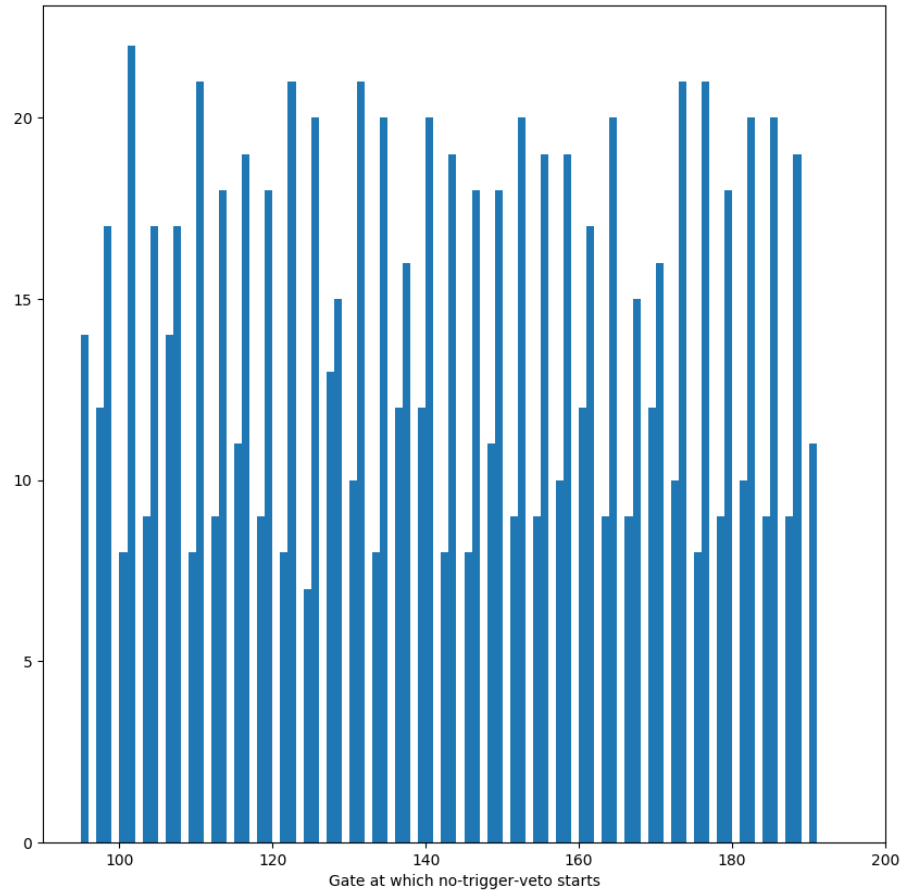
In this case INJVFULL = 1000 and INJVGATE = 800
So total gate-length = 1800 revolution cycles



Inj-Kick frequency = 50 Hz, trigger = 100 Hz



Number of hits vs frame number
(1000 frames)

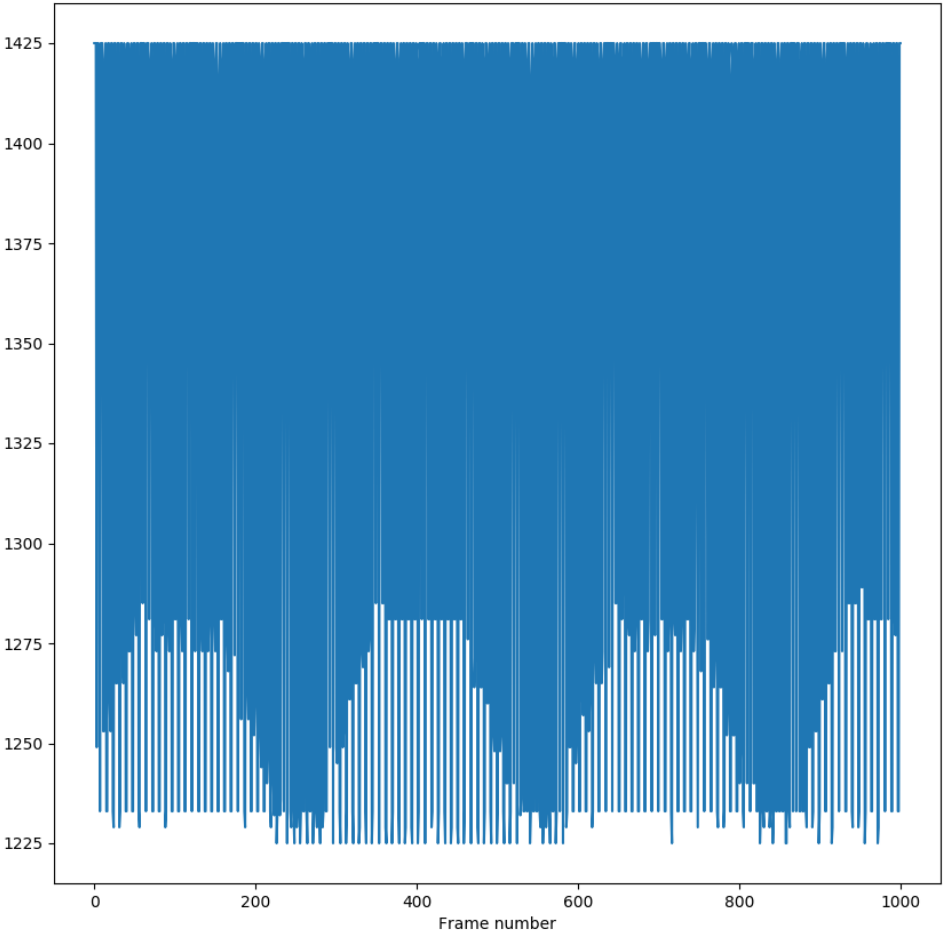


Gate at start of no-trigger-veto

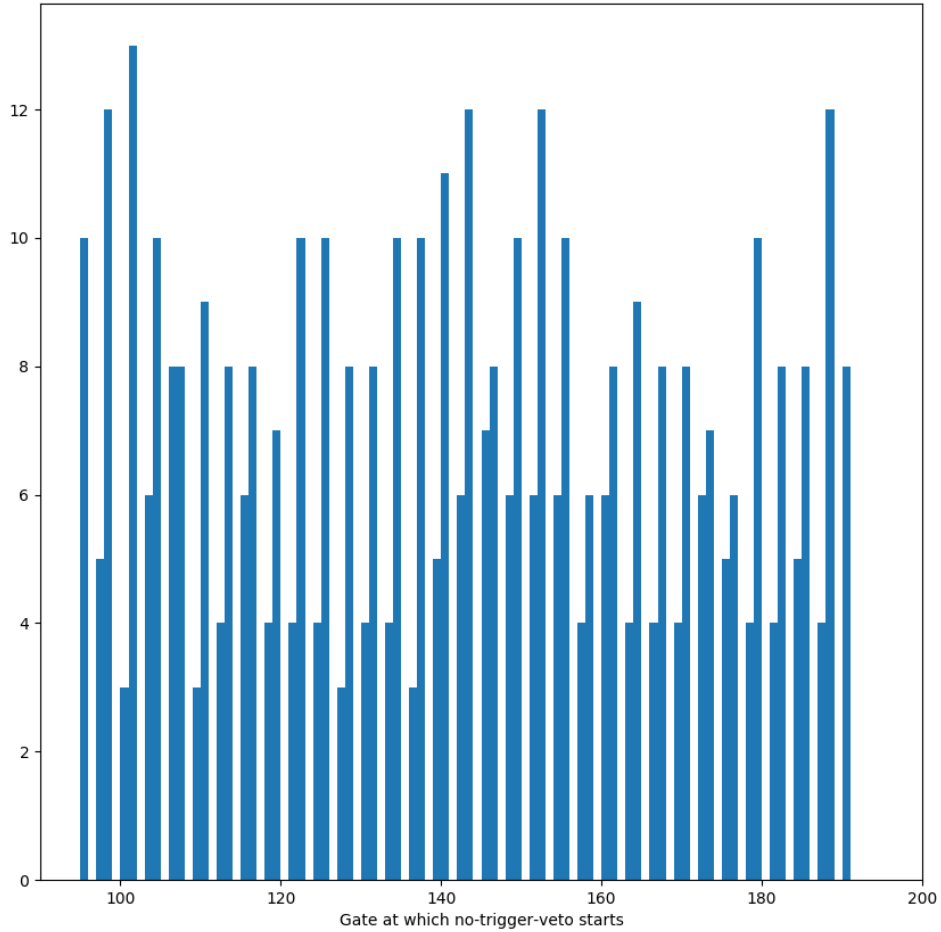
Number of frames in gated-mode: 909
Number of frames not in gated mode: 91
Probability of frame to be in gated mode: ~91%

Inject-kick signal every 20ms or ~2000 revolution cycles
Period in gater mode = INJVFULL + INJVGATE = 1000 + 800 = 1800 revolution cycles

Inj-Kick frequency = 25 Hz, trigger = 100 Hz



Number of hits vs frame number
(1000 frames)



Gate at start of no-trigger-veto

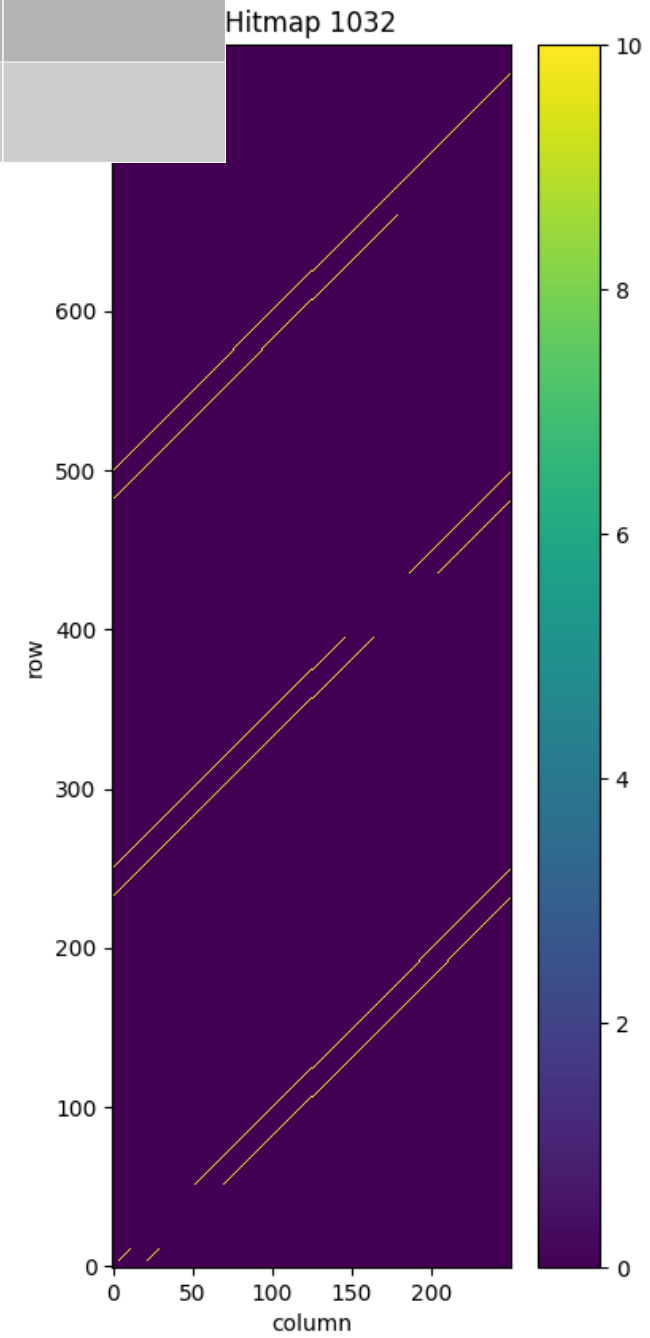
Number of frames in gated-mode: 450
Number of frames not in gated mode: 550
Probability of frame to be in gated mode: ~45%

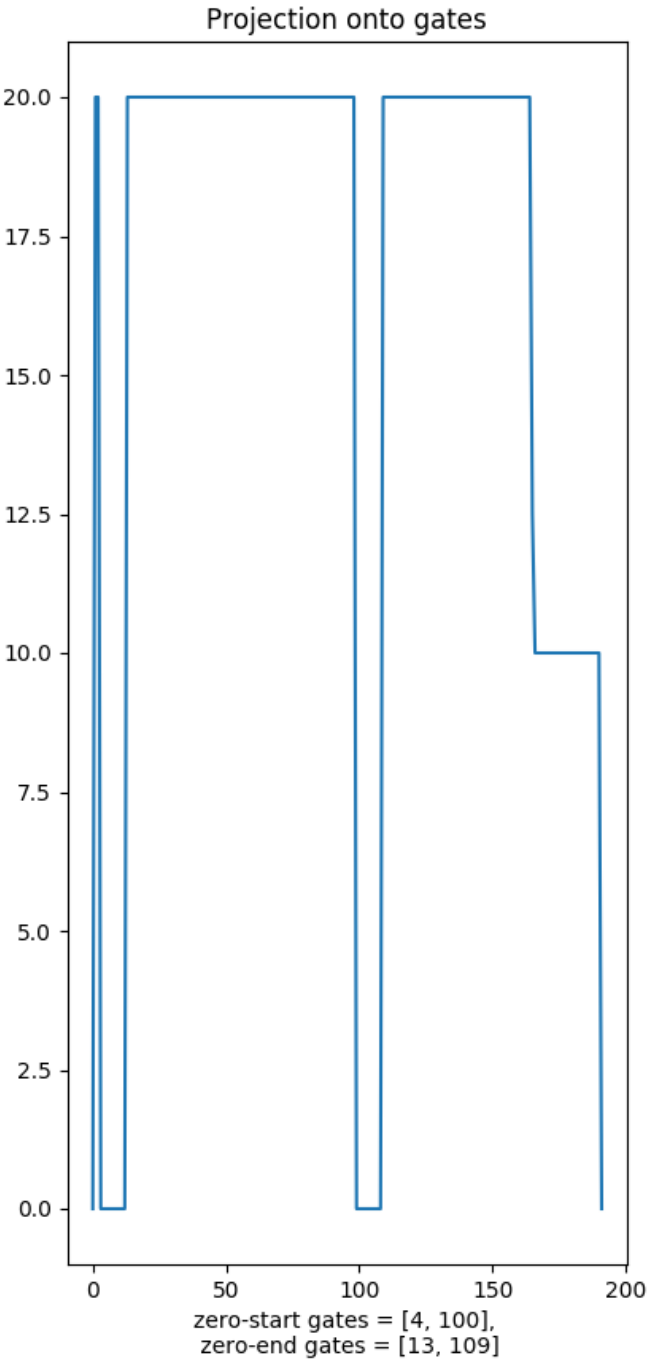
Inject-kick signal every 40ms or ~4000 revolution cycles
Period in gated mode = INJVFULL + INJVGATE = 1000 + 800 = 1800 revolution cycles

Backup slides

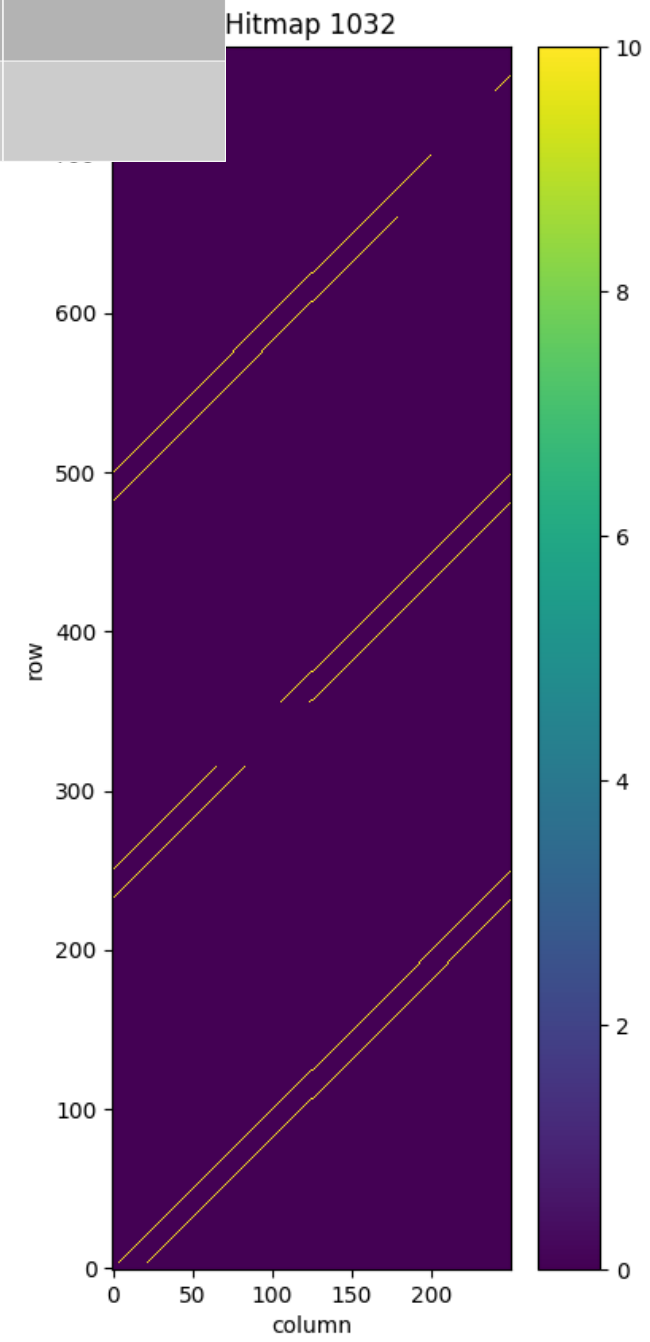
Test 1 backup slides

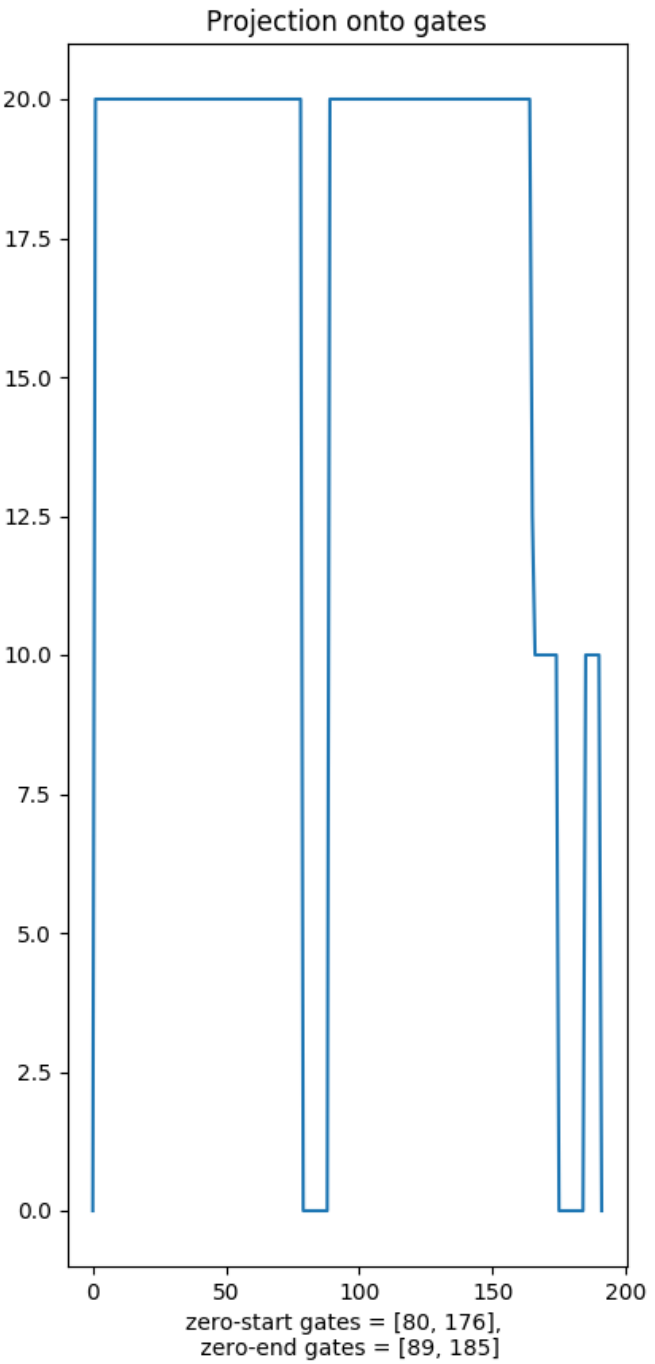
Input Gate-offset	Input Gate-length	DHP-latency	kicksub
0	10		



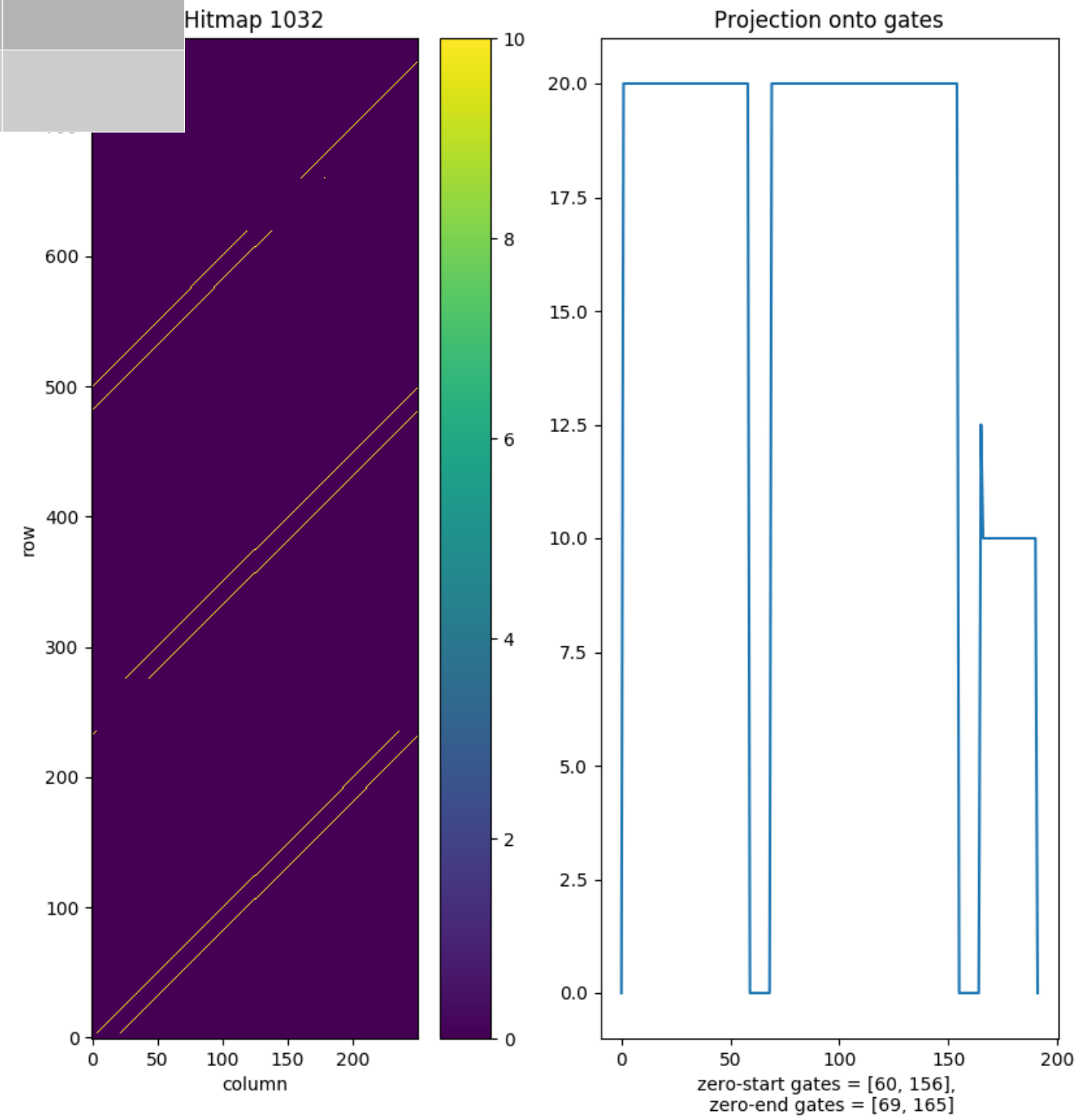


Input Gate-offset	Input Gate-length	DHP-latency	kicksub
20	10		

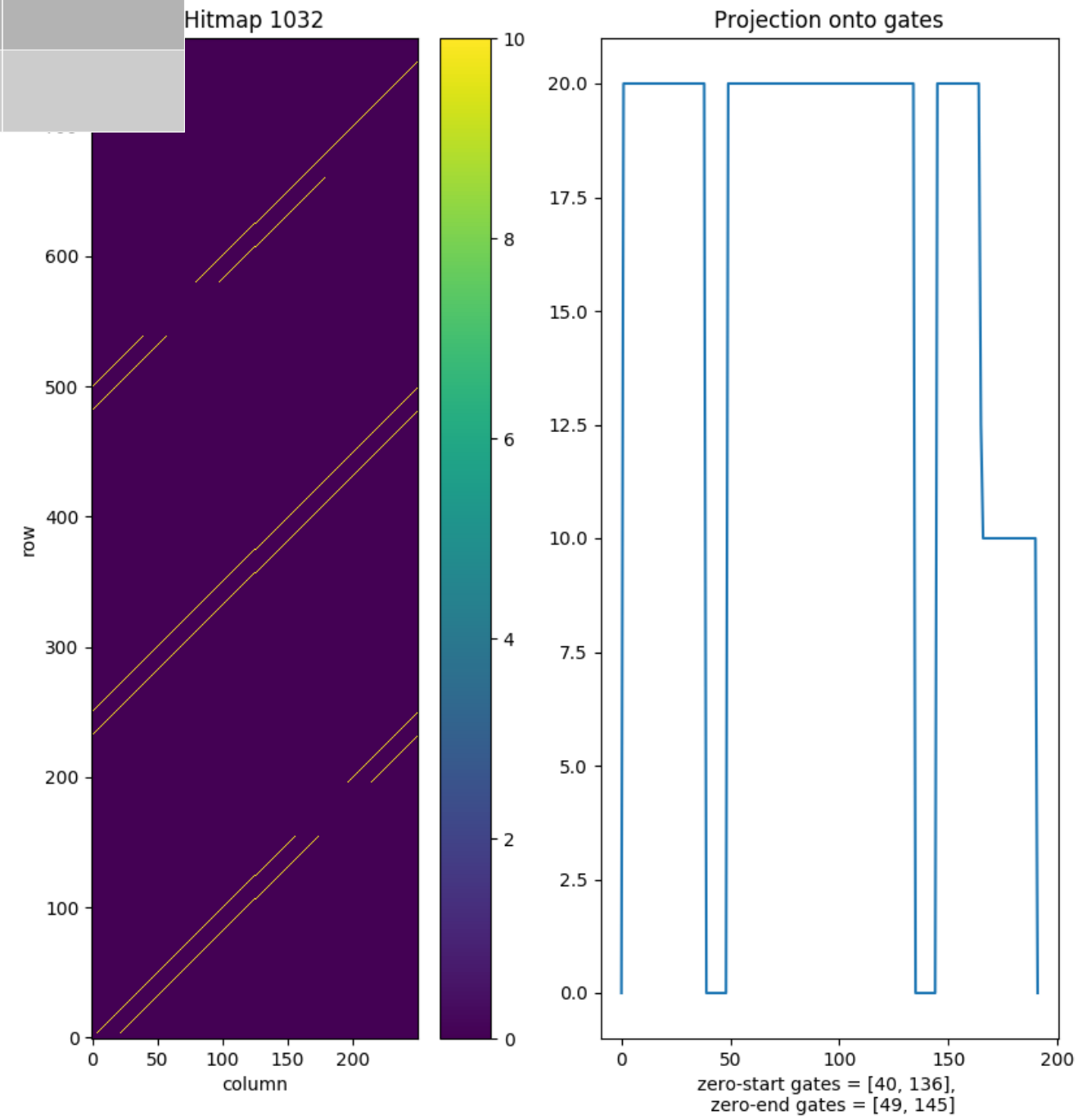




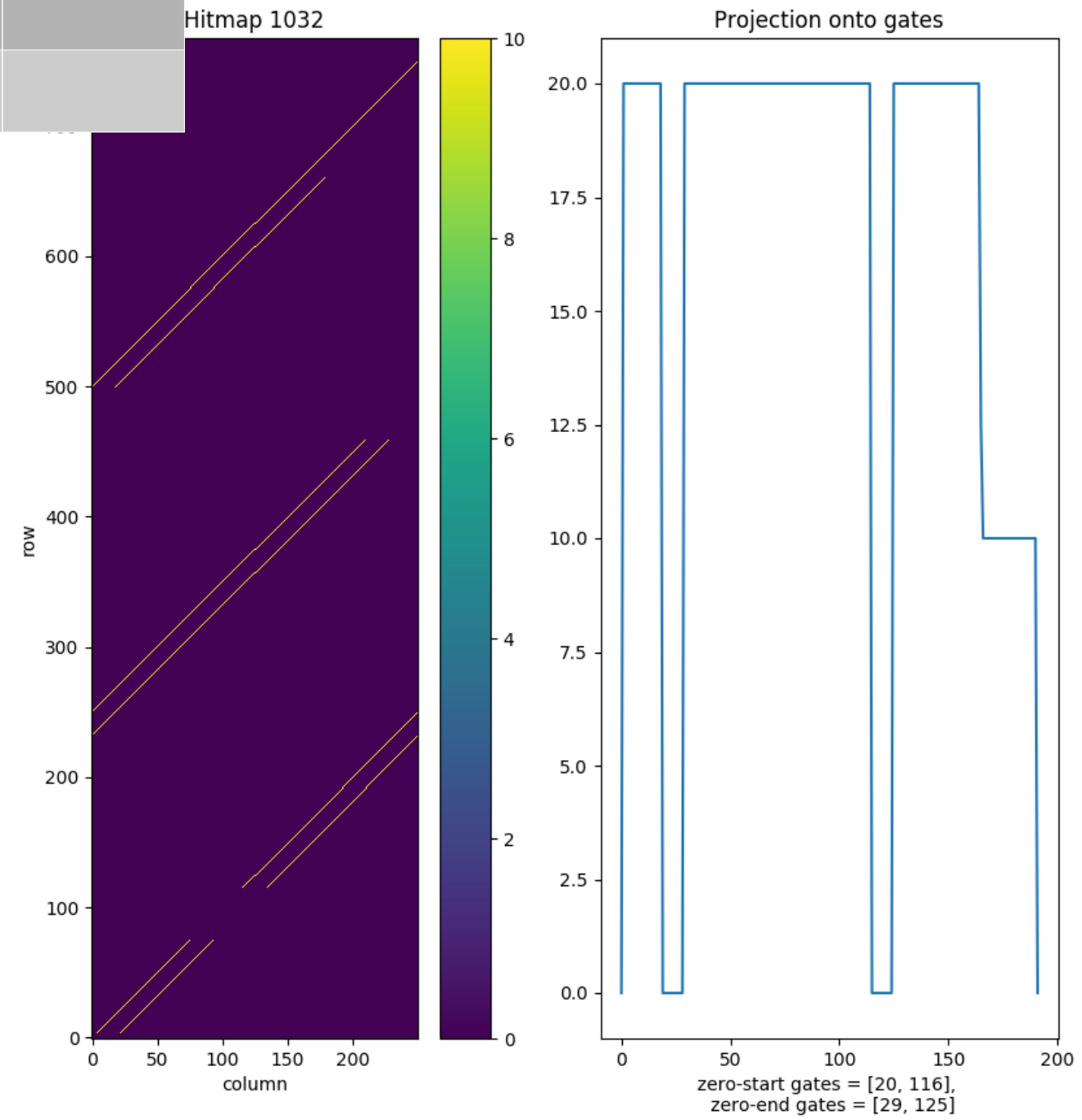
Input Gate-offset	Input Gate-length	DHP-latency	kicksub
40	10		



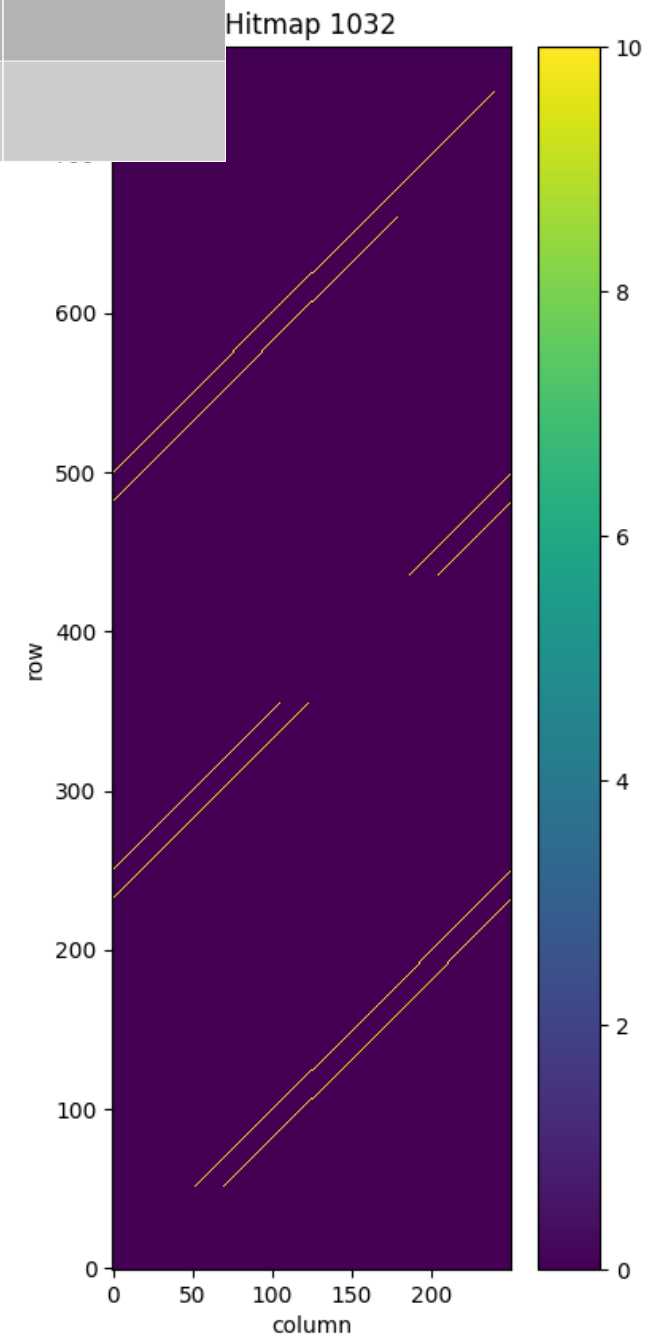
Input Gate-offset	Input Gate-length	DHP-latency	kicksub
60	10		

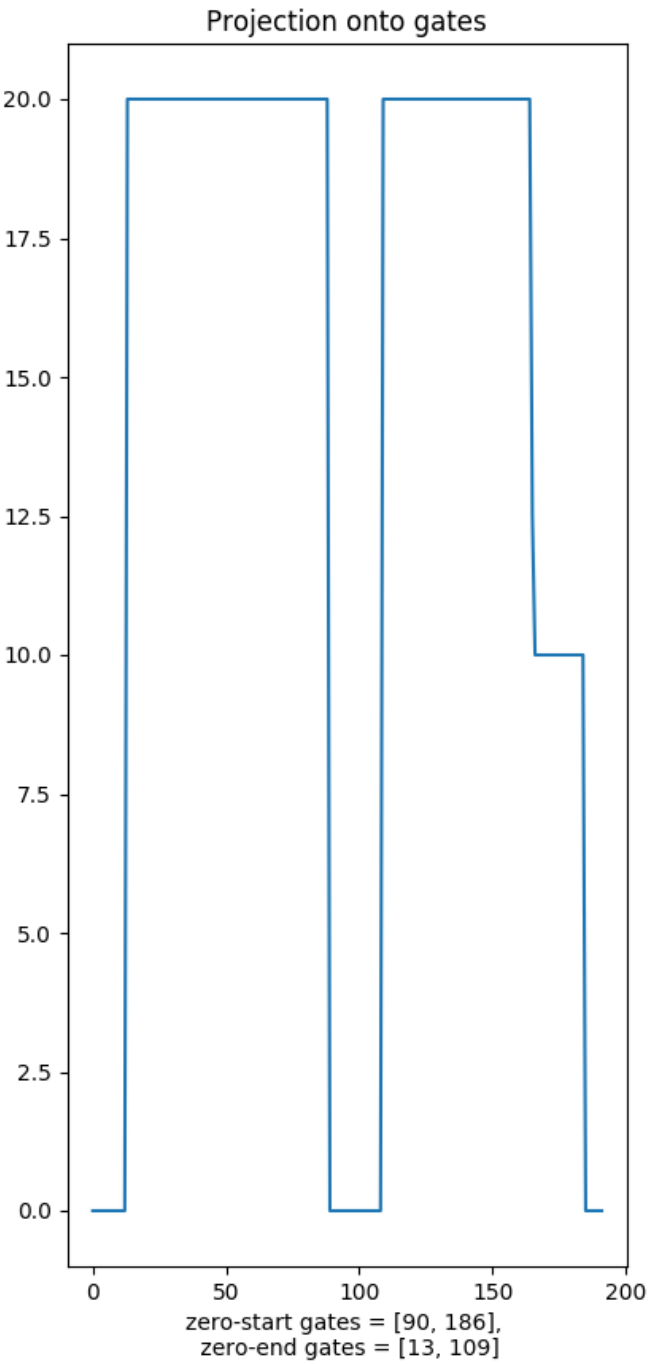


Input Gate-offset	Input Gate-length	DHP-latency	kicksub
80	10		

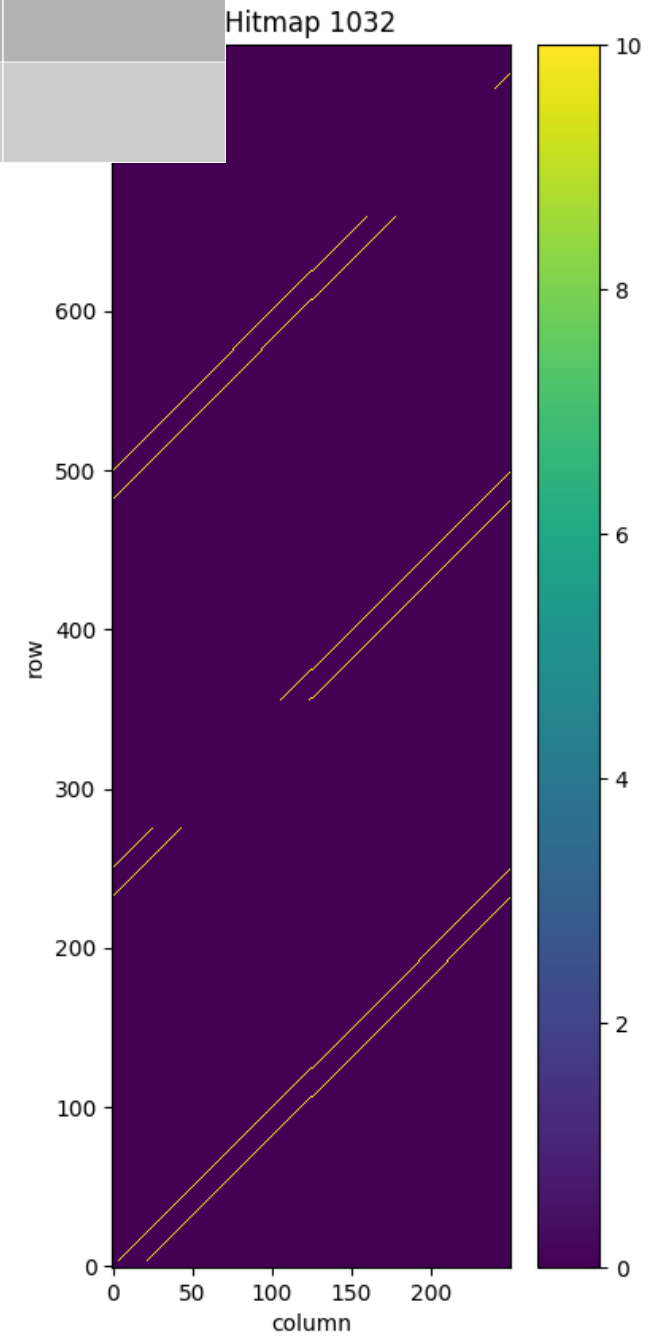


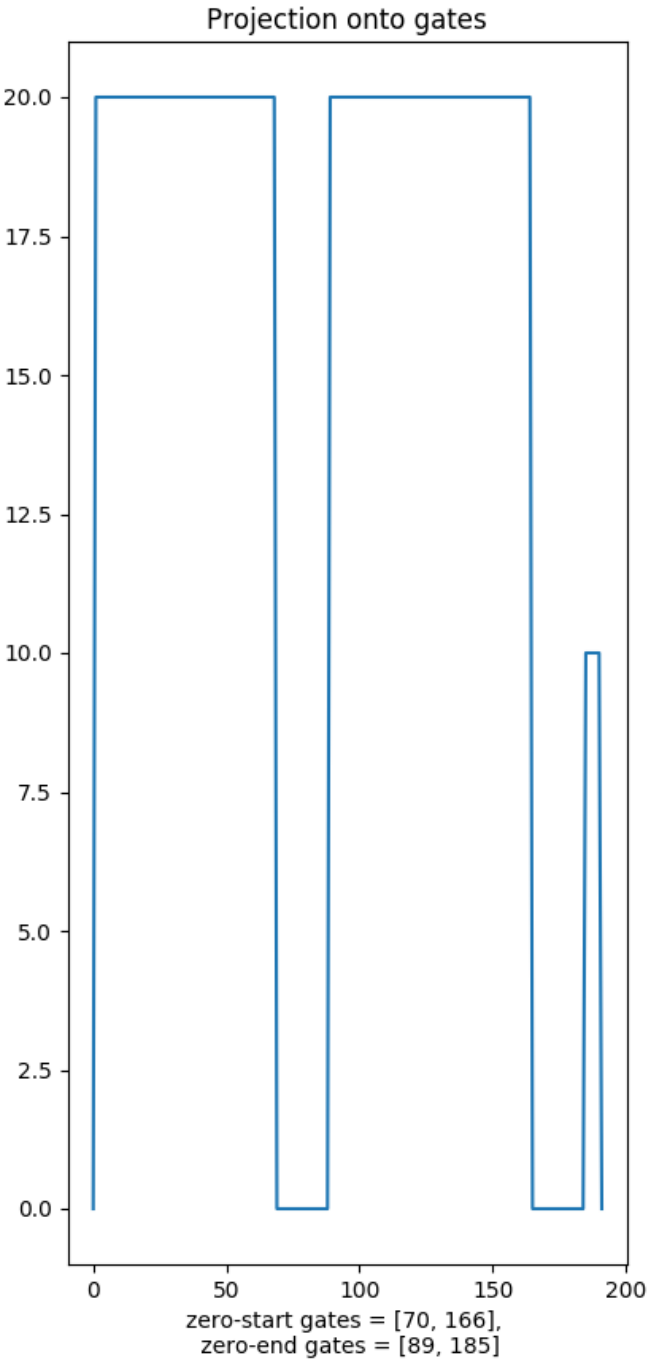
Input Gate-offset	Input Gate-length	DHP-latency	kicksub
0	20		



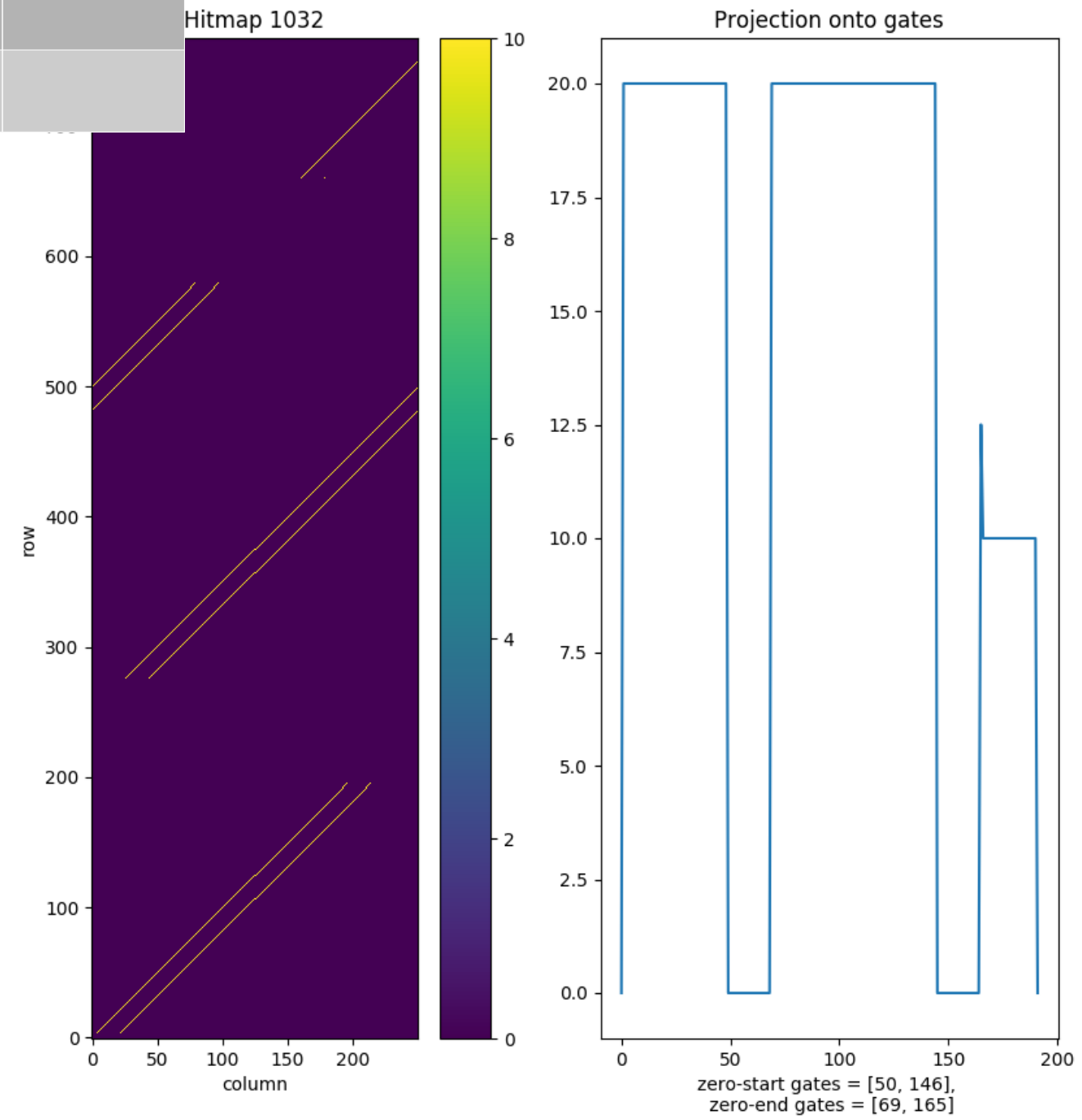


Input Gate-offset	Input Gate-length	DHP-latency	kicksub
20	20		

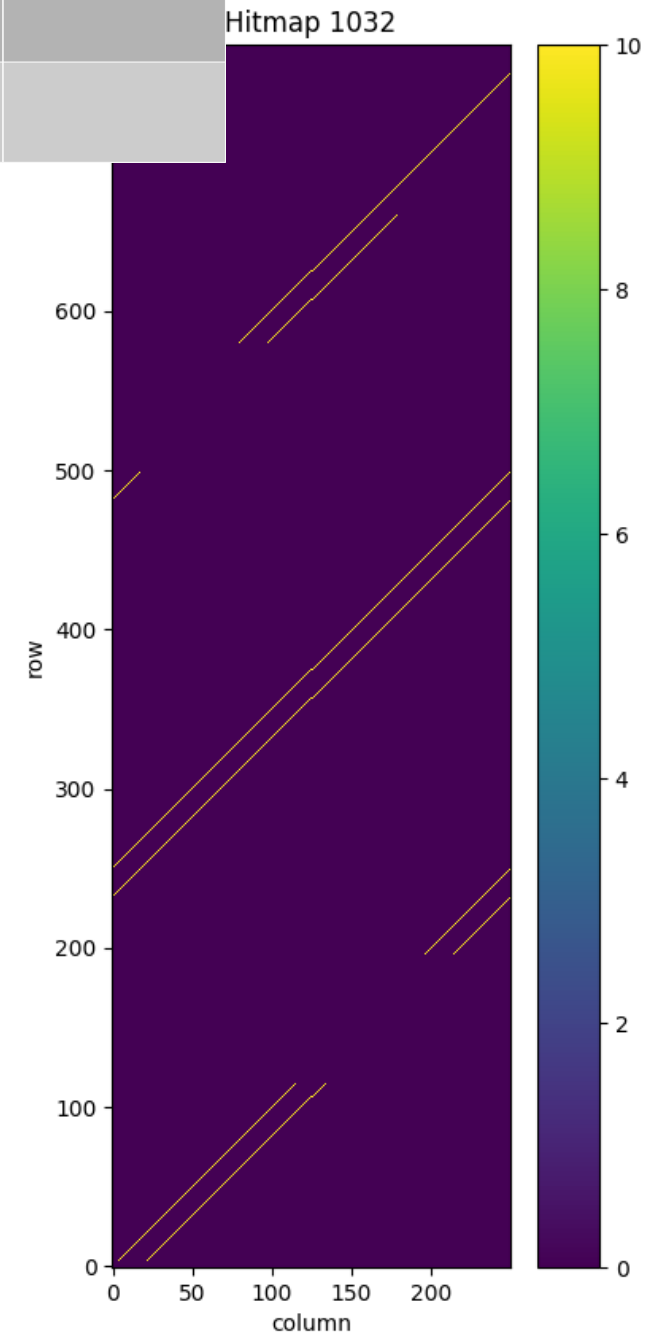


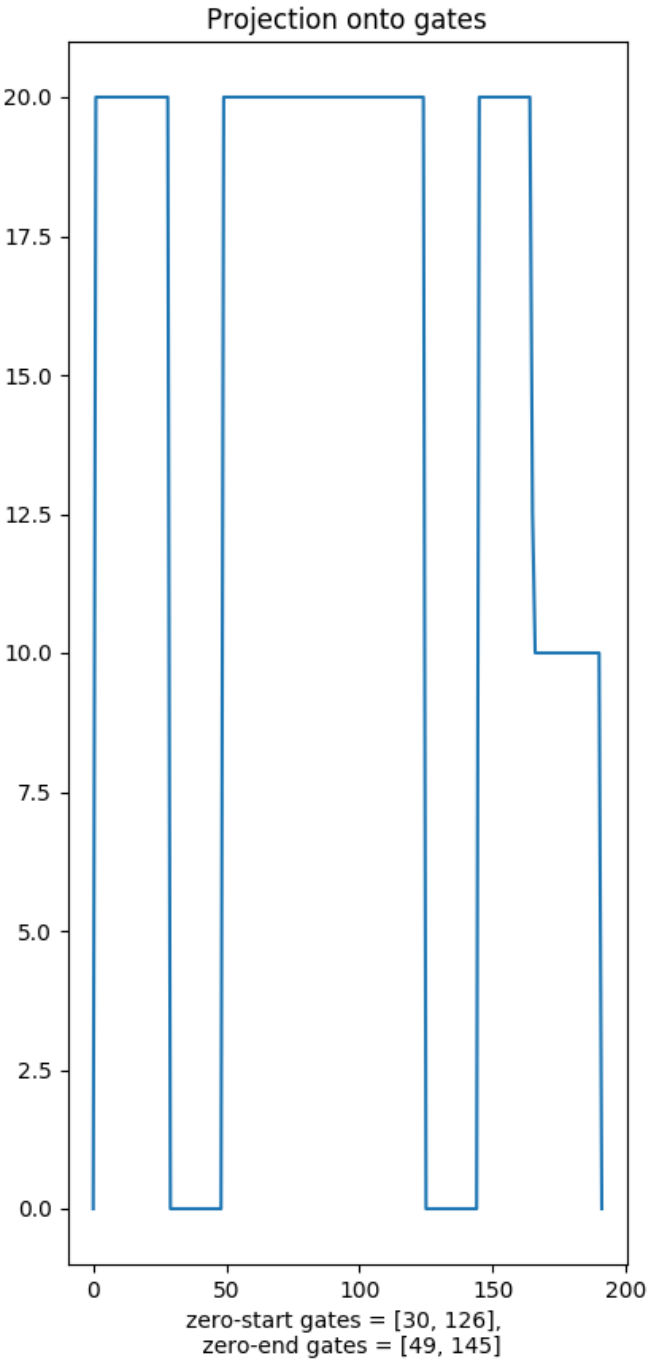


Input Gate-offset	Input Gate-length	DHP-latency	kicksub
40	20		

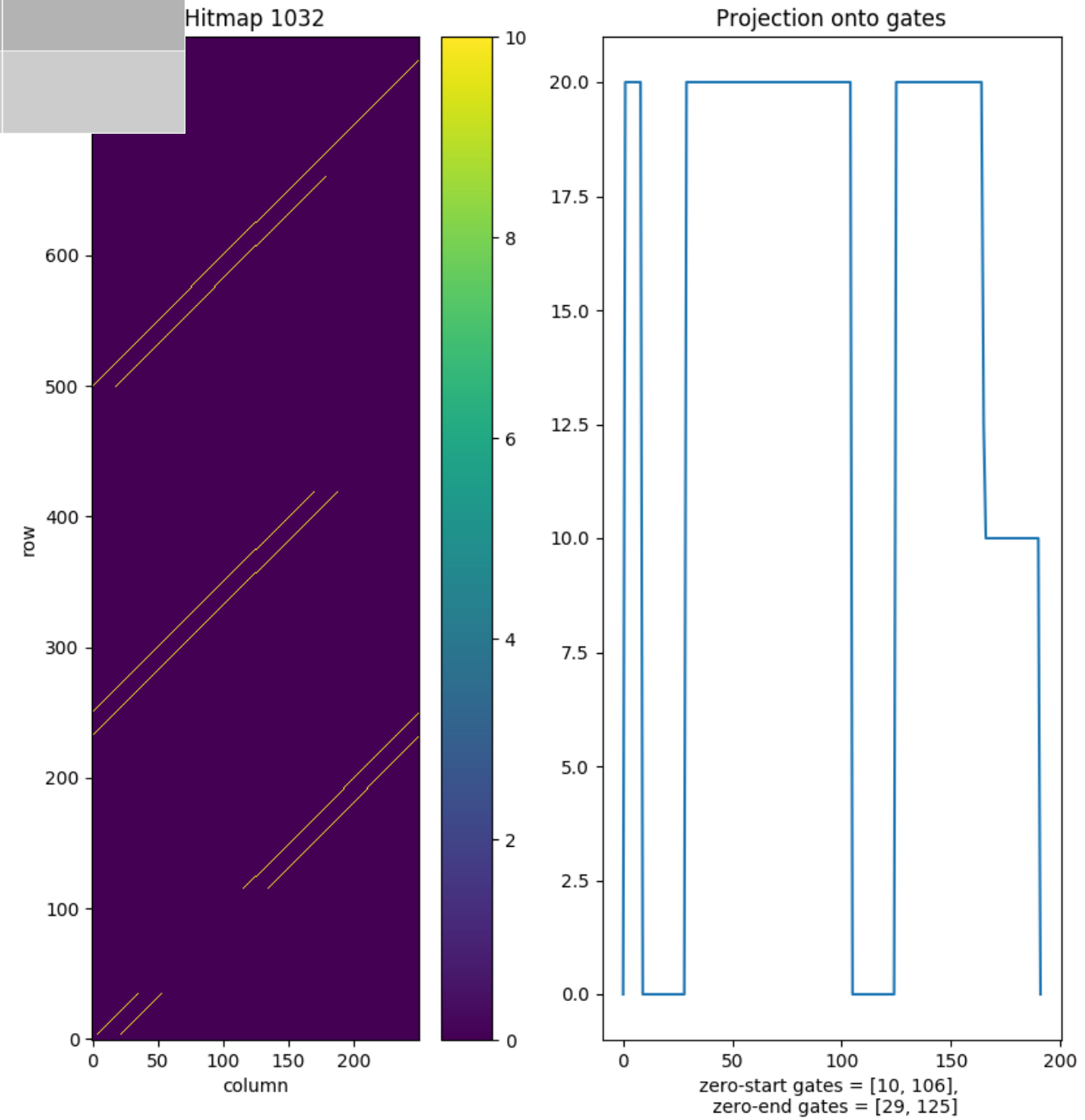


Input Gate-offset	Input Gate-length	DHP-latency	kicksub
60	20		

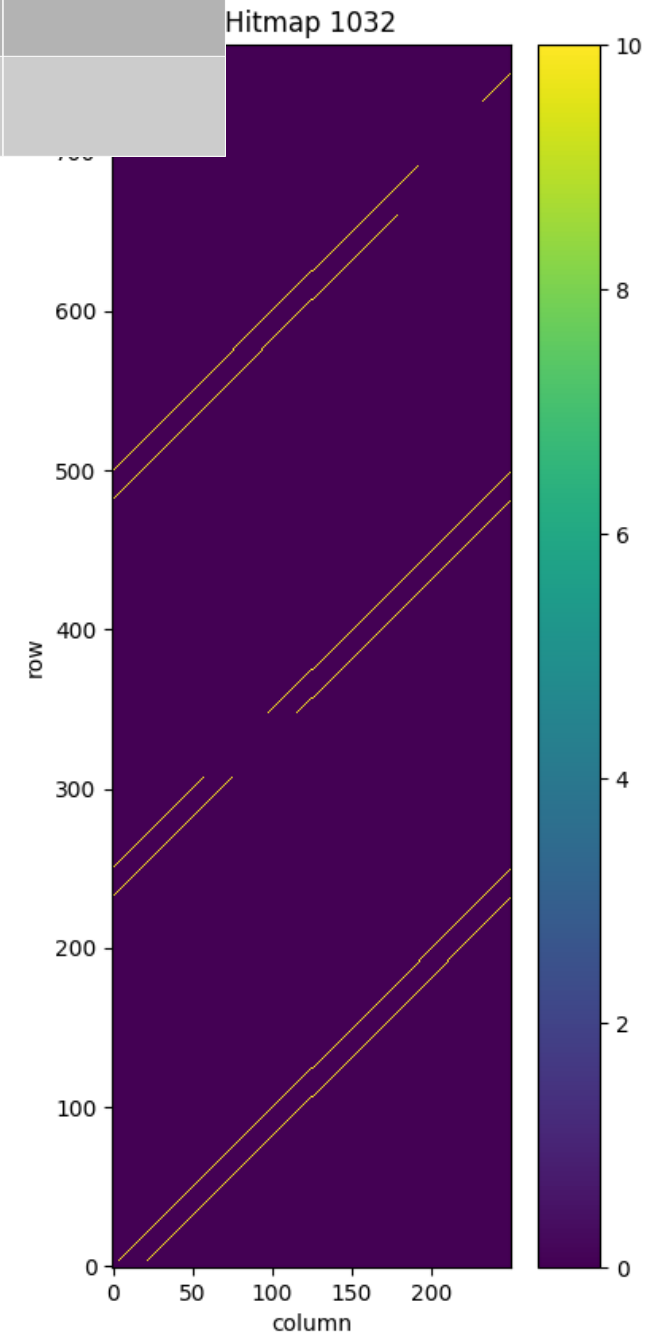


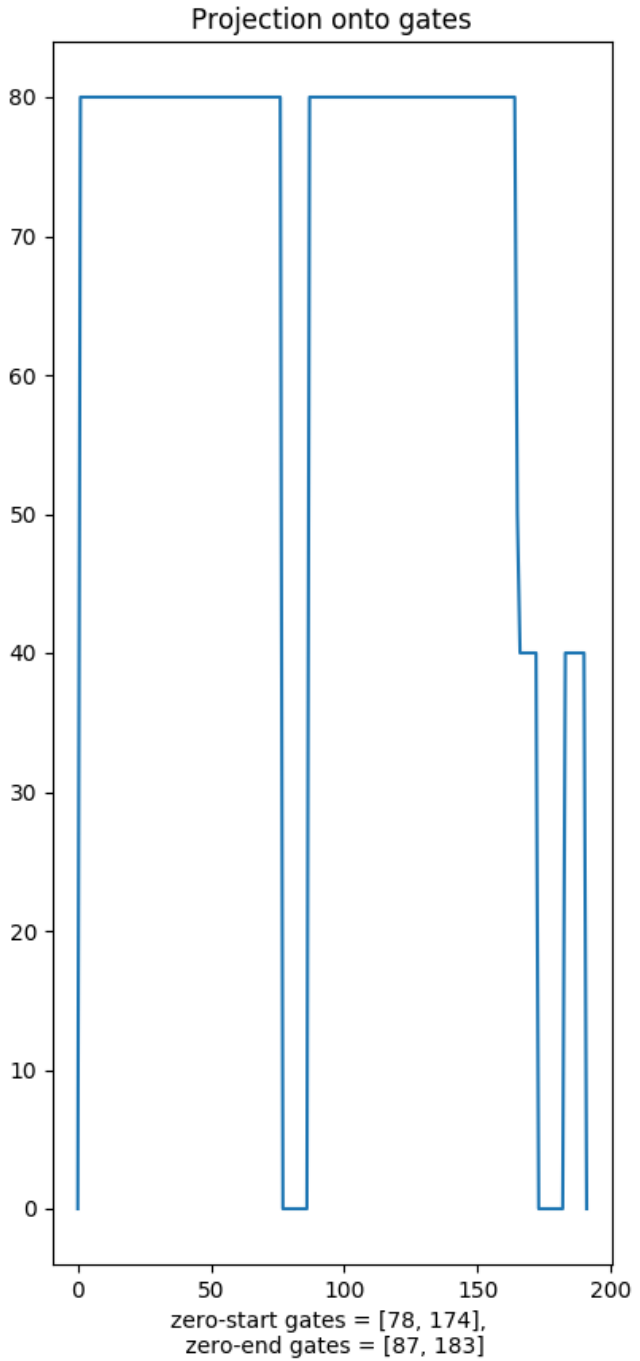


Input Gate-offset	Input Gate-length	DHP-latency	kicksub
80	20		

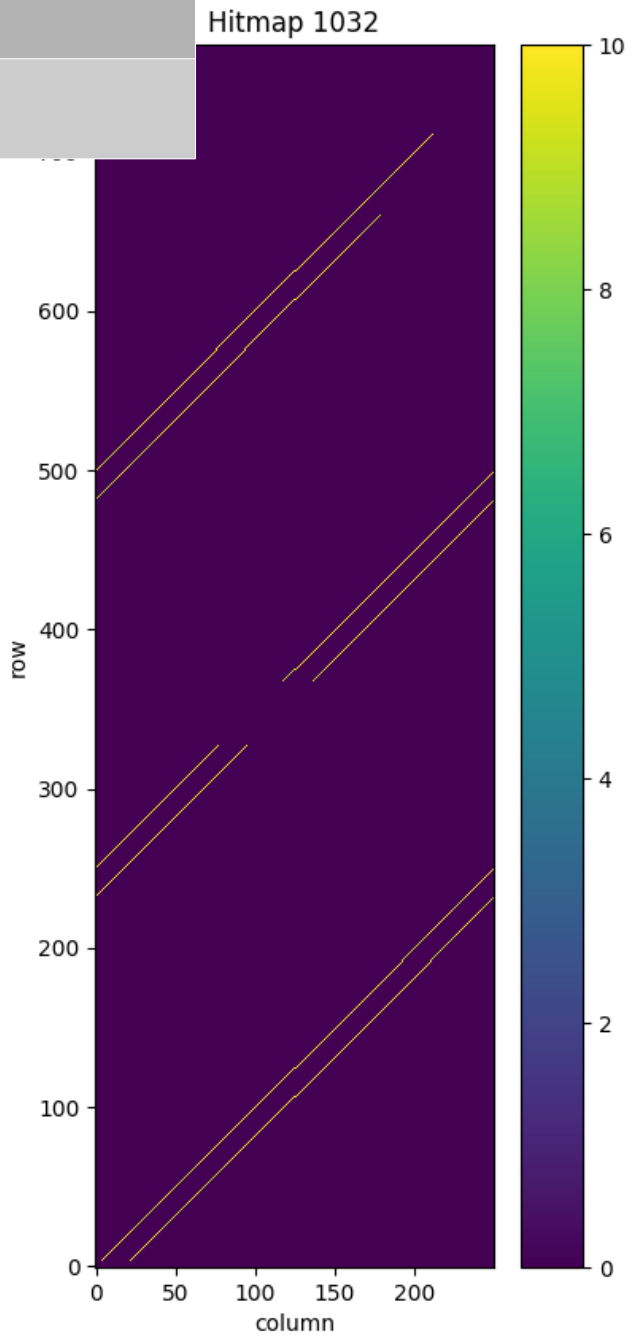


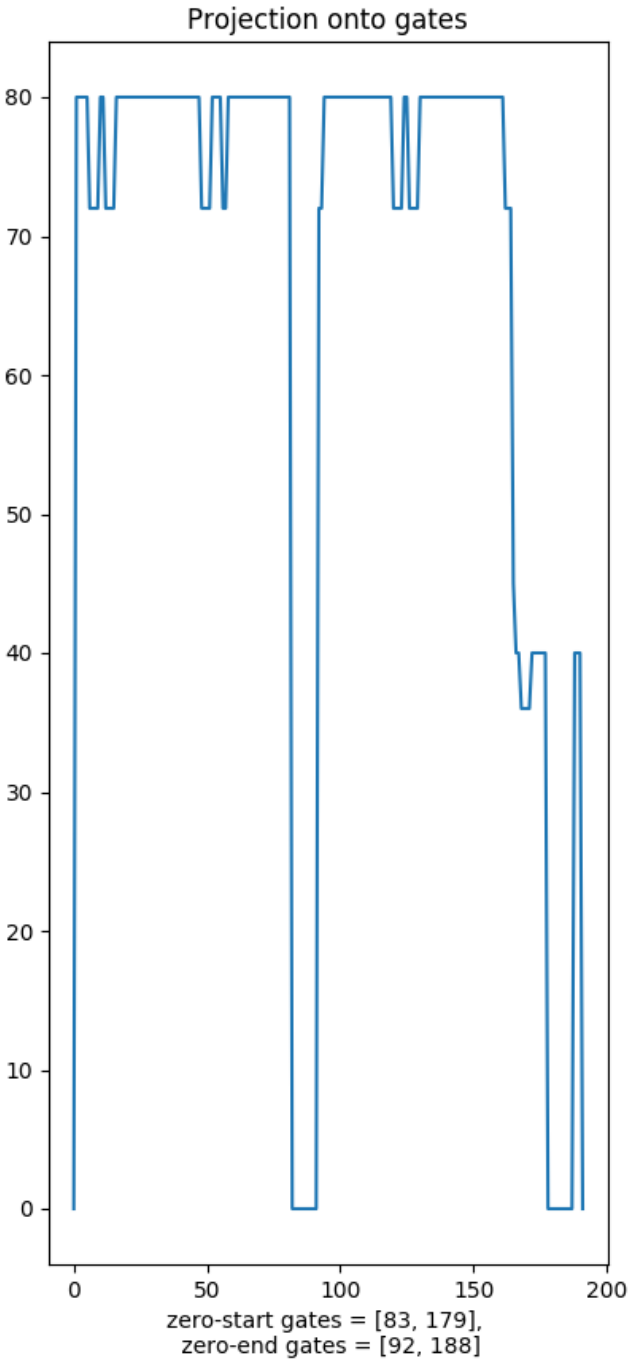
Input Gate-offset	Input Gate-length	DHP-latency	kicksub
22	10	5	



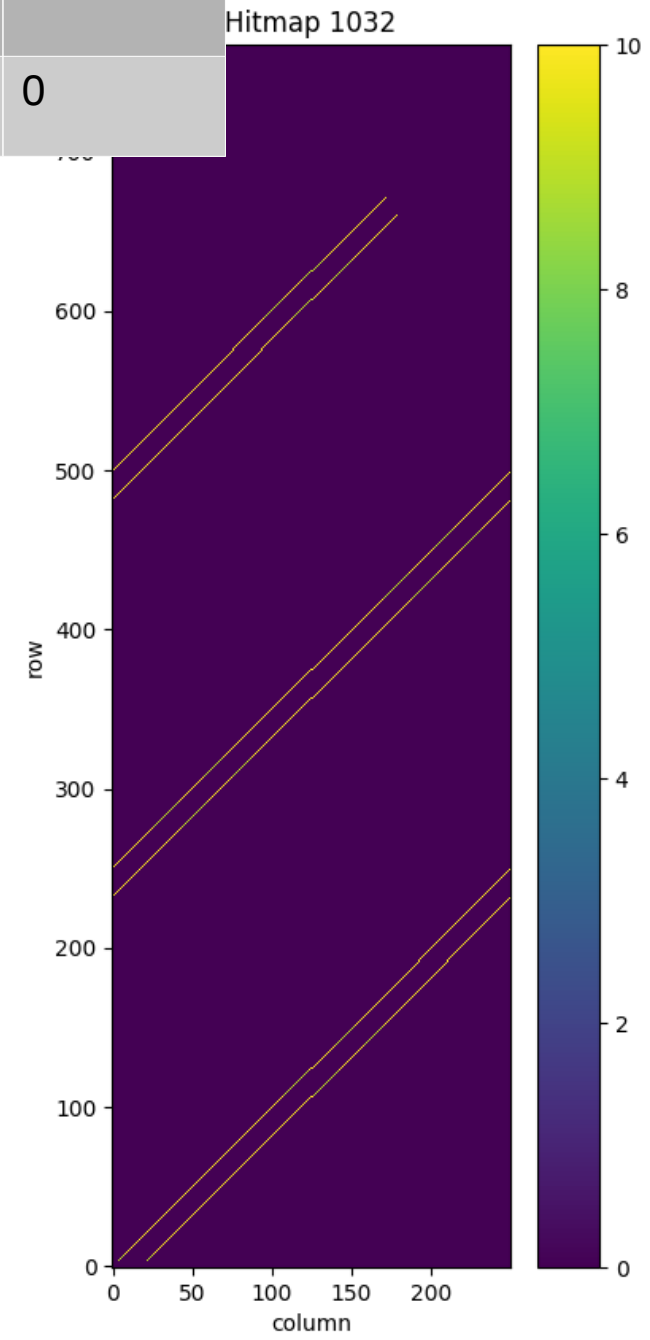


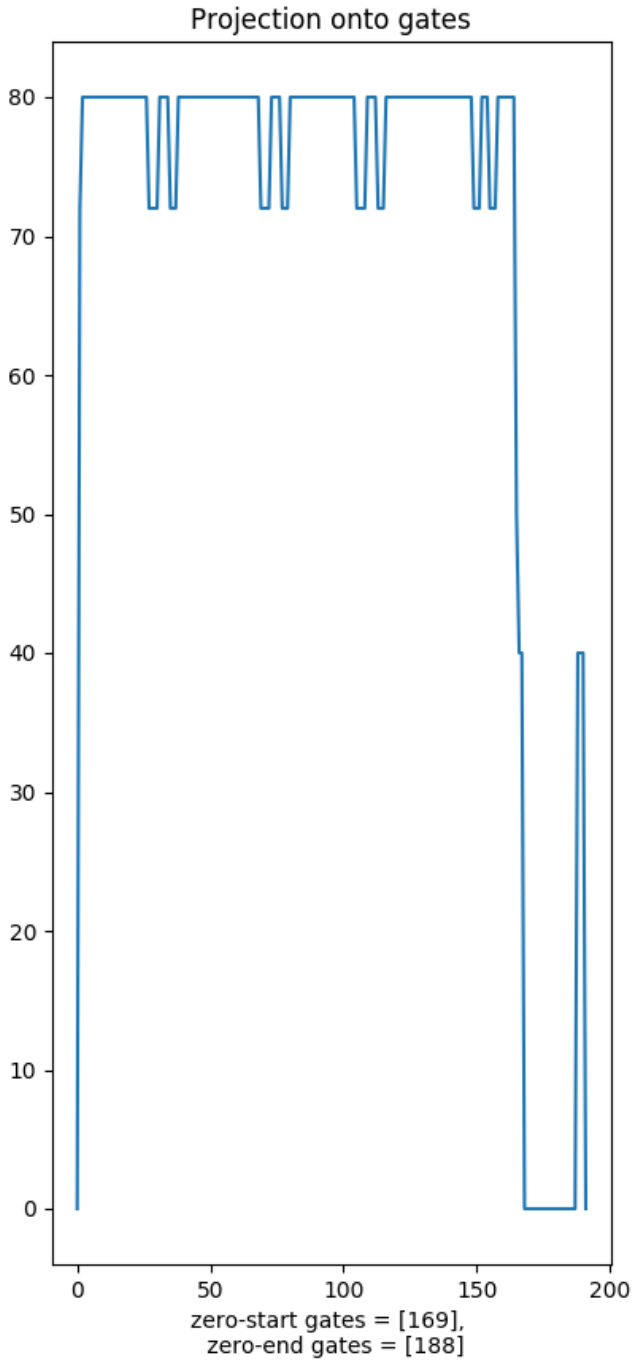
Input Gate-offset	Input Gate-length	DHP-latency	kicksub
22	10	10	



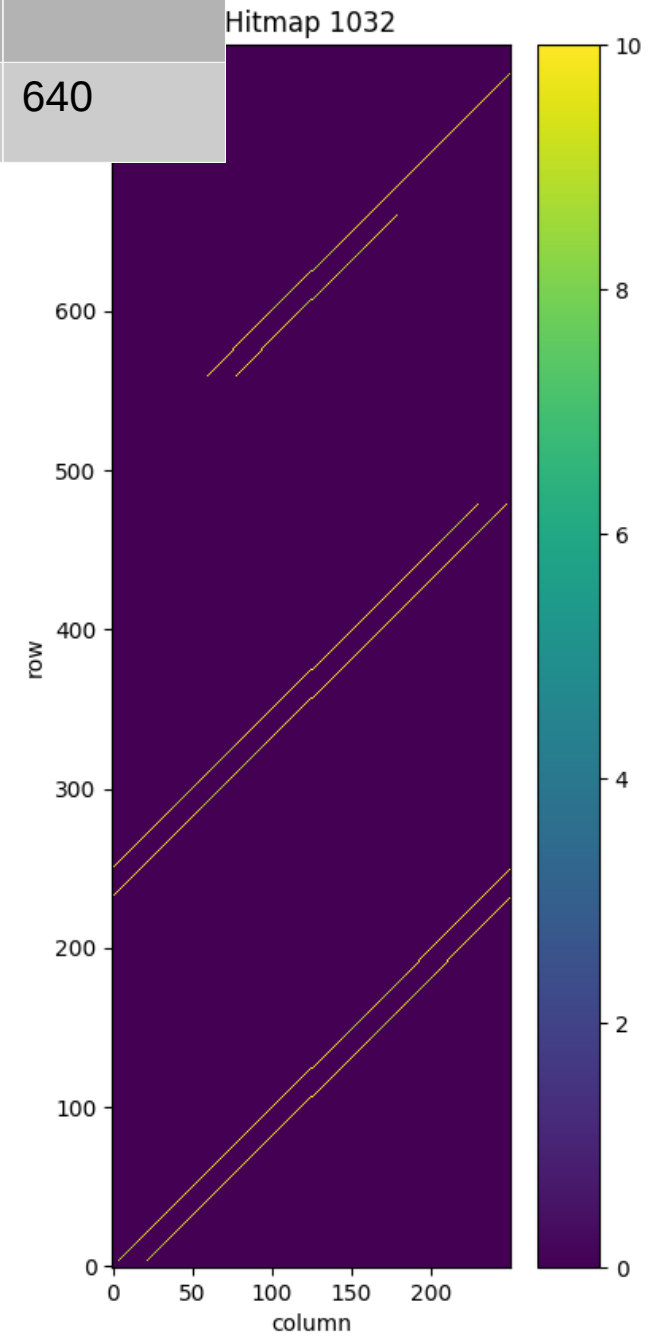


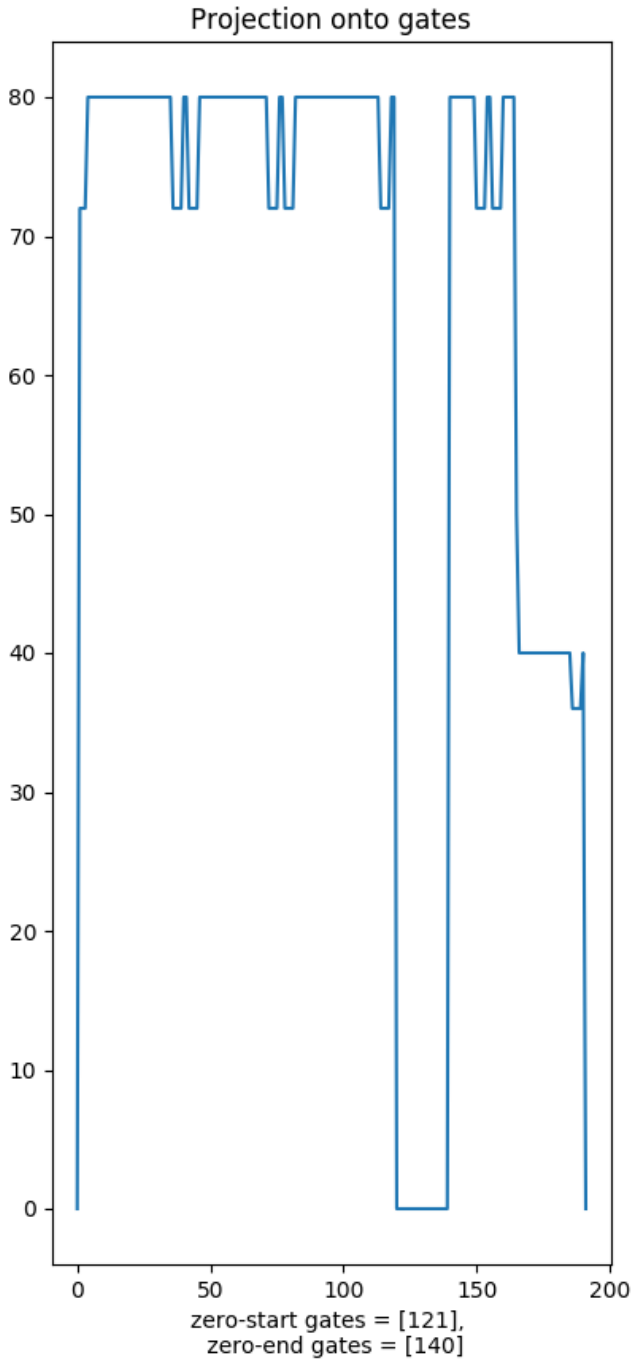
Input Gate-offset	Input Gate-length	DHP-latency	kicksub
22	20	10	0



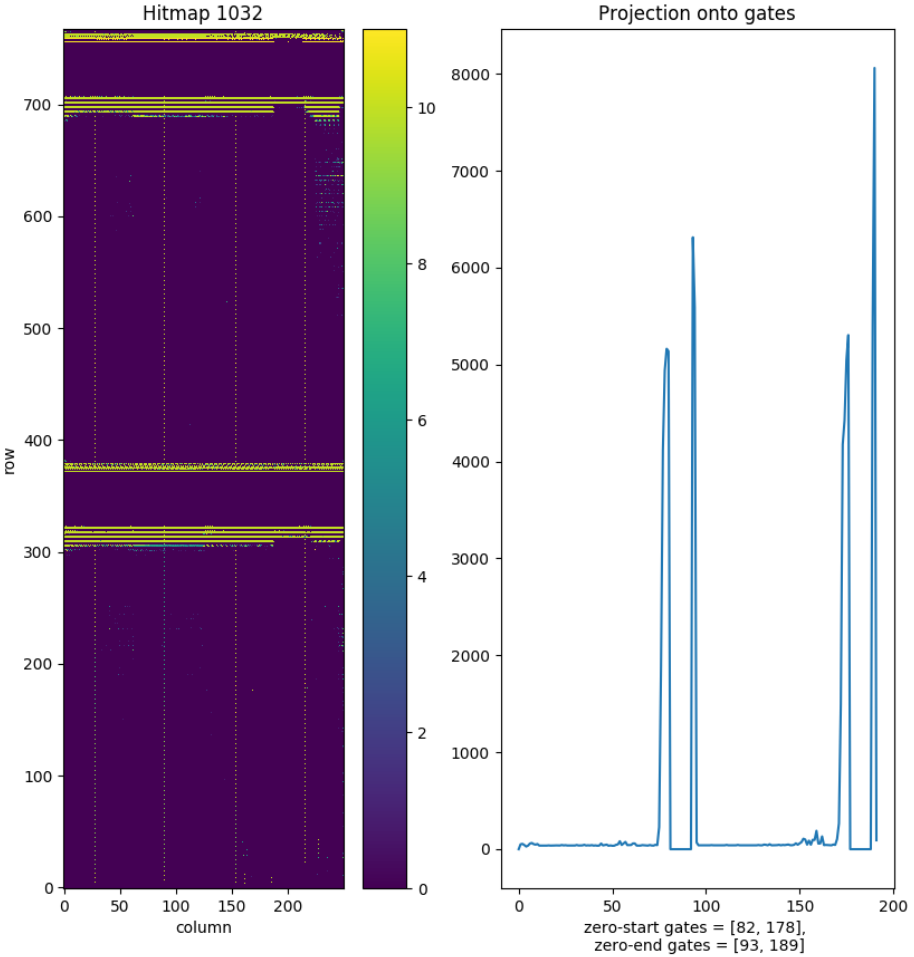


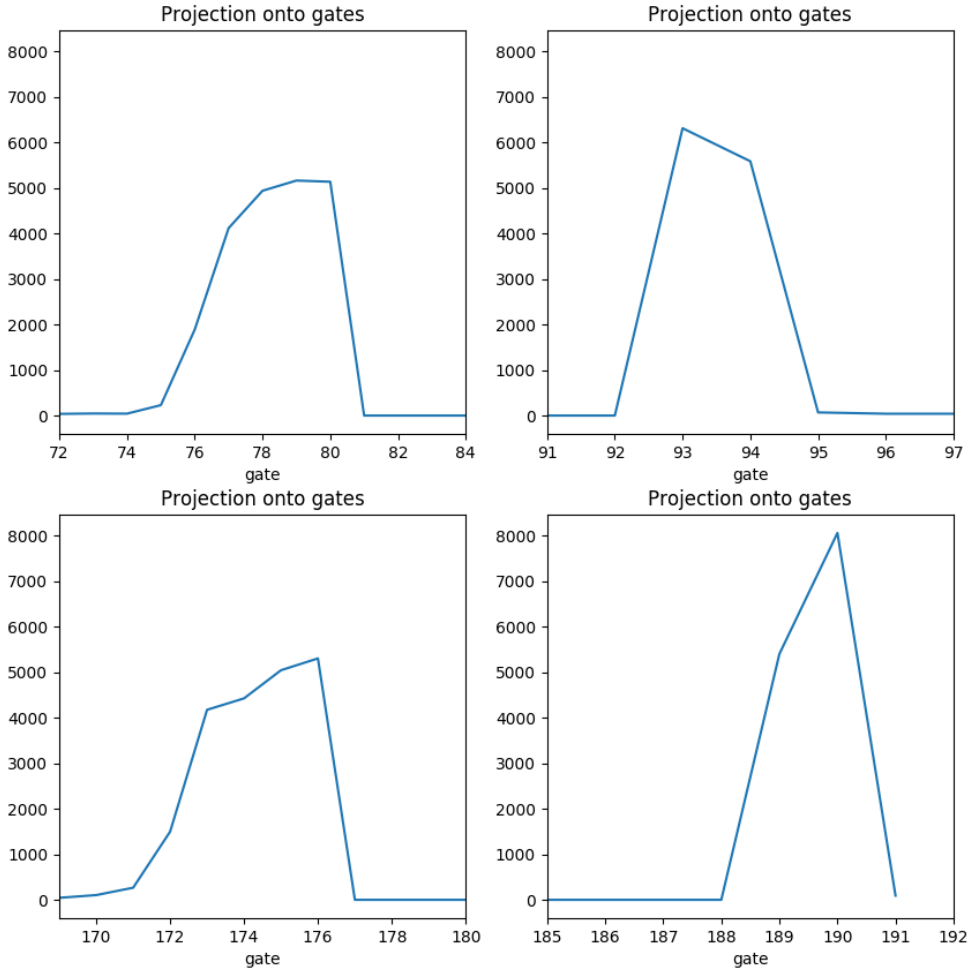
Input Gate-offset	Input Gate-length	DHP-latency	kicksub
22	20	10	640



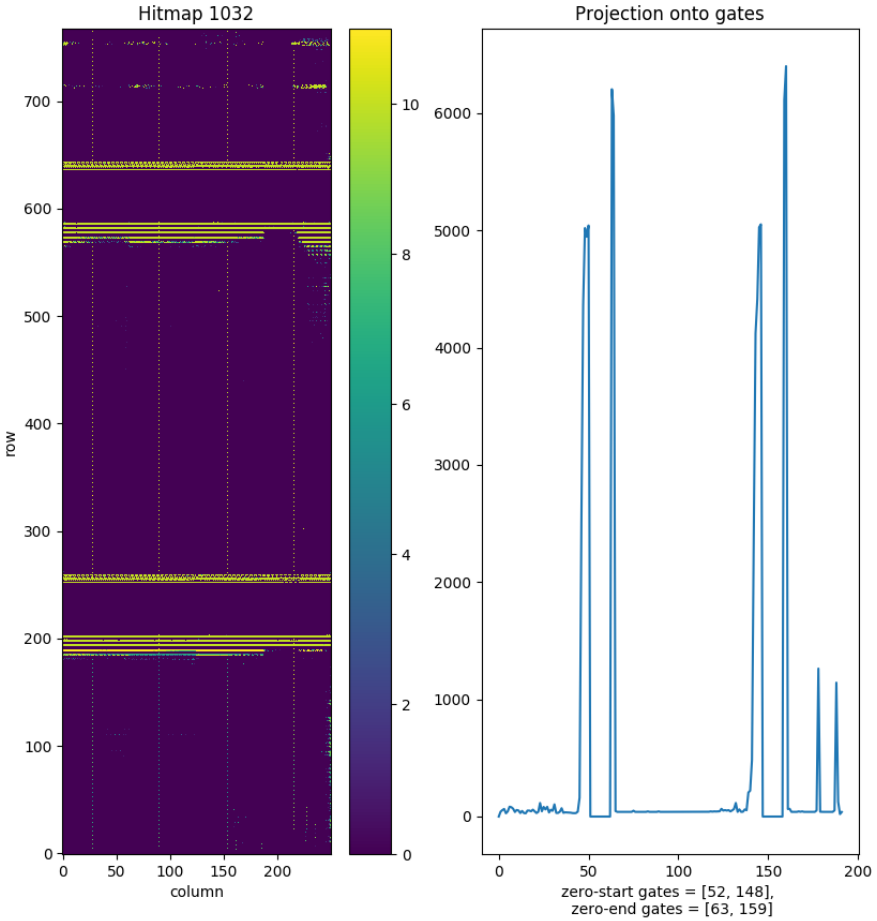


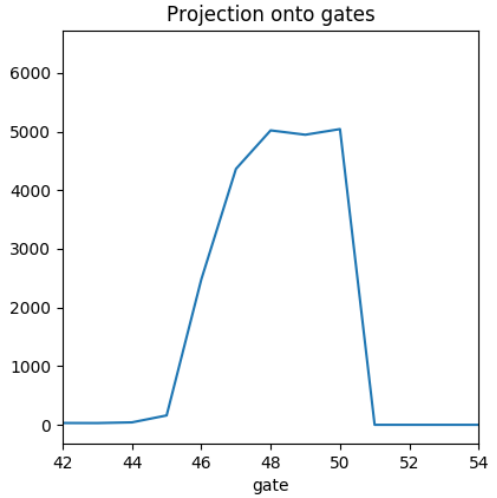
Test 2 backup slides

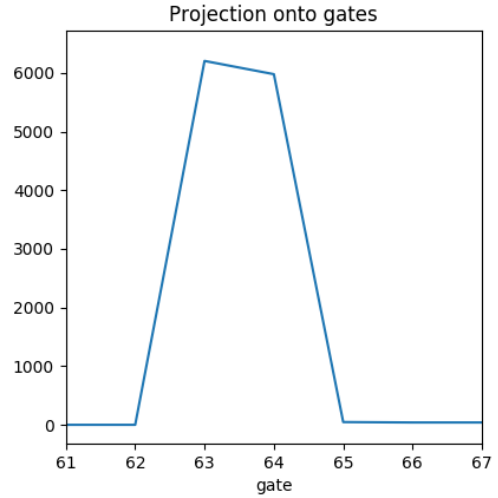


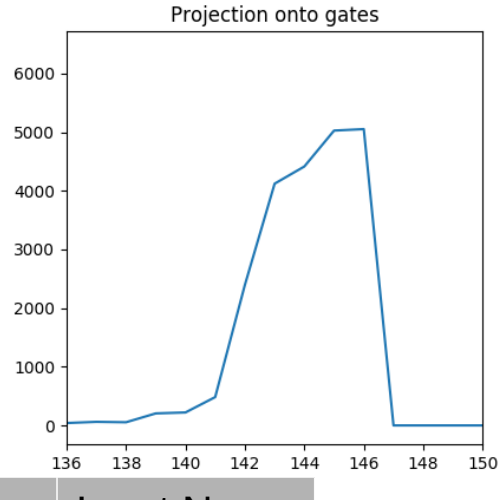


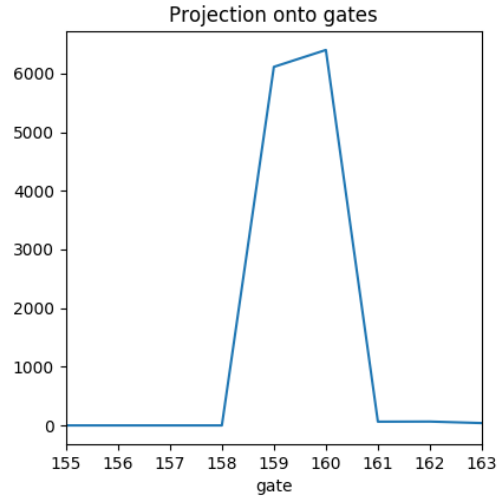
Input Gate-offset	Input Gate-length	Input No-trigger-offset	Input No-trigger-length
0	10	12	12



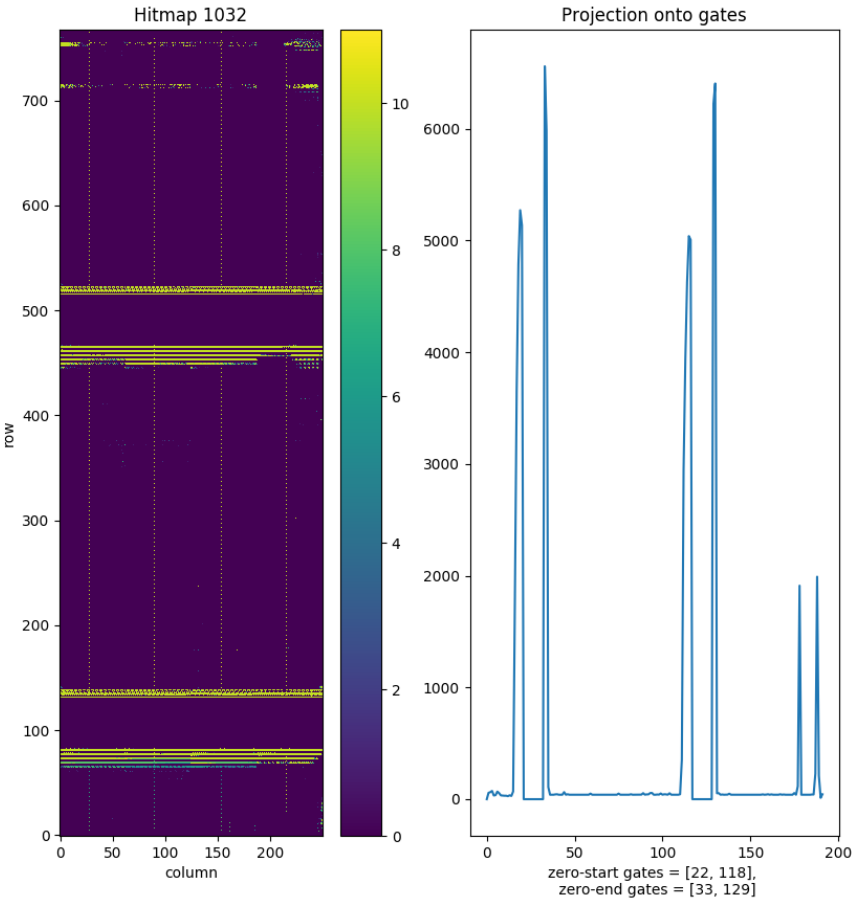


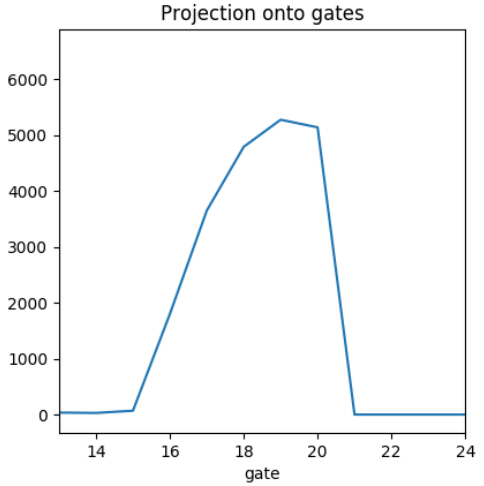


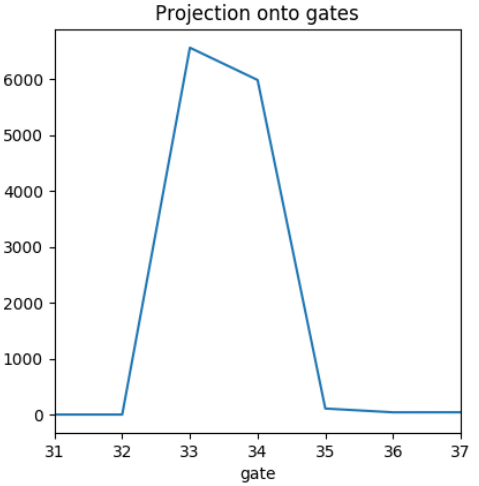


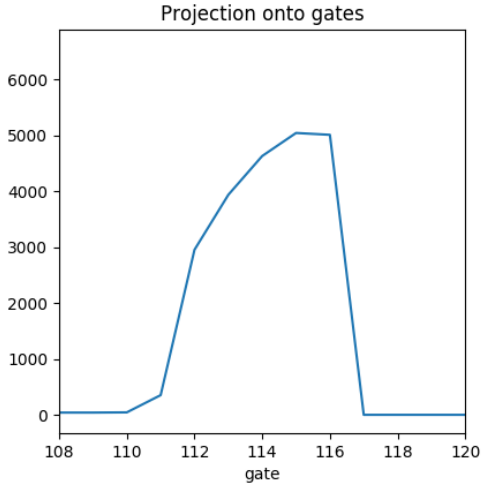


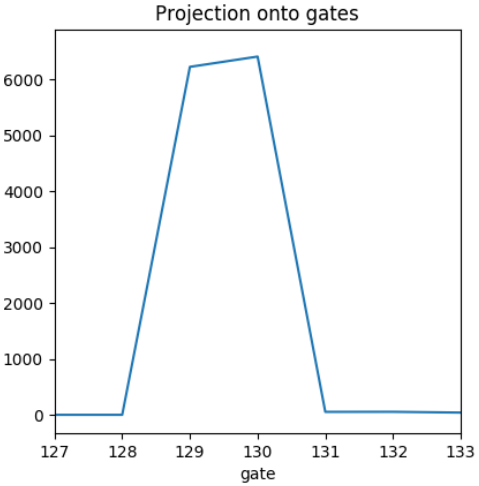
Input Gate-offset	Input Gate-length	Input No-trigger-offset	Input No-trigger-length
30	10	42	12



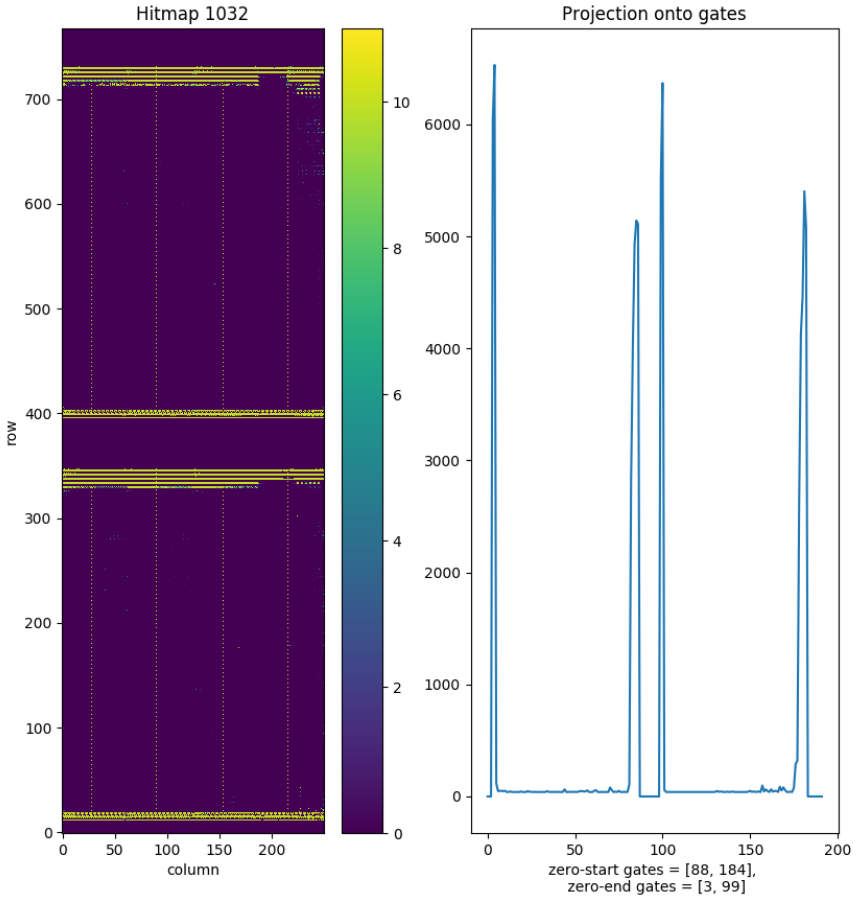


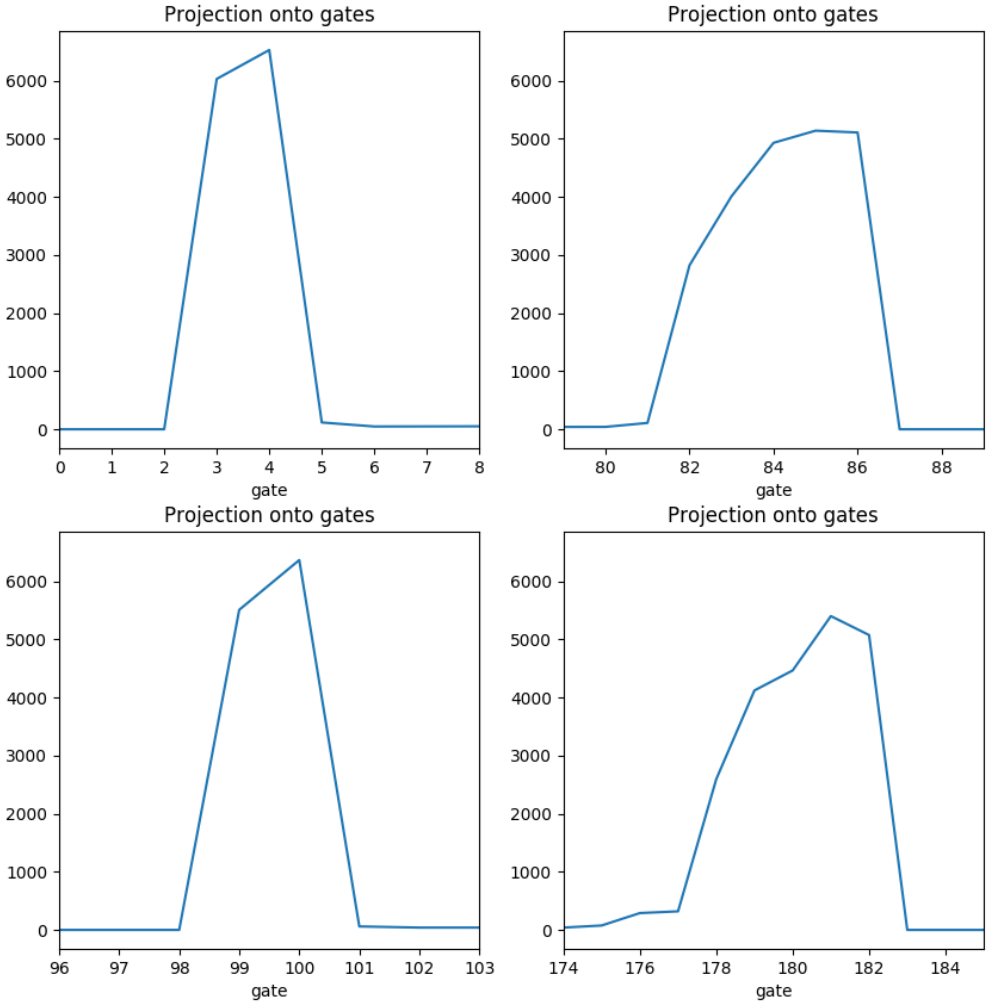




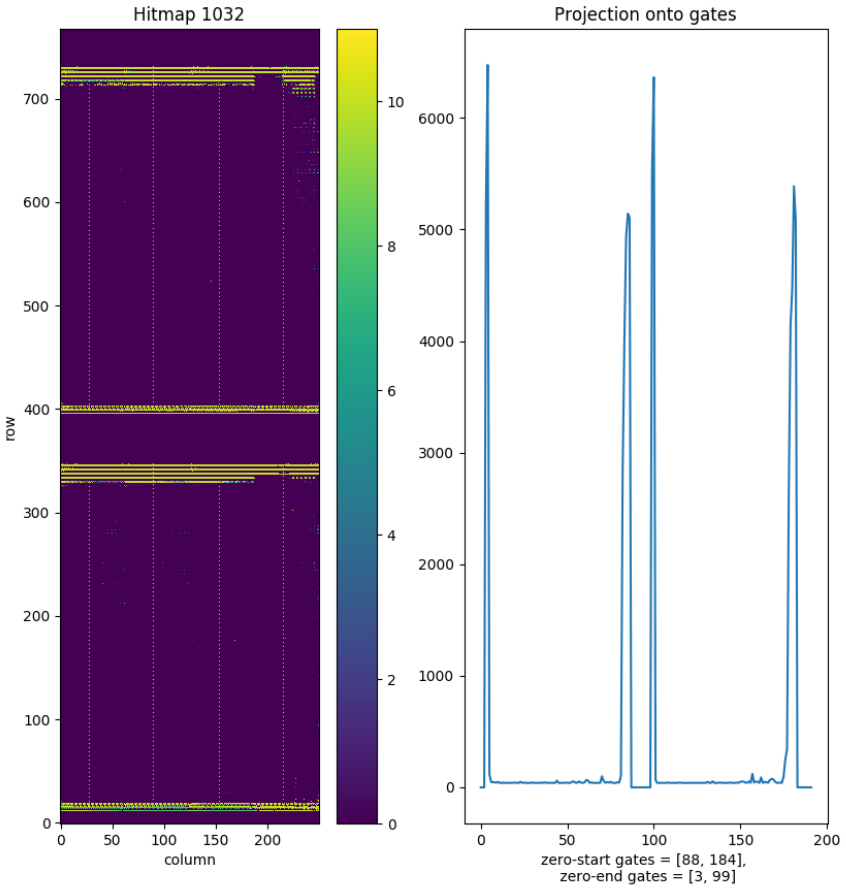


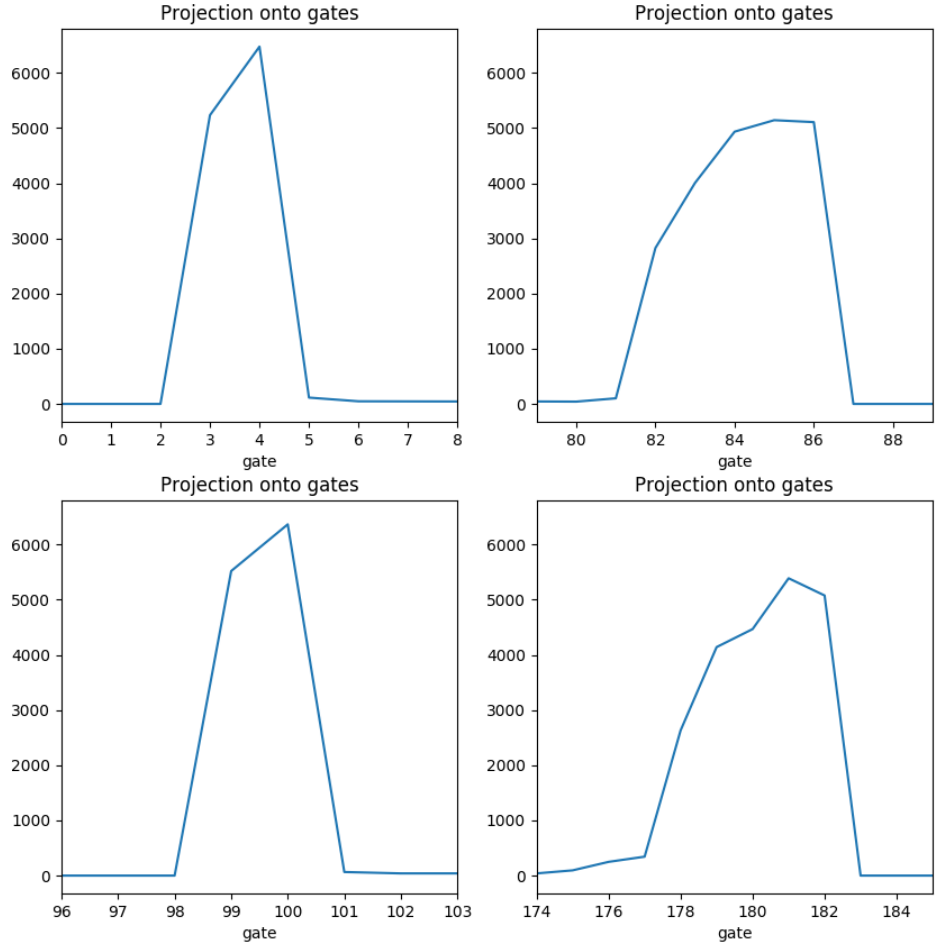
Input Gate-offset	Input Gate-length	Input No-trigger-offset	Input No-trigger -length
60	10	72	12



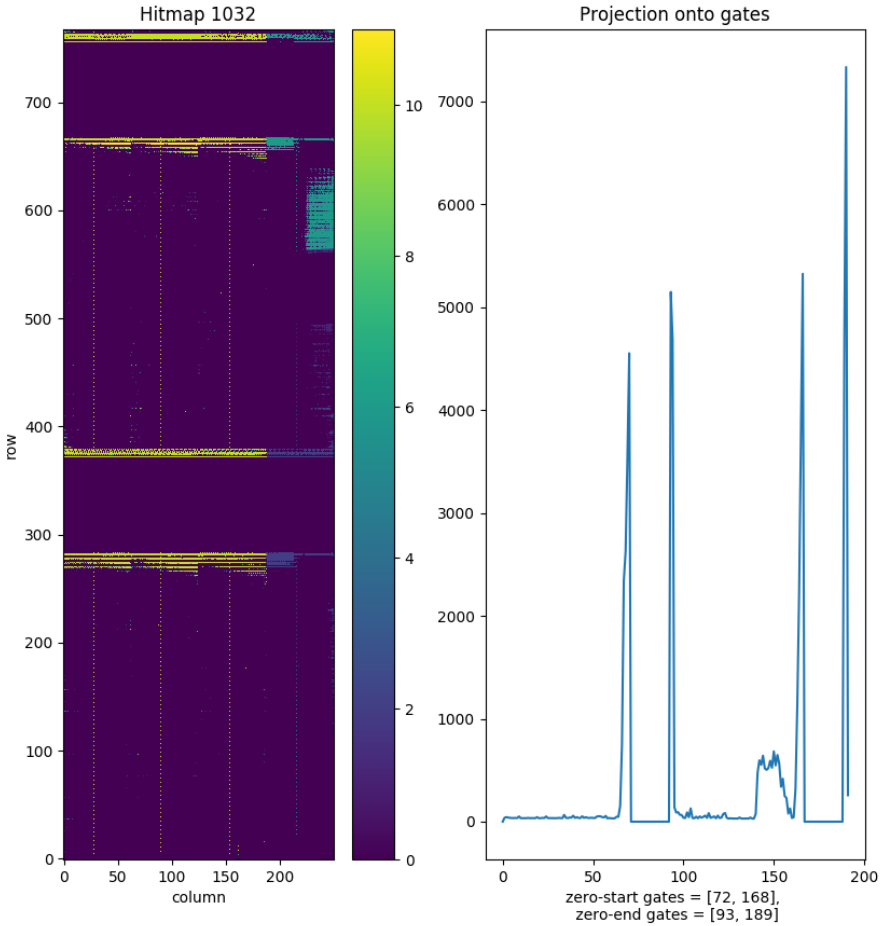


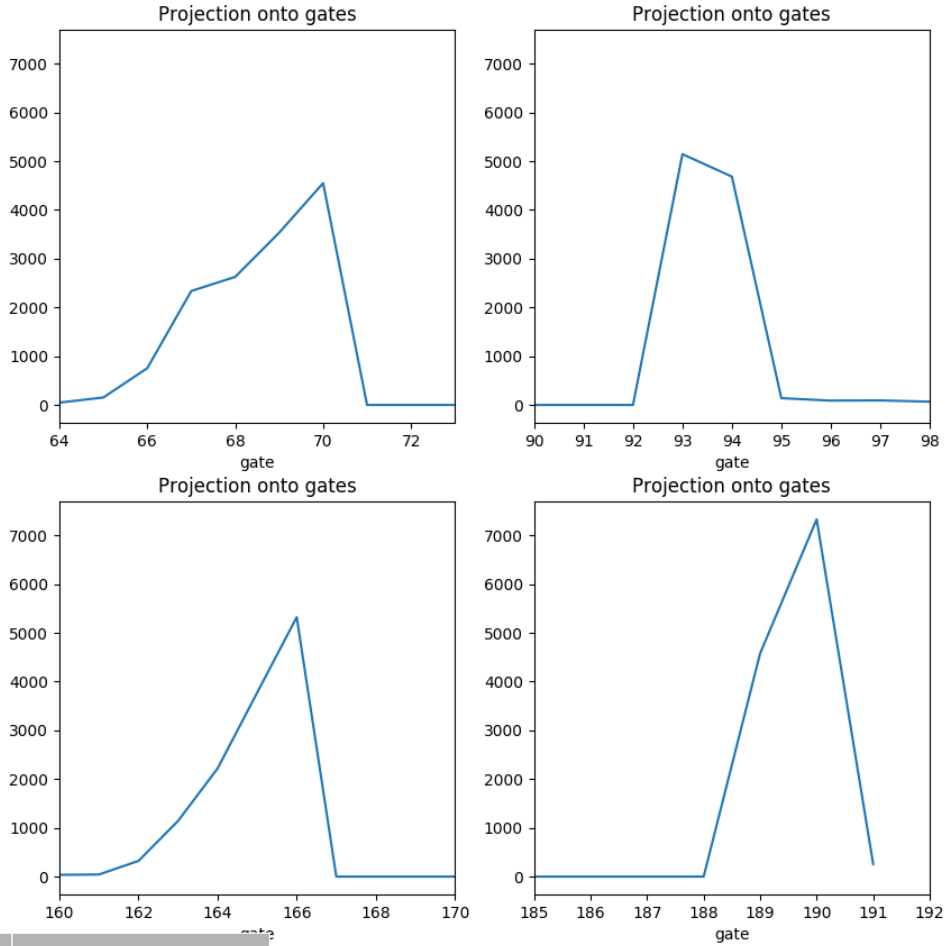
Input Gate-offset	Input Gate-length	Input No-trigger-offset	Input No-trigger-length
90	10	102	12



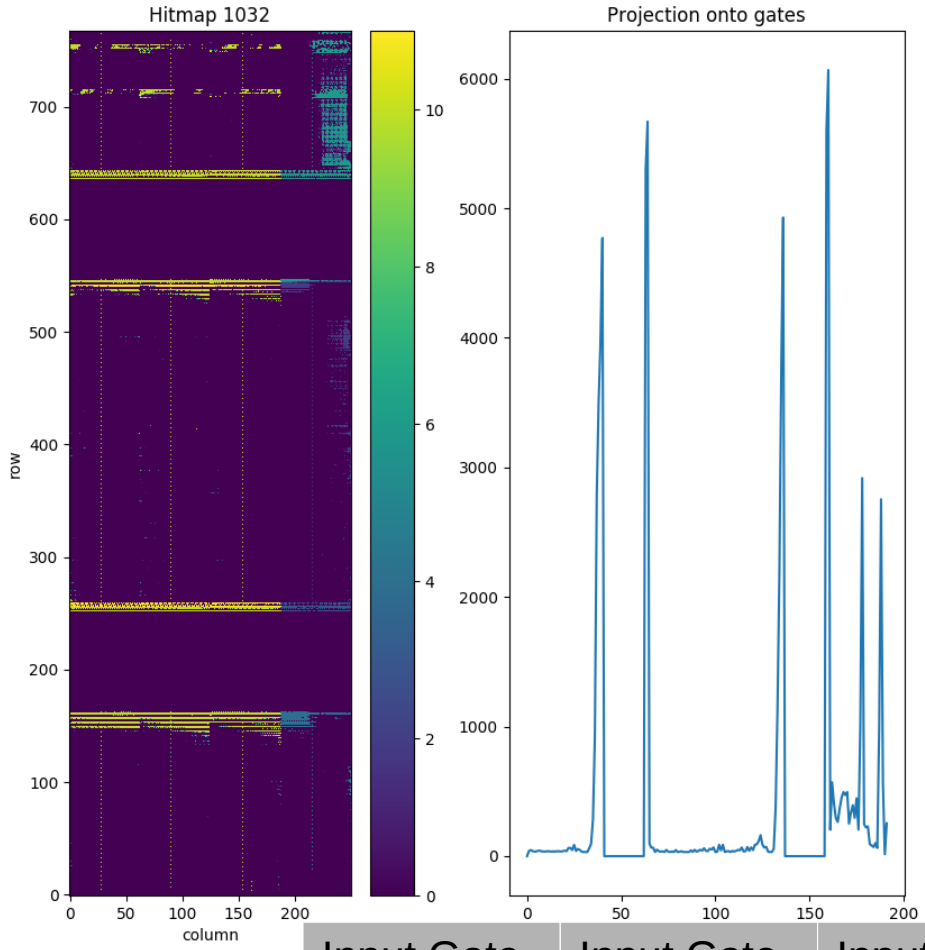


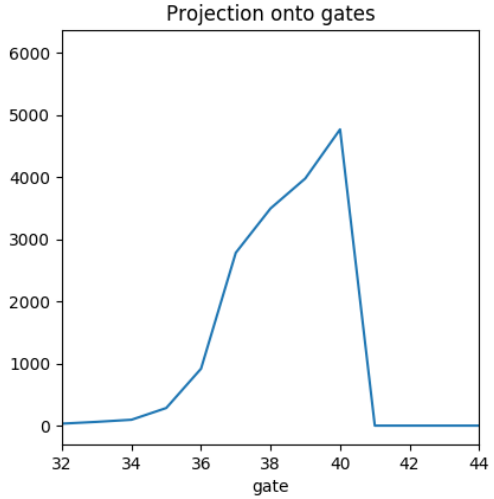
Input Gate-offset	Input Gate-length	Input No-trigger-offset	Input No-trigger -length
90	10	6	12

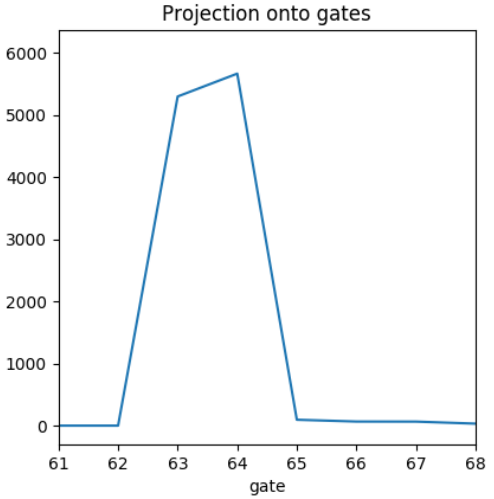


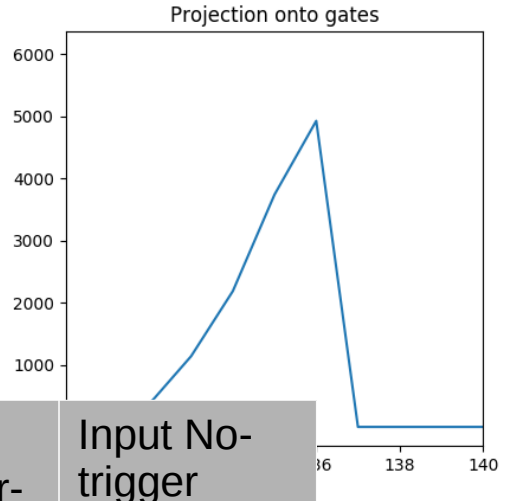


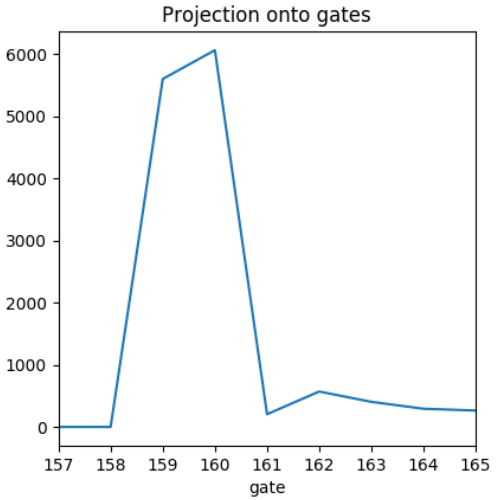
Input Gate-offset	Input Gate-length	Input No-trigger-offset	Input No-trigger -length
0	20	12	22



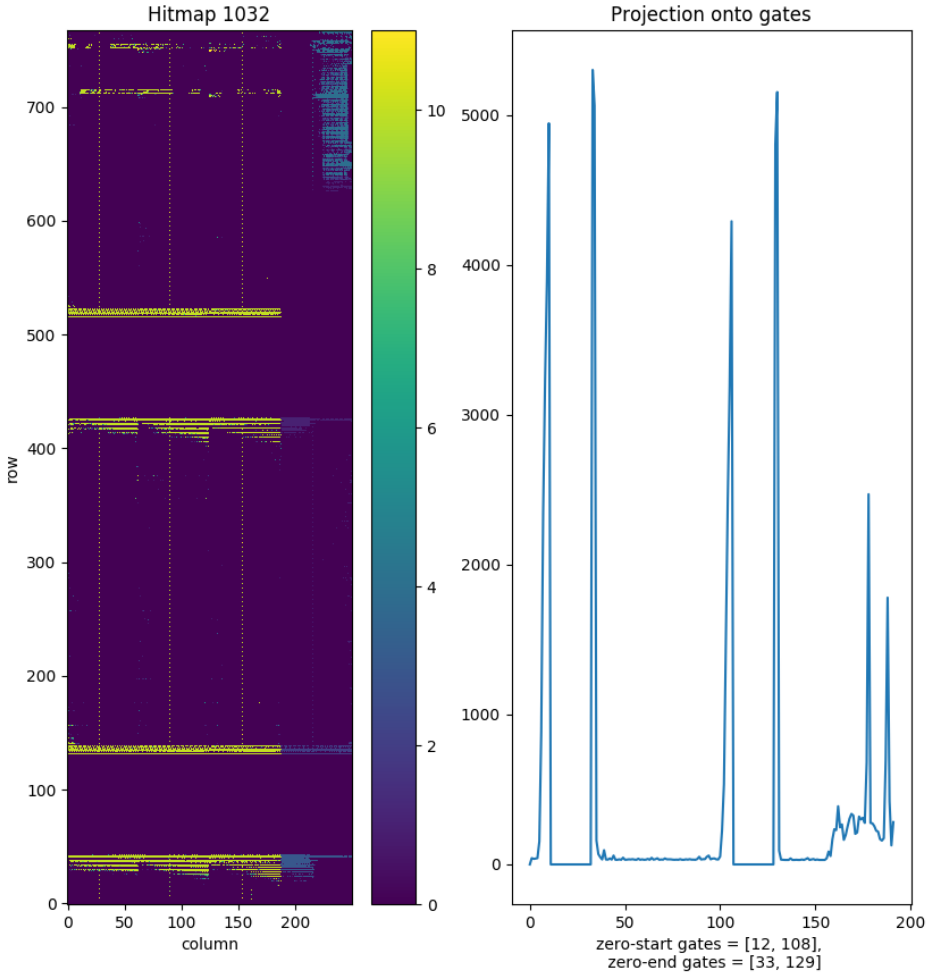


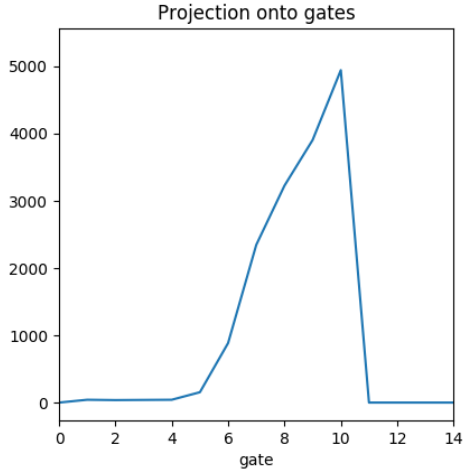


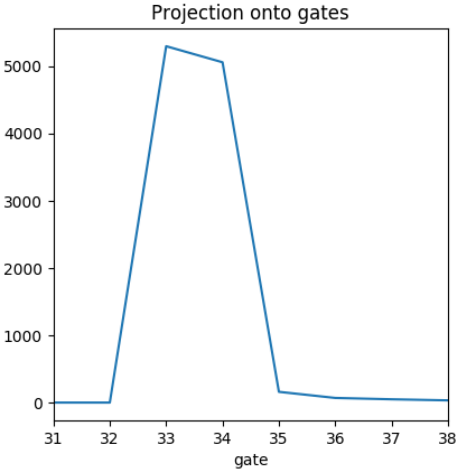


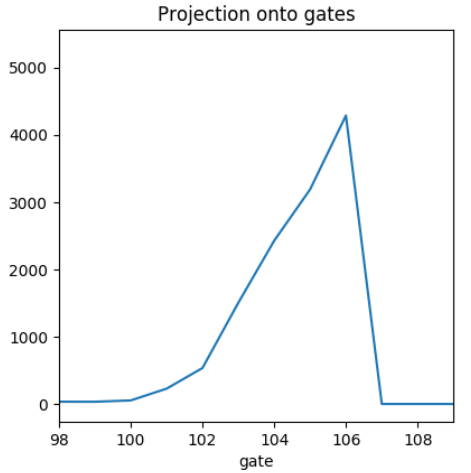


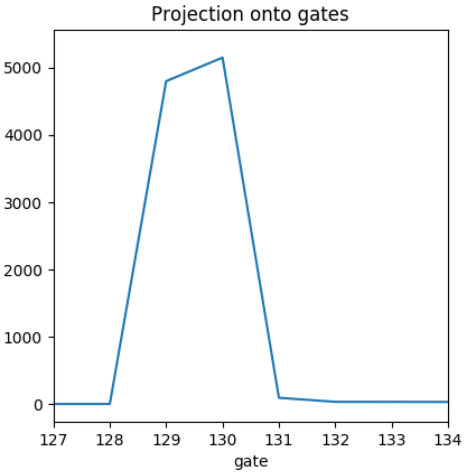
Input Gate-offset	Input Gate-length	Input No-trigger-offset	Input No-trigger -length
30	20	42	22



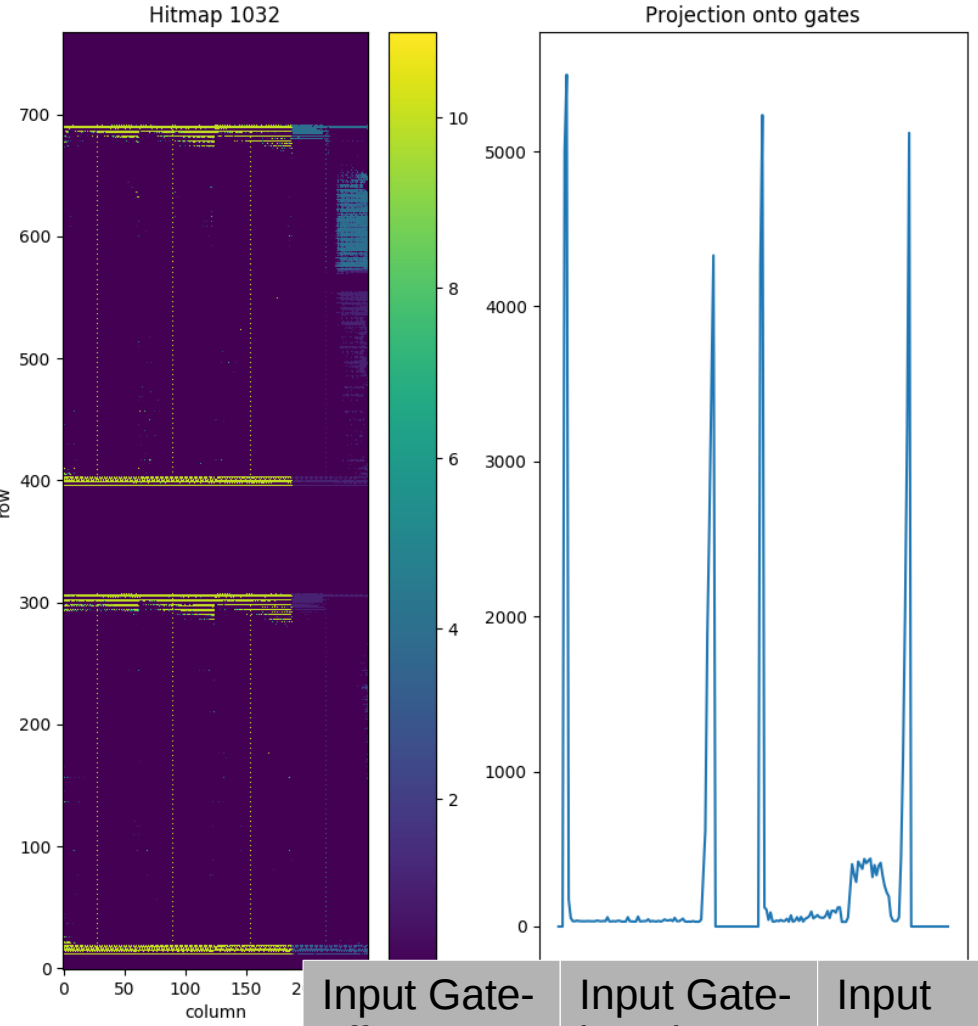


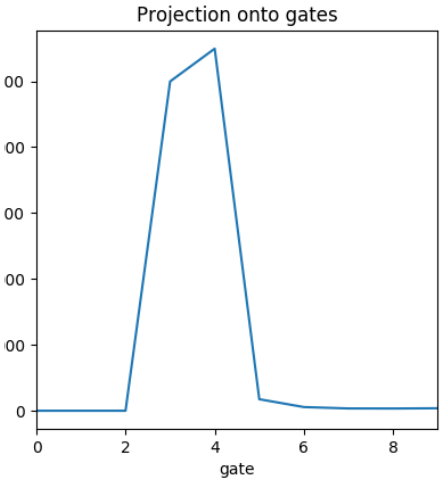


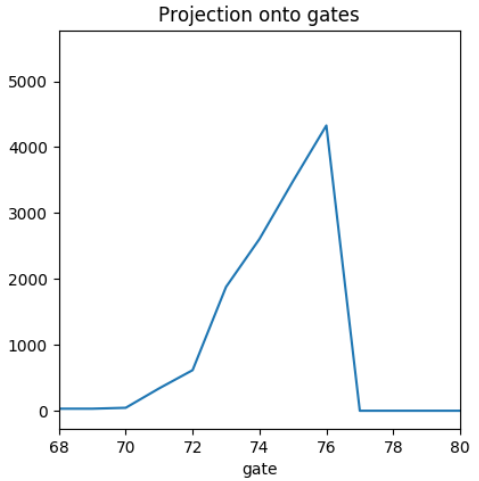


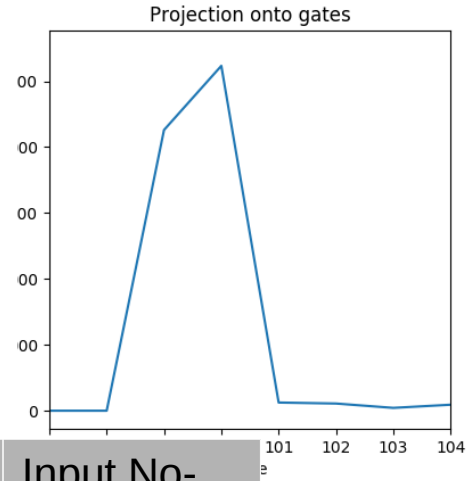


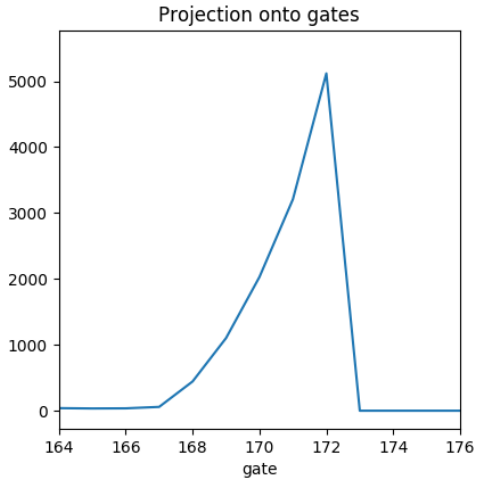
Input Gate-offset	Input Gate-length	Input No-trigger-offset	Input No-trigger-length
60	20	72	22



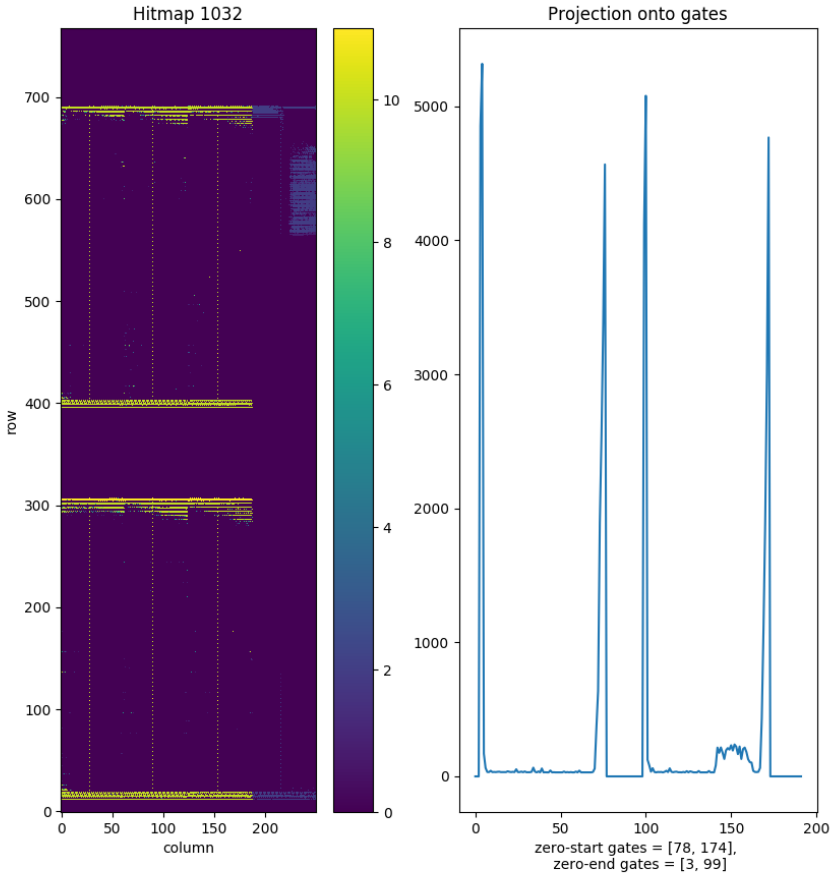


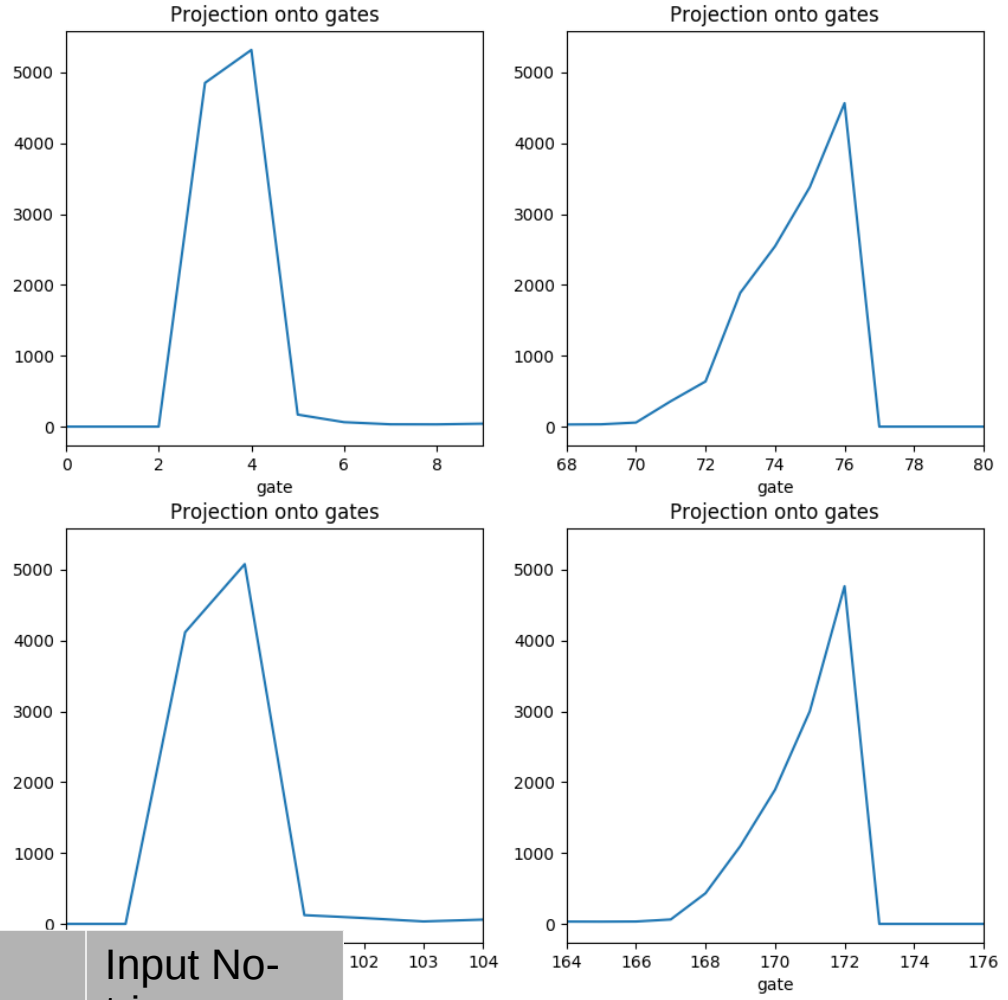




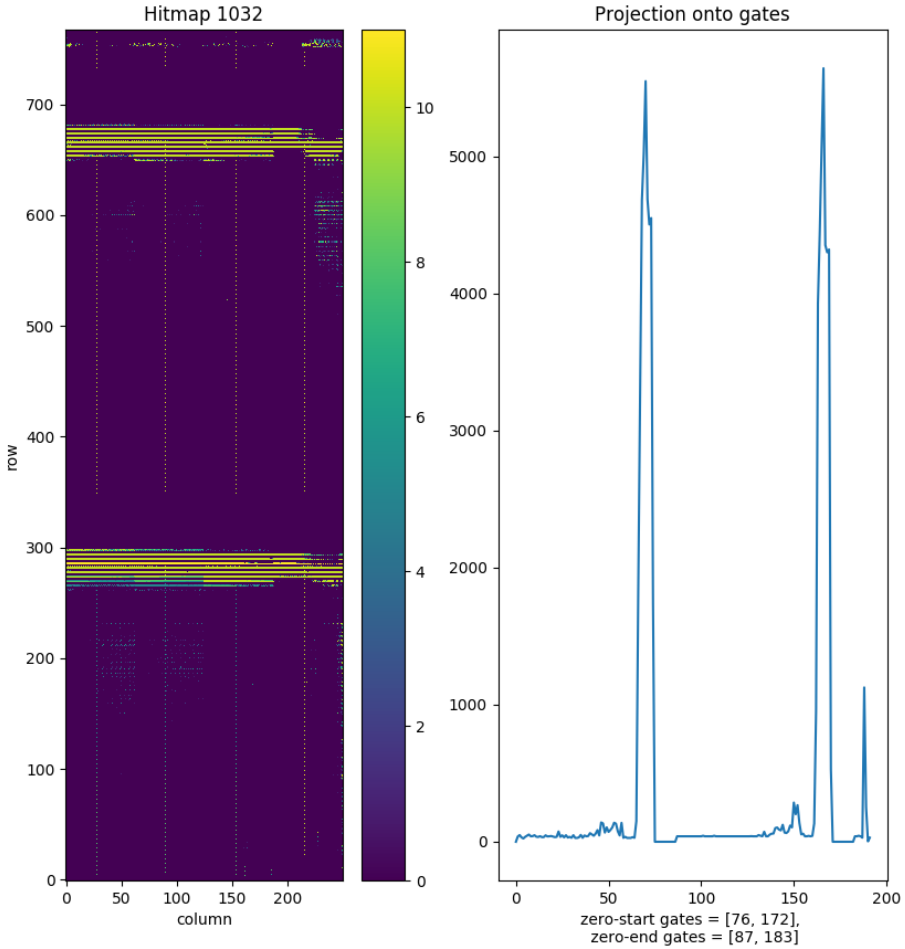


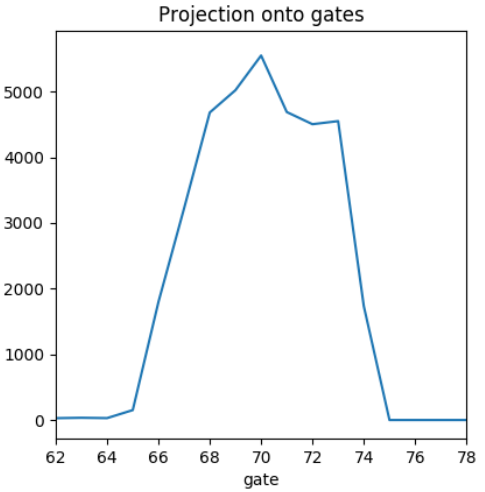
Input Gate-offset	Input Gate-length	Input No-trigger-offset	Input No-trigger-length
90	20	102	22

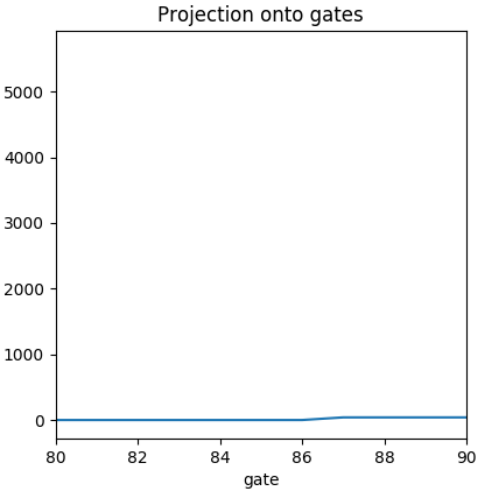


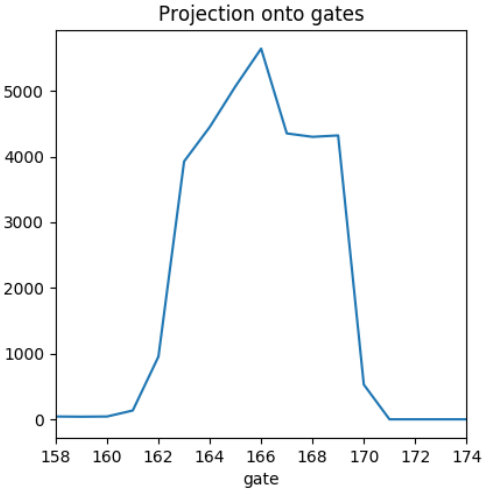


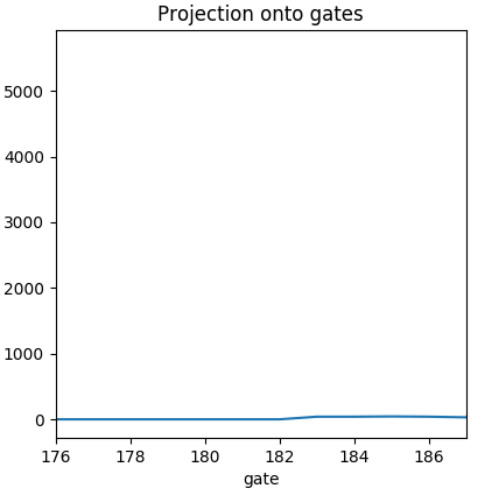
Input Gate-offset	Input Gate-length	Input No-trigger-offset	Input No-trigger-length
90	20	6	22



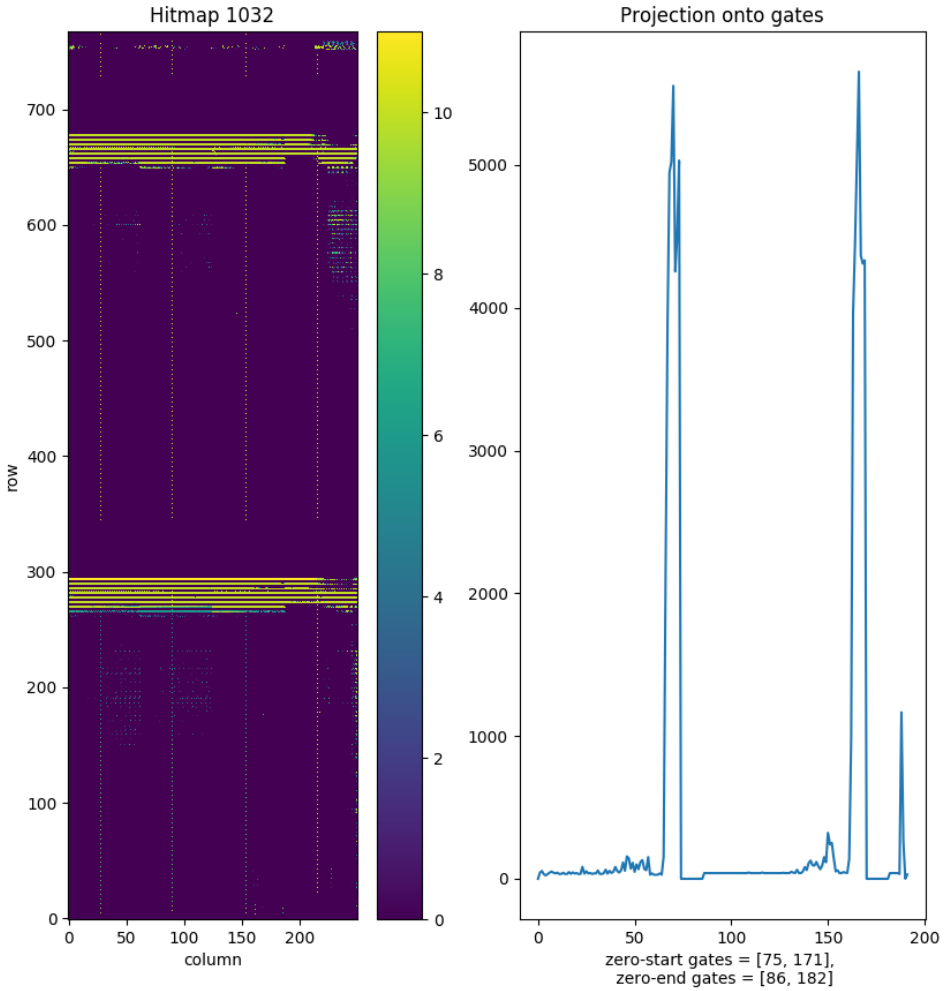


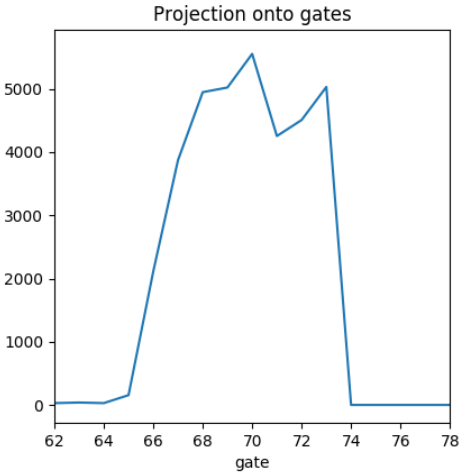


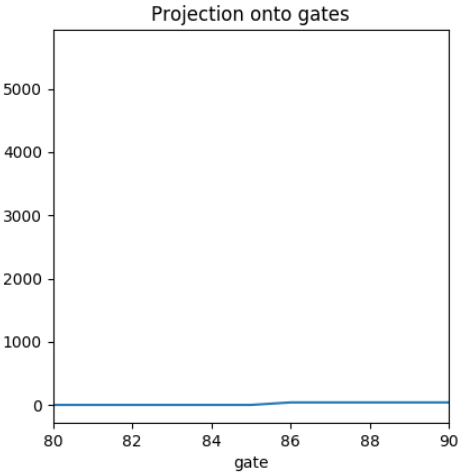


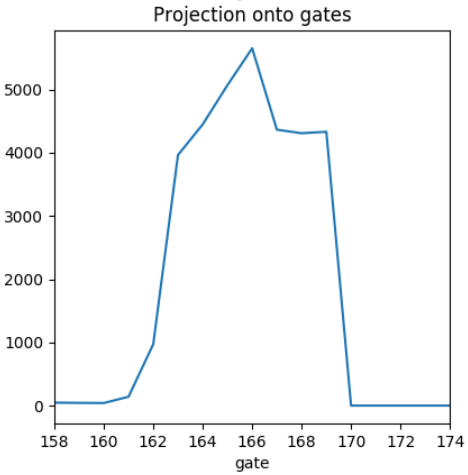


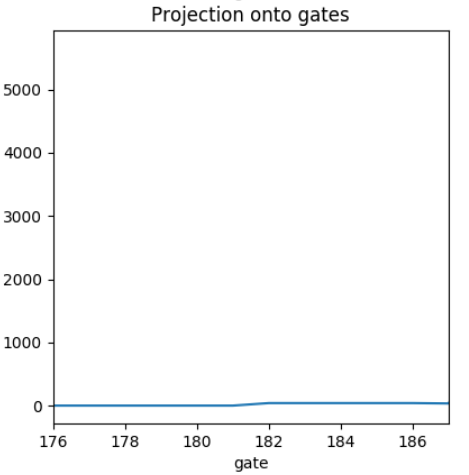
Input Gate-offset	Input Gate-length	Input No-trigger-offset	Input No-trigger -length
10	10	18	12





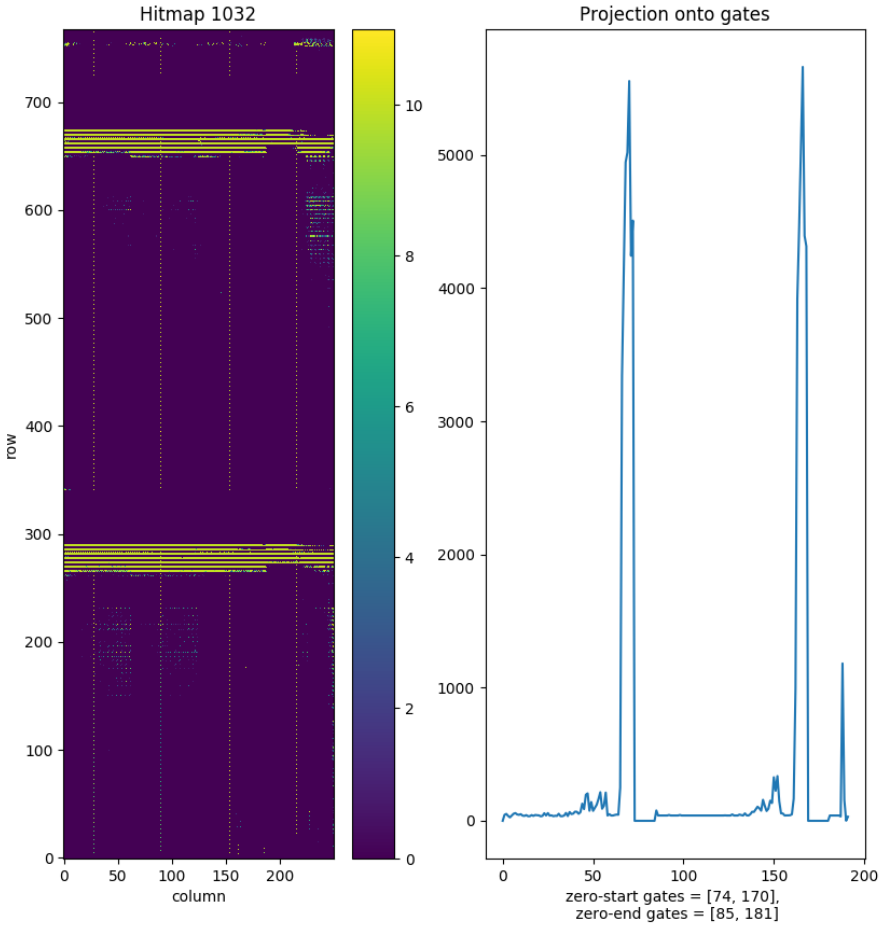


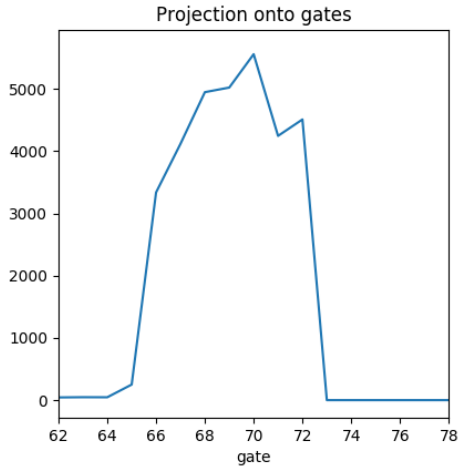


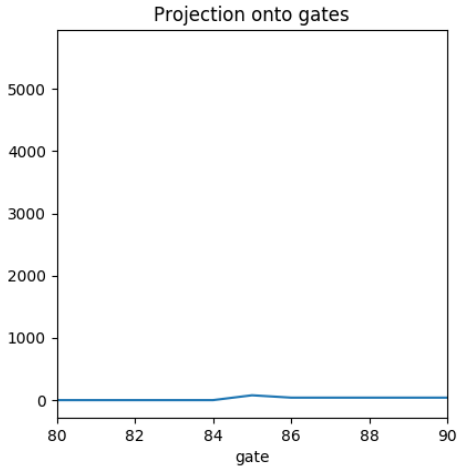


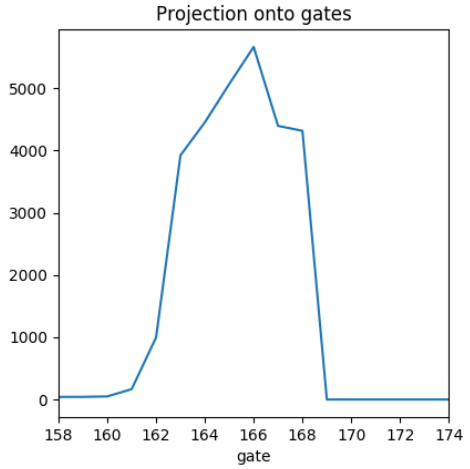
Input Gate-offset	Input Gate-length	Input No-trigger-offset	Input No-trigger -length
10	10	19	12

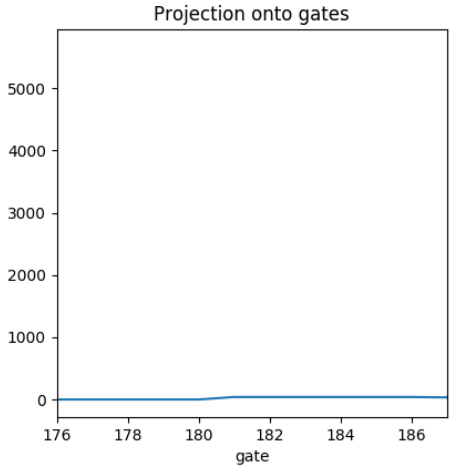
Input Gate-offset	Input Gate-length	Input No-trigger-offset	Input No-trigger -length
10	10	20	12



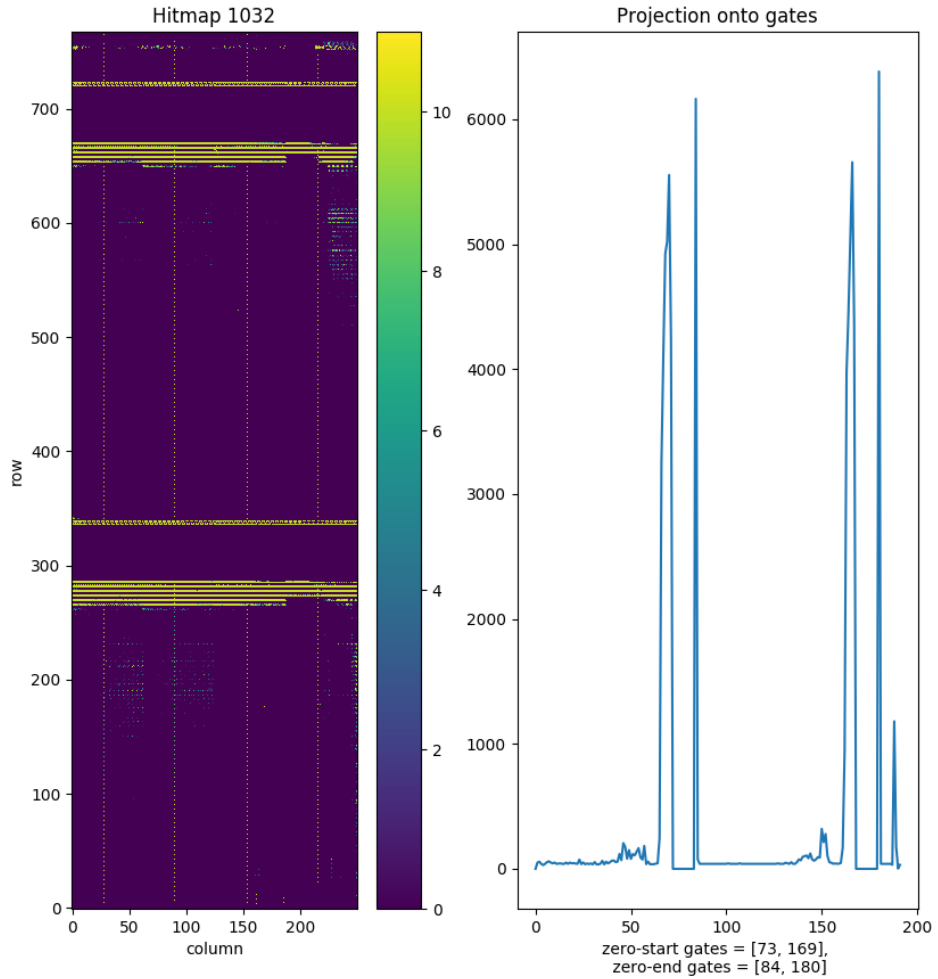


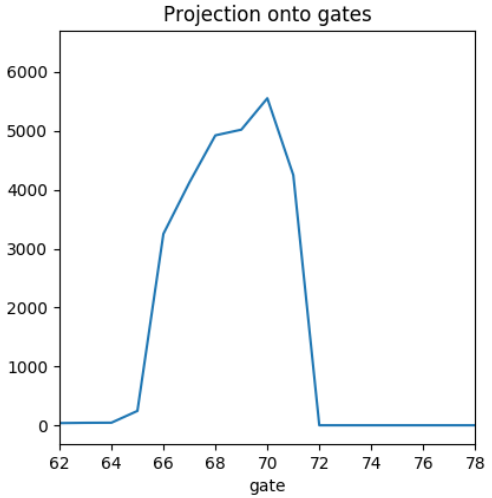


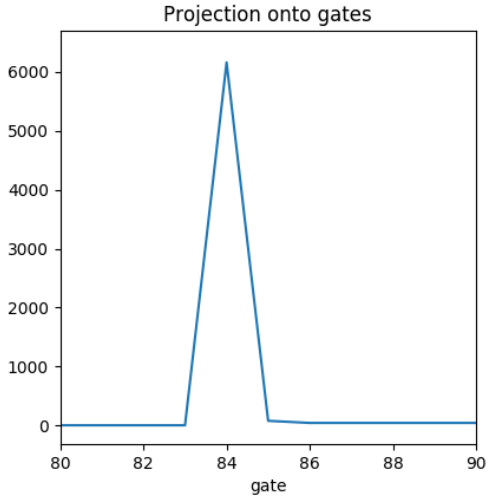


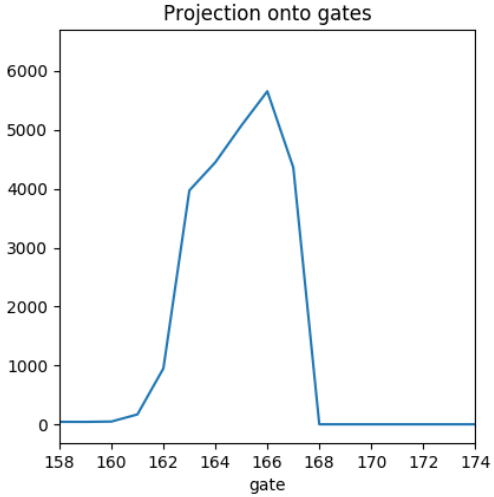


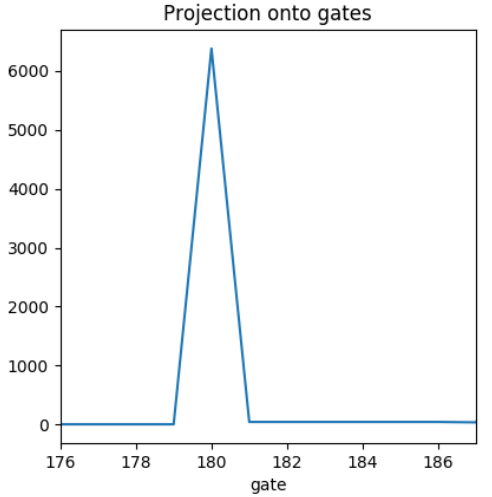
Input Gate-offset	Input Gate-length	Input No-trigger-offset	Input No-trigger -length
10	10	21	12



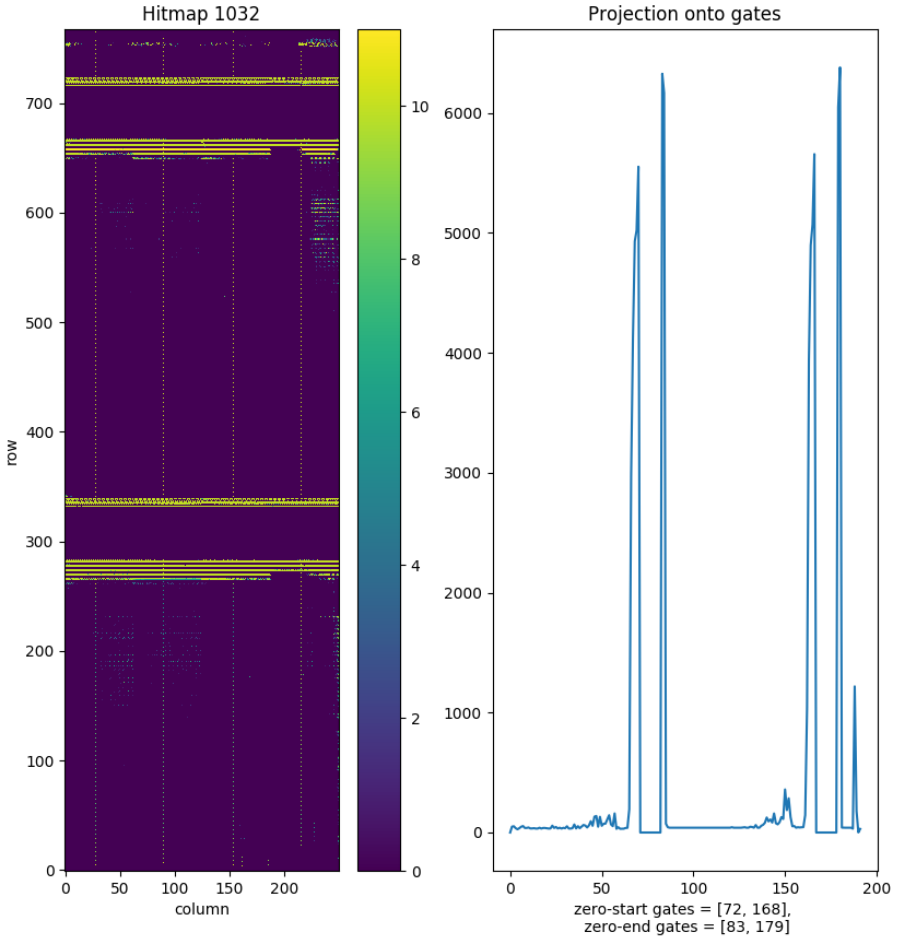


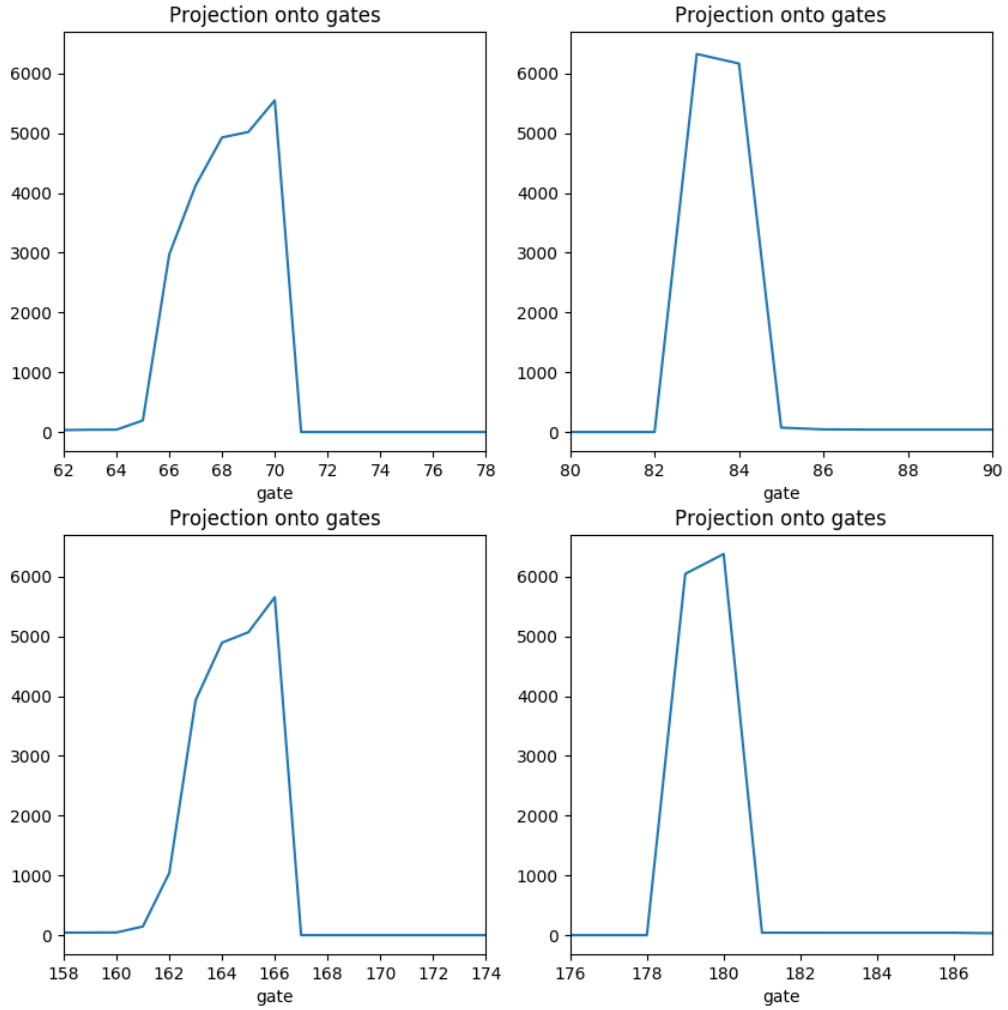






Input Gate-offset	Input Gate-length	Input No-trigger-offset	Input No-trigger -length
10	10	22	12





Input Gate-offset	Input Gate-length	Input No-trigger-offset	Input No-trigger -length
10	10	23	12