# TOP

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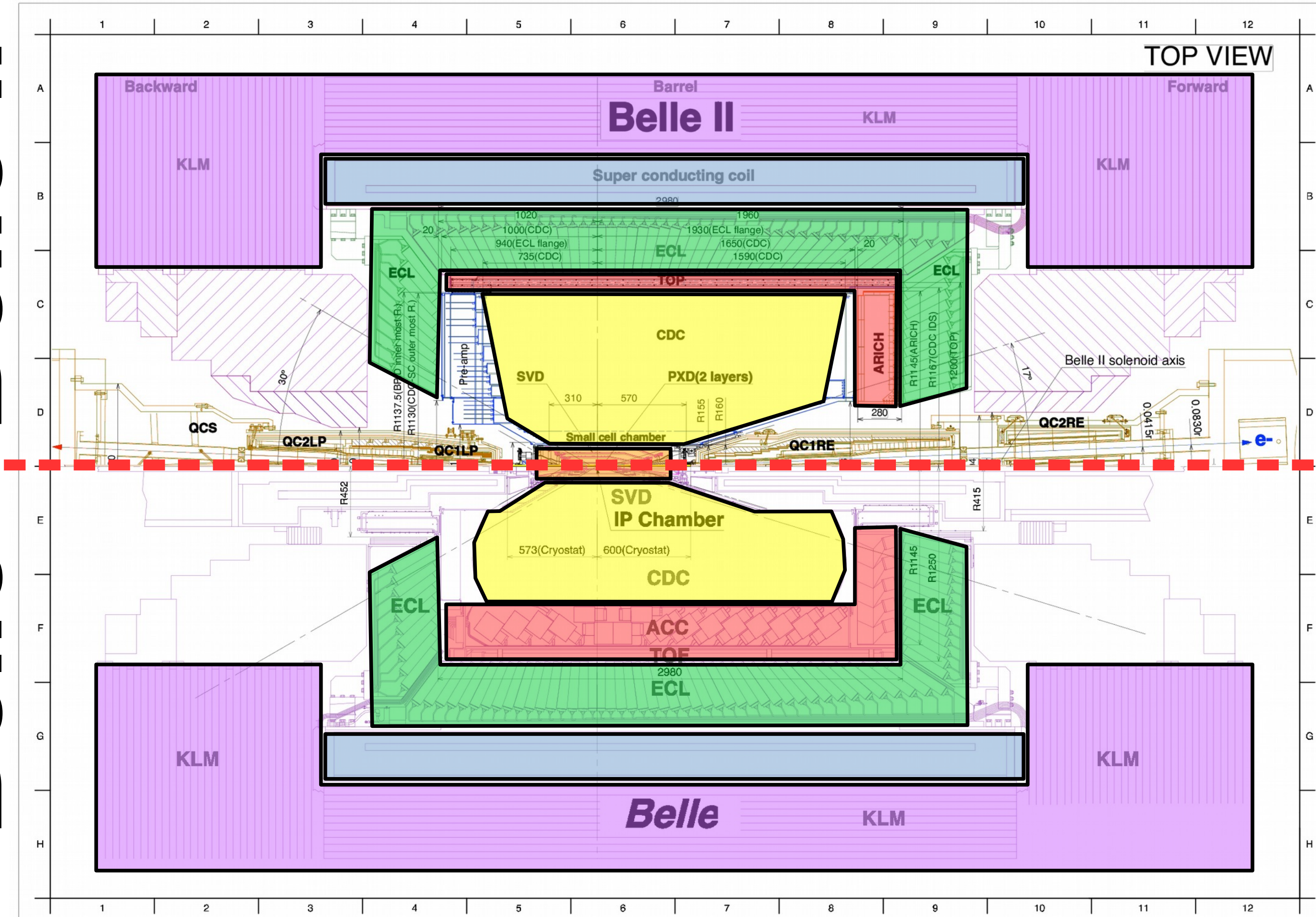
For the TOP Grou[

Belle II TRG/DAQ WS
Yonsei University
08/26/2019

# Belle II Detector Upgrade

Belle II

Belle




$K_L$/Muon System

Magnet Coil

EM Calorimeter

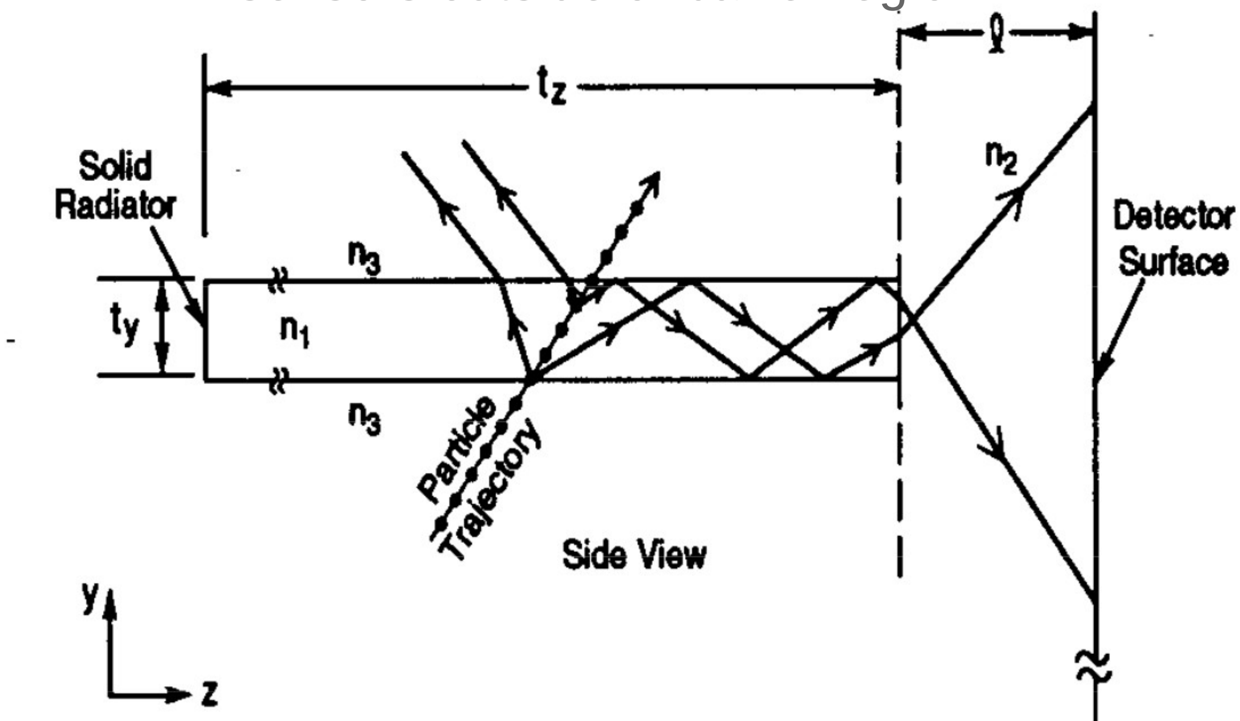
π/K Identification

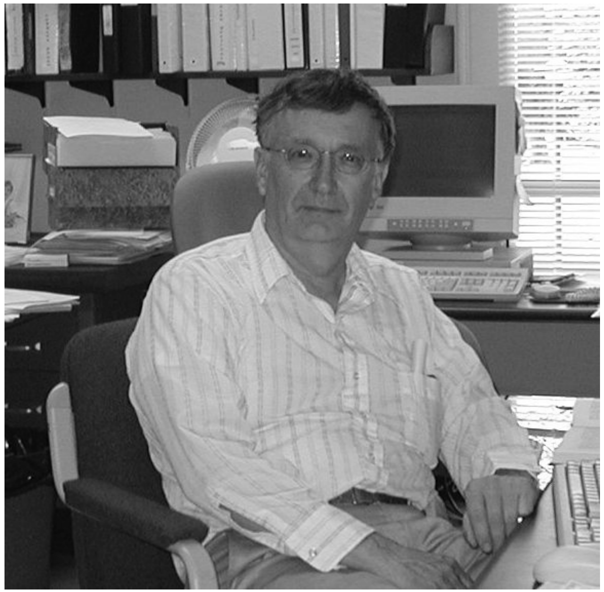
Drift Chamber

Silicon Tracking

# Belle II Barrel PID: A DIRC Derivate I

- DIRC: “Detector for Internally Reflected Cherenkov Light”
  - B. Ratcliff, SLAC PUB637 1
- Excellent solution to barrel PID needs in B-factories
  - Thin: Only radiator + casing in front of calorimeter, sensors outside of barrel region



# Belle II Barrel PID: A DIRC Derivate II

- DIRC: “Detector for Internally Reflected Cherenkov Light”
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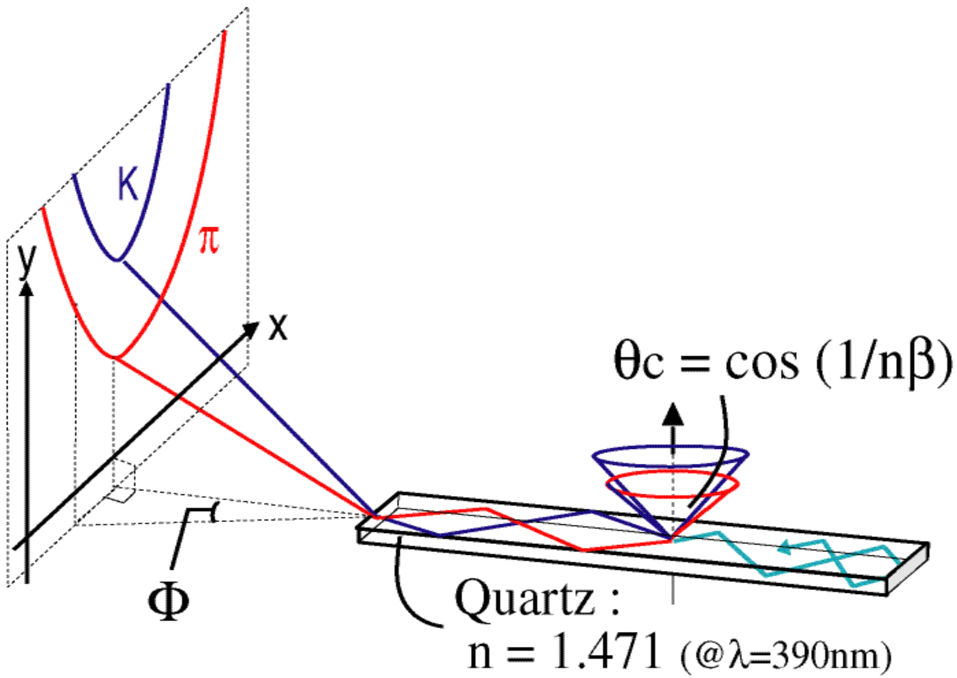
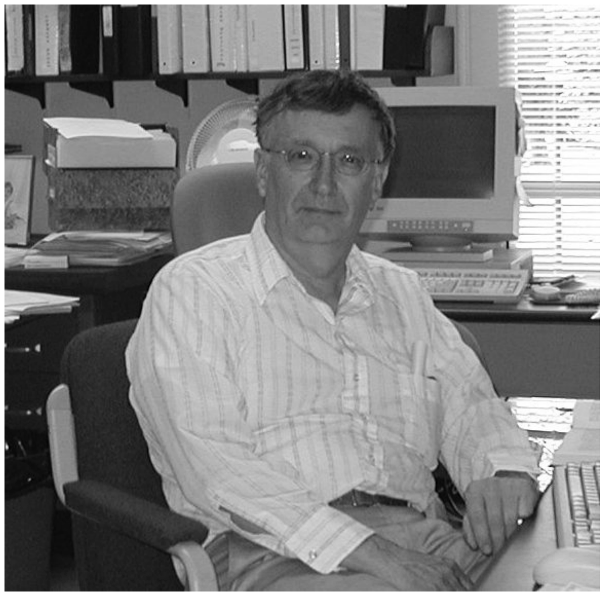
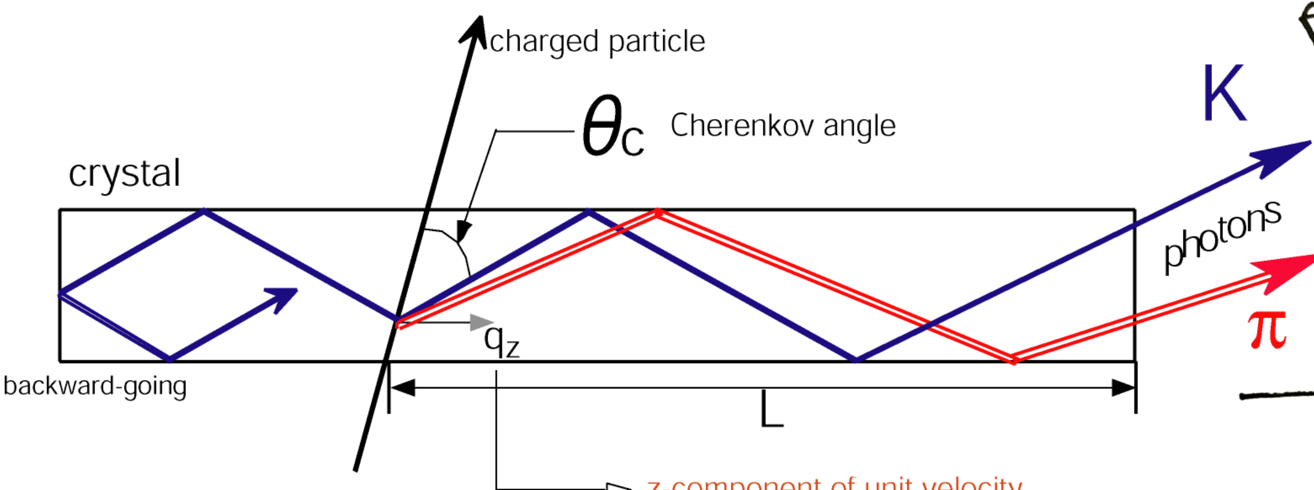
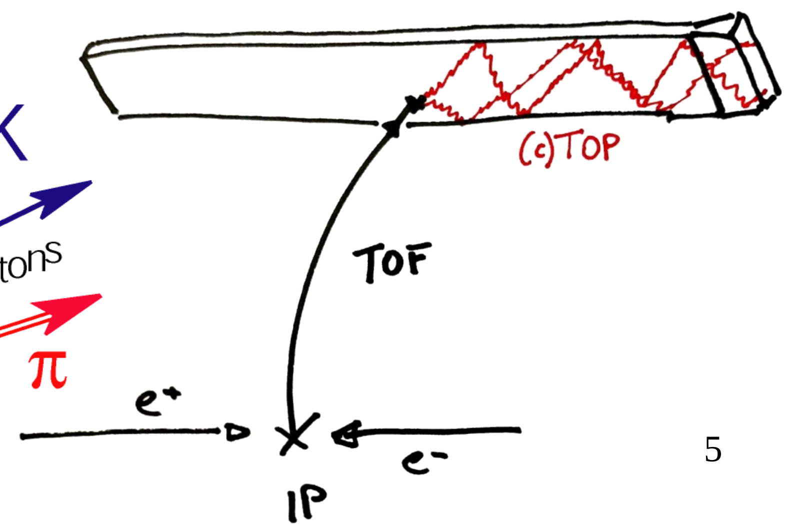


# The “Time of Propagation” (TOP) Detector I

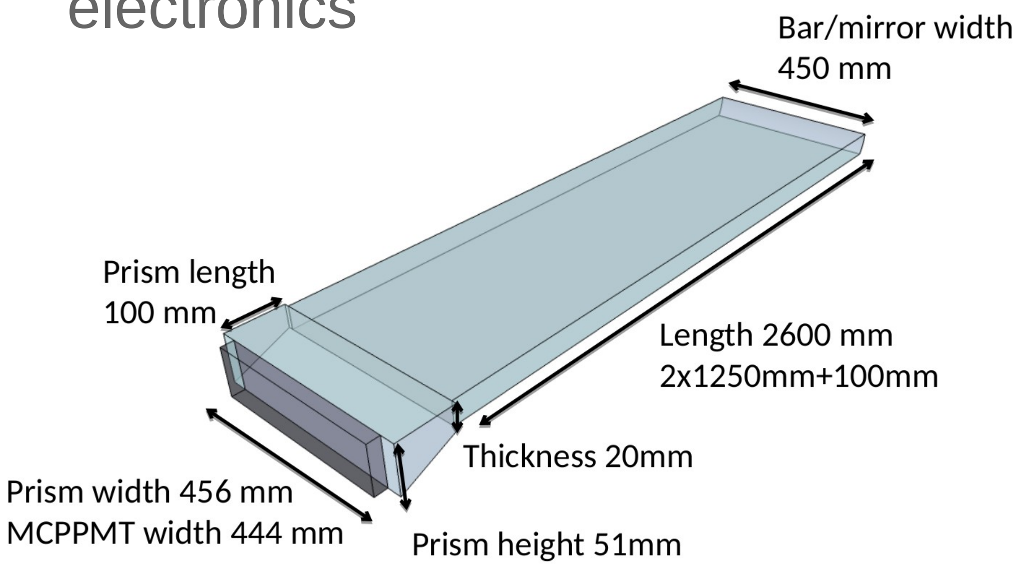
- A DIRC, but smaller: use timing instead of large expansion volume
- Instead of reconstructing the full ring image, measure time of propagation (path length) of individual Cherenkov photons.
  - Cherenkov photons from lighter particles arrive earlier on average
  - Since collision timing is well known (in principle), measure ToF at the same time
  - Chromatic dispersion is really not making this easier...

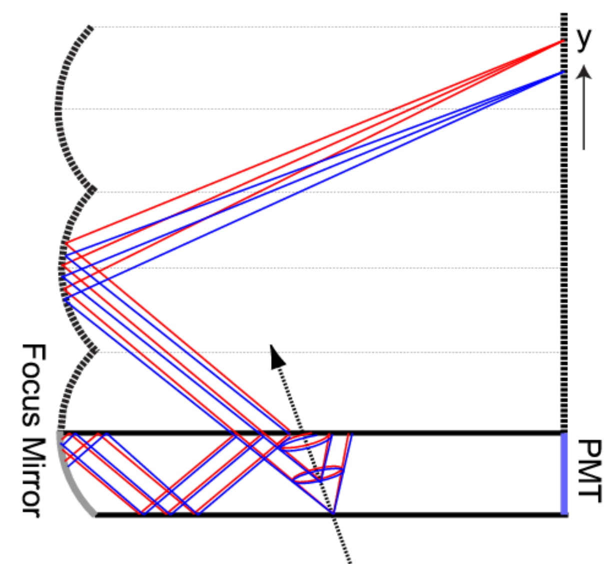


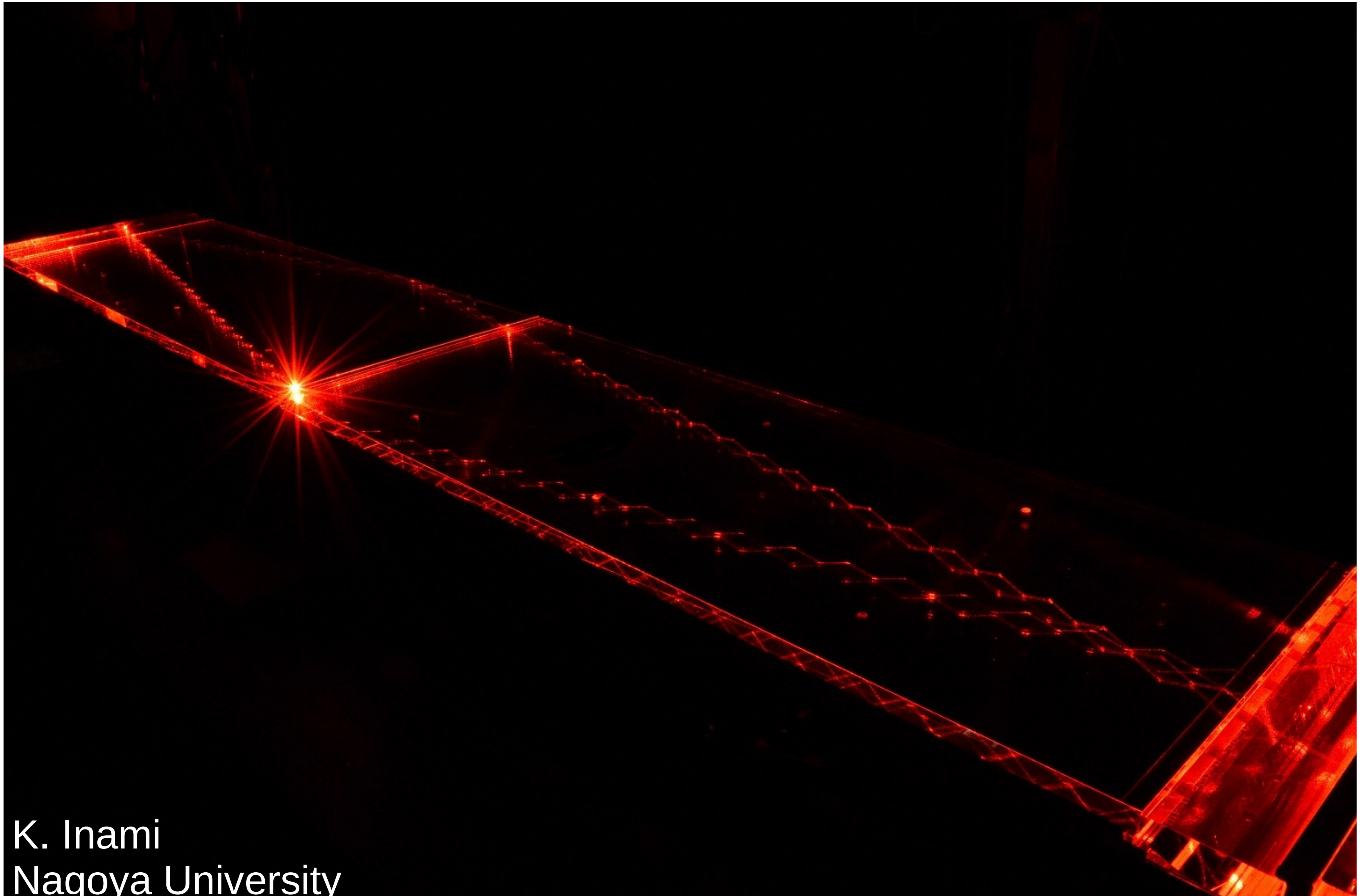
# The "Time of Propagation" (TOP) Detector II

- 16 quartz Cherenkov radiator bars arranged around IP
- Forward side: spherical mirror
  - Effectively removes bar thickness for reflected photons
  - Different wavelengths are focused on slightly different points
- Backward side: small expansion prism, sensors, readout electronics



# TOP: Total Internal Reflection



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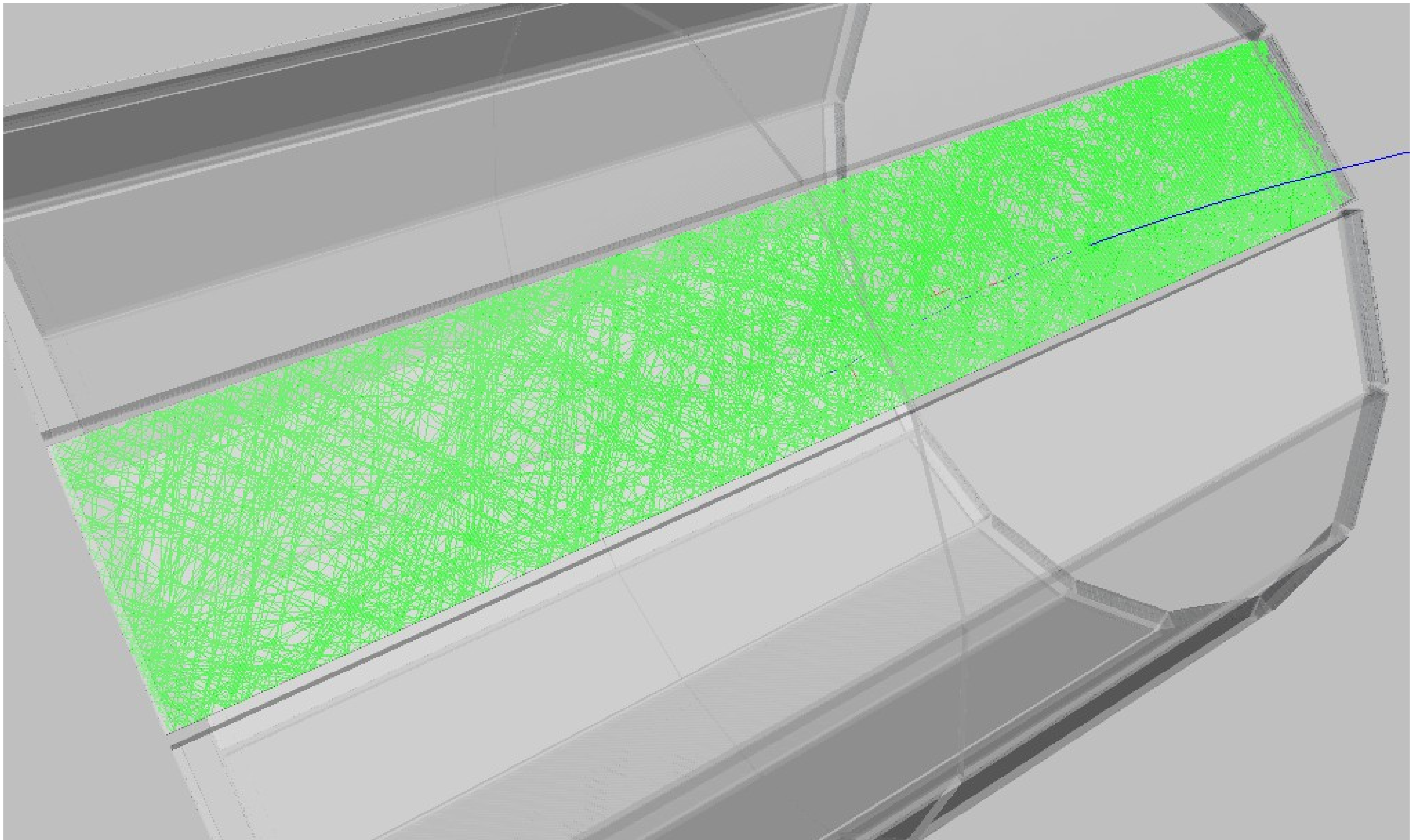
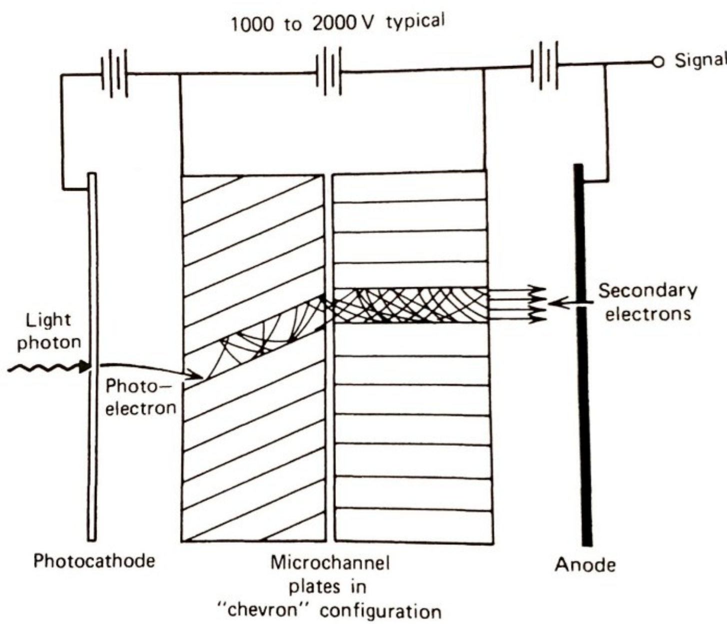


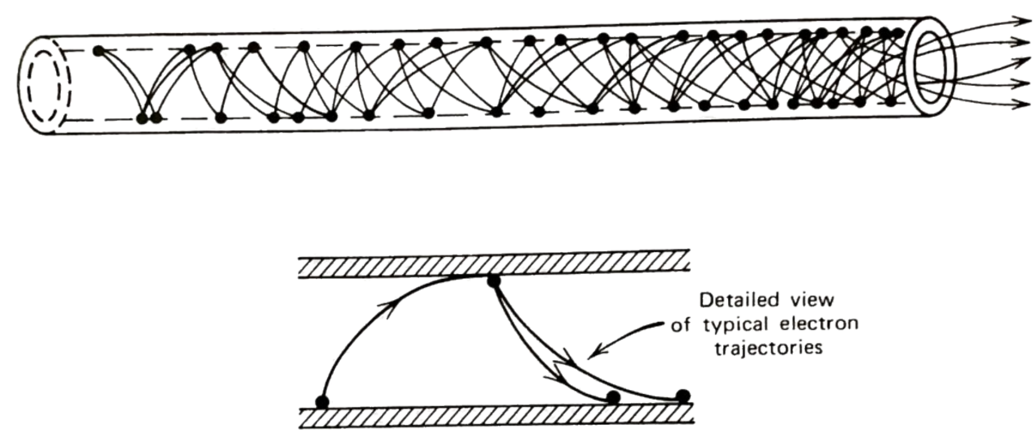
# TOP Readout: Requirements

- Goal: <100ps single optical photon time resolution
- Sensor requirements:
  - single photon efficiency
  - <50ps single photon time resolution
  - ~few mm spatial resolution
  - Operation in 1.5T B-field
- Electronics requirements:
  - 30kHz trigger rate
  - <50ps electronics time resolution
  - <30ps clock distribution jitter

# TOP Readout: Micro-Channel-Plate PMTs

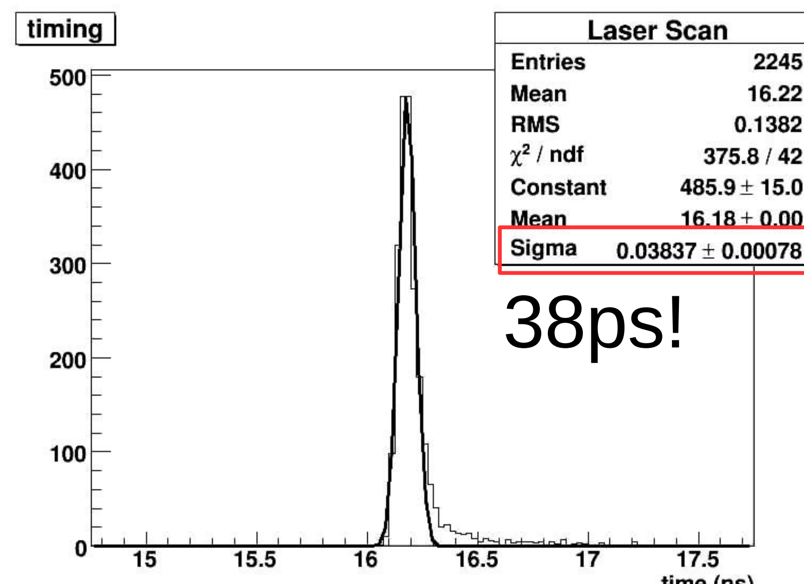
- Very fast amplification, but not well controlled
  - Good time resolution, single photon efficiency, but large output spread
- (Mostly) resistant to B-fields
- Pixelated anodes for spatial resolution



# Hamamatsu MCP-PMTs

- Measured single photon time resolution <40ps
- Lifetime (integrated charge) is limited
  - Original version ~1C/cm² (~50% of TOP)
  - ALD and LE-ALD versions: >10C/cm² (other ~50% of TOP)

# TOP Readout: Electronics

- Reads MCP-PMT signals
- Time resolution <50ps
  - ~GSa/s sampling
  - ~500MHz bandwidth


?

# TOP Readout: Electronics

- Reads MCP-PMT signals
- Time resolution <50ps
  - ~GSa/s sampling
  - ~500MHz bandwidth
- 8192 channels
- Affordable
- Low power
- Small form factor
- Online data processing
- etc. etc.

# Readout: Electronics

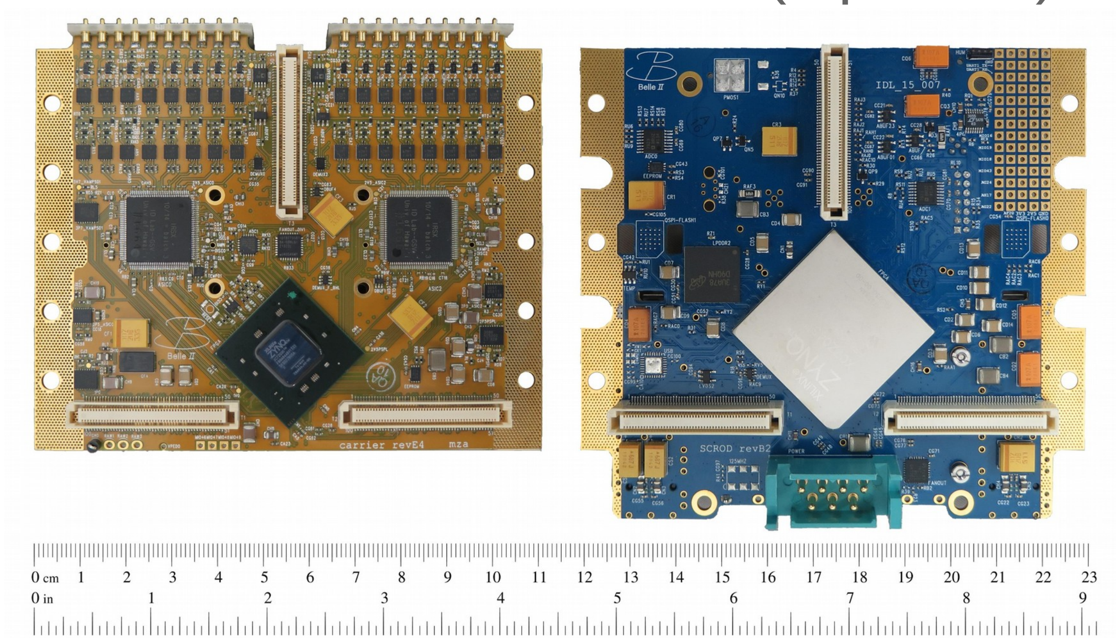
- “Oscilloscope on a Chip”: IRSX ASIC
  - Designed by IDLAB, UH (Prof. Gary Varner)
- Operated at 2.7GSa/s in TOP
  - ~600MHz analog bandwidth
  - 32k analog buffer cells (~10us)
  - 12 bit digitisation w/o deadtime
- Power budget ~600mW/ch
  - ASIC: ~125mW/ch
  - Preamp: ~150mW/ch
  - FPGAs: ~300mW/ch

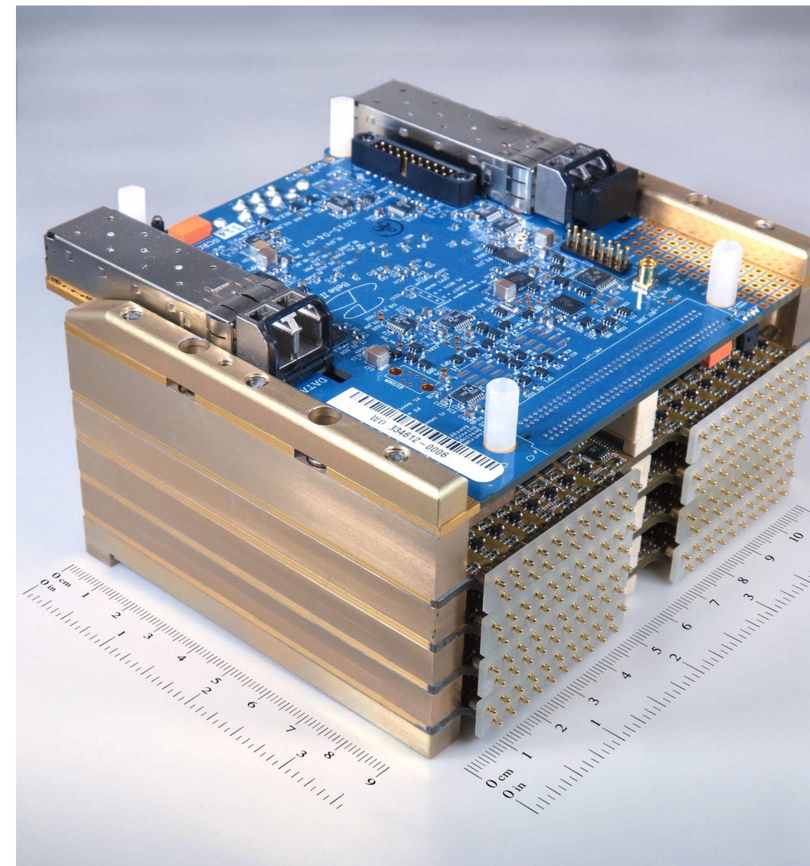
# Online Data Reduction

- Whole TOP stores $22 \times 10^{12}$ samples every second
- Only digitise relevant ASIC samples
  - Based on global trigger, local channel triggers
- Apply all raw data conditioning in frontend
  - Pedestal subtraction
  - Time base calibrations
- Extract waveform features in frontend
  - Photon timing, pulse shape parameters
- Write out only feature parameters
- Powerful frontend processing: 320 FPGAs, 640 ARM cores
  - Based on Xilinx Zynq SoCs: FPGA + ARM CPU

# TOP Frontend Readout Modules

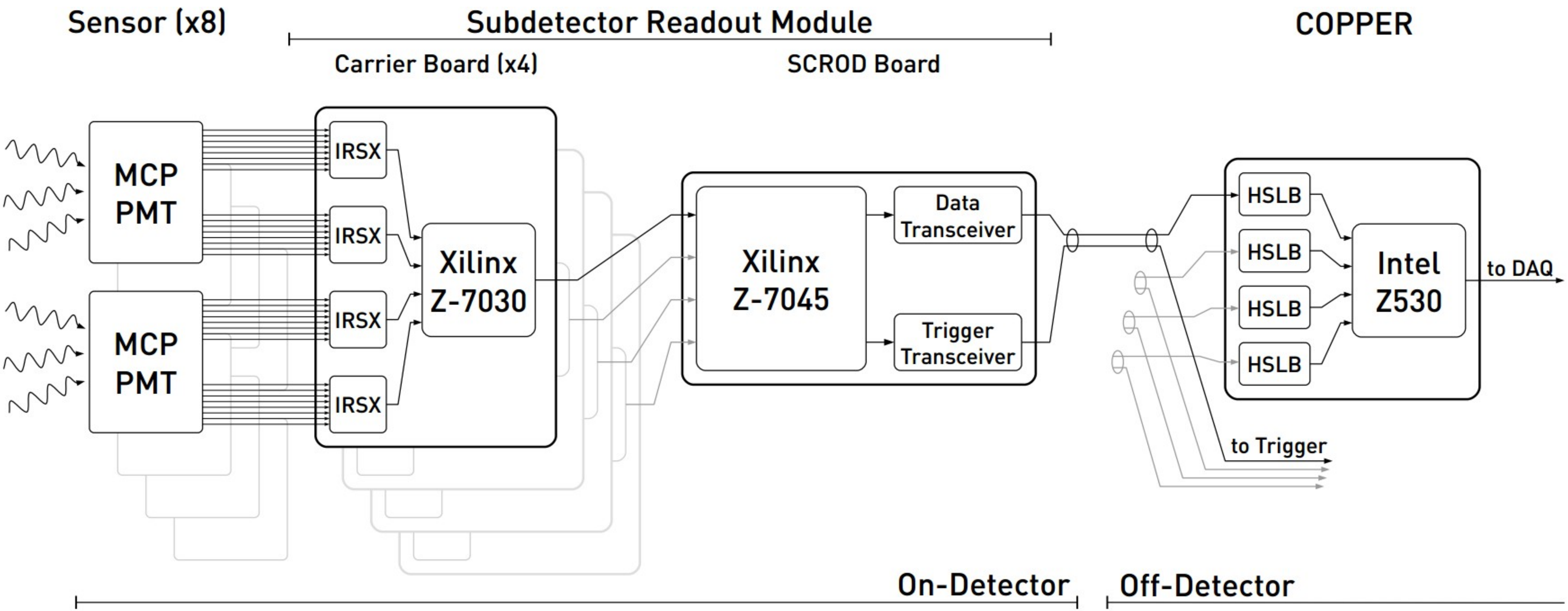
- Carrier: 4 ASICs, Zynq 7030
- SCROD: Zyng 7045
- Module: SCROD + 4 Carriers
  - 64 modules in total (4 per bar)



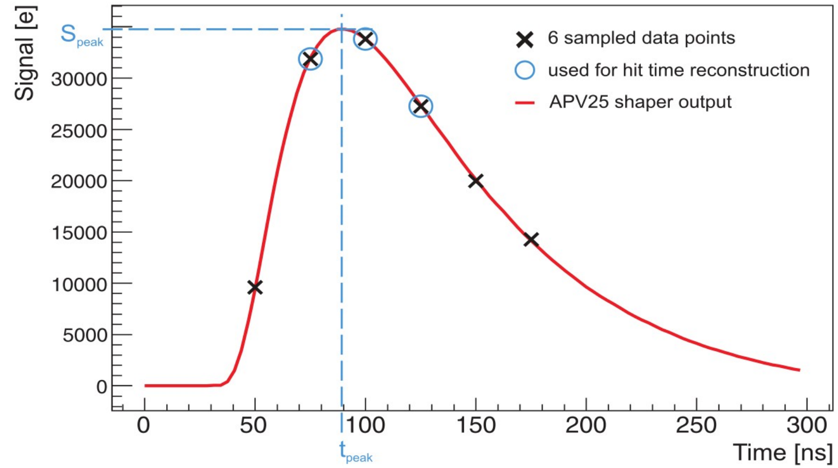
# Readout Dataflow

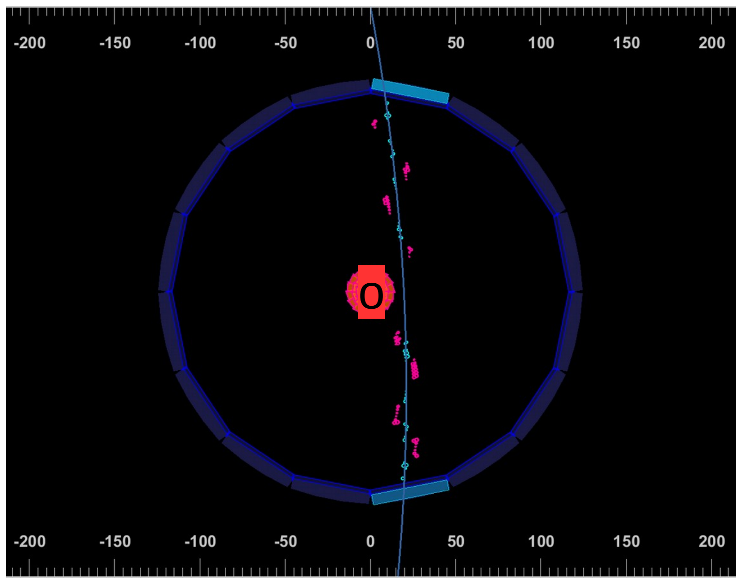
- Carrier FPGAs control ASICs, push waveform segments to SCROD
- Feature extraction on SCROD ARM CPU



# TOP Event Timing for Trigger

- Precise event time is important for SVD readout: 25ns frame spacing, can afford only few ns of jitter
  - ECAL and drift chamber trigger timing but resolution is ~tens of ns
- Why not use TOP information for L1 $T_0$ estimate?
- Complicated photon timing structure due to reflections etc.
  - Live likehood analysis of streamed TOP hit timings (no geometric info available)
  - No tracking information on trigger level
  - Estimated to produce <3ns T0 resolution (eventually)
- FPGA Infrastructure is set up, successfully used TOP timing for cosmics trigger
  - TOPTRG b2link readout it set up and included in local/global data taking



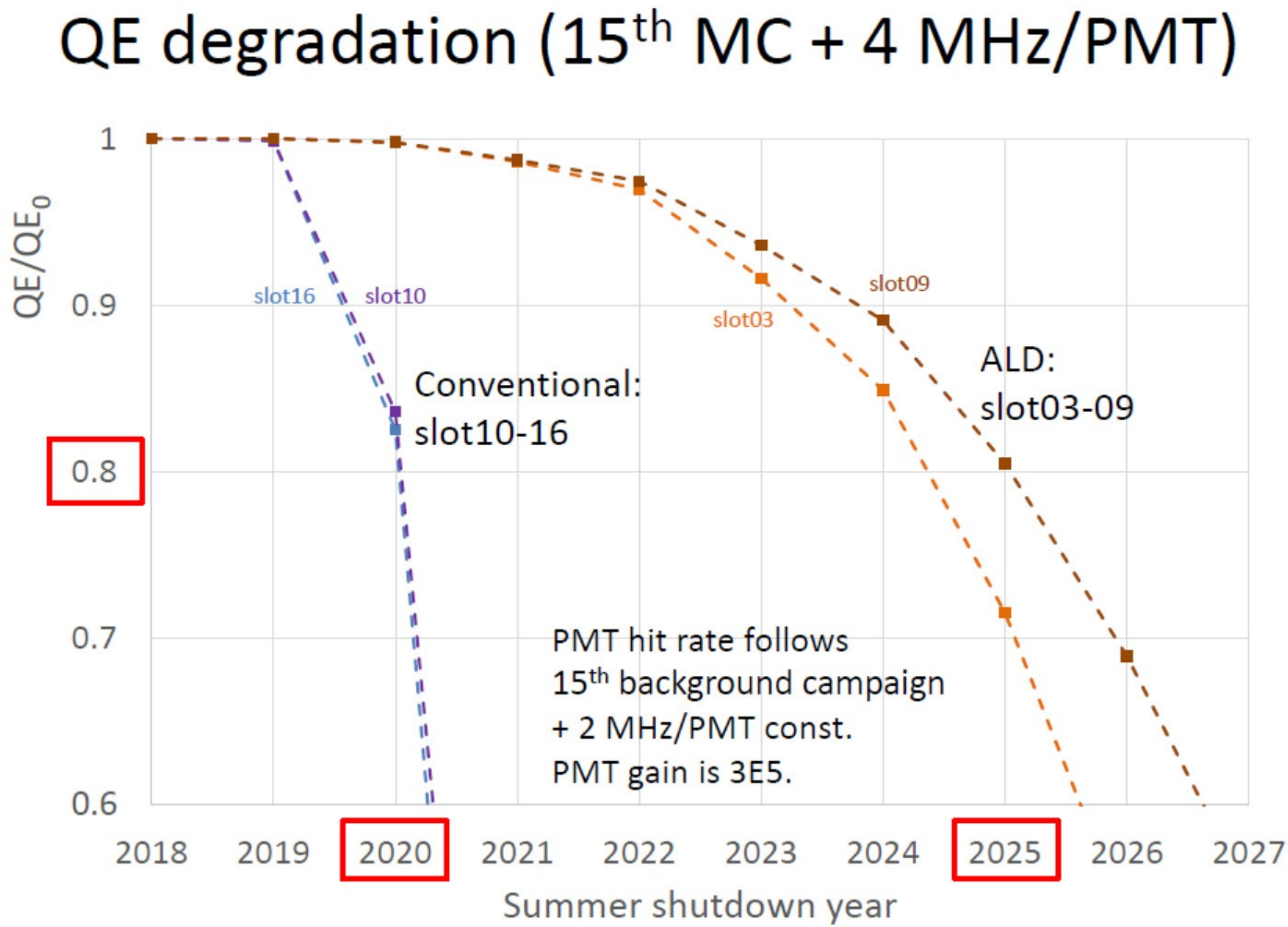
# Readout Status

- SCROD CPU crashes at ~1 BS/day
  - Recover by powercycle of the frontend (~20min)
  - Strong dependence on background conditions: happens more often when background rates are high and “spiky”
  - Don’t the know the exact reason, difficult to debug, cannot reproduce reliably
  - Maybe SEUs? Implementing SEU detection cores and DDR error checking into FW now. (but issue also happens in null runs without beam, though very rarely)
- Some ASICs self-masking in some runs (no response from ASIC within timeout)
  - Negligible hit loss, mostly recovered on run restart/SALS
- Configuration/pedestal acquisition works through slowcontrol system, will be tested and refined until beam start.

# Operations

- Stable Readout with injected occupancy (>>average physics occupancy) tested and verified at 20kHz
  - However: we don't have a good idea how to generate "spiky" "beam-background-like" occupancy for testing
- TOP conditions are fully monitored through nsm2 network
- TOP configuration and "setup for data taking" is now implemented and confirmed working from the TOP copper library
  - Needs some more testing
  - Frontend programming daq_slc app still missing (but simple)

# PMT Degradation and Replacement Plans



# Summary

- TOP is the first detector of its kind
  - Novelties in design and implementation
  - Cutting edge performance requirements


- TOP was basically stable in Phase 3 so far…
  - … except for crashing boardstacks, losing about 30-45min of luminosity per day for power cycling frontends.
- TOP PID performance is approaching MC predictions
  - Finally getting complex calibrations under control

# Hawaii Waveform Sampling ASICs

- Hawaii Instrumentation Development Lab spinoff: Nalu Scientific
  - Founded by Isar Mostafanezhad (ex-postdoc of IDLab)
- Commercialisation of switched capacitor waveform sampling ASICs based on IDLab designs
- Three ASICs available:
  - SiRead: 32 channels, ~1 GSa/s
  - ASoC: 8 Channels, ~3 GSa/s
  - Aardvarc: 4 Channels, ~14 Gsa/s

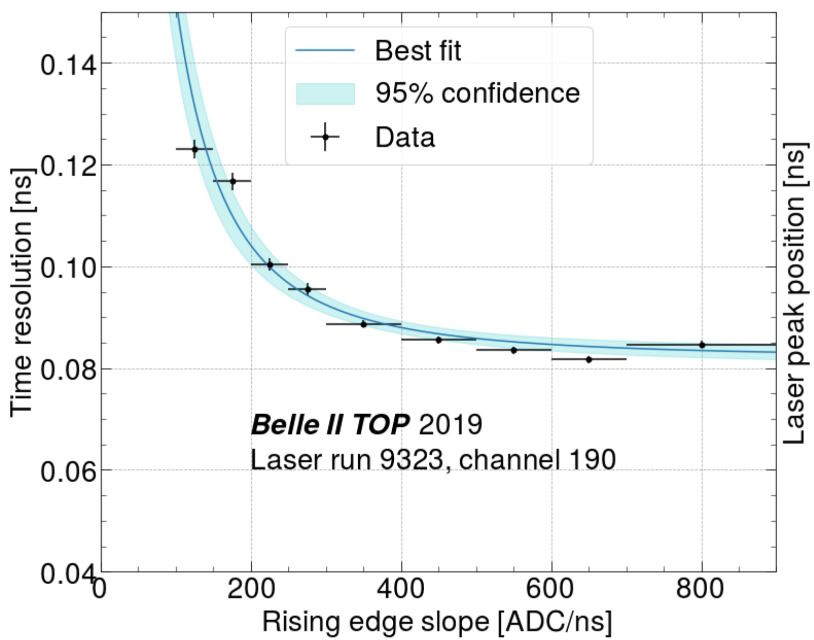
Nalu Scientific

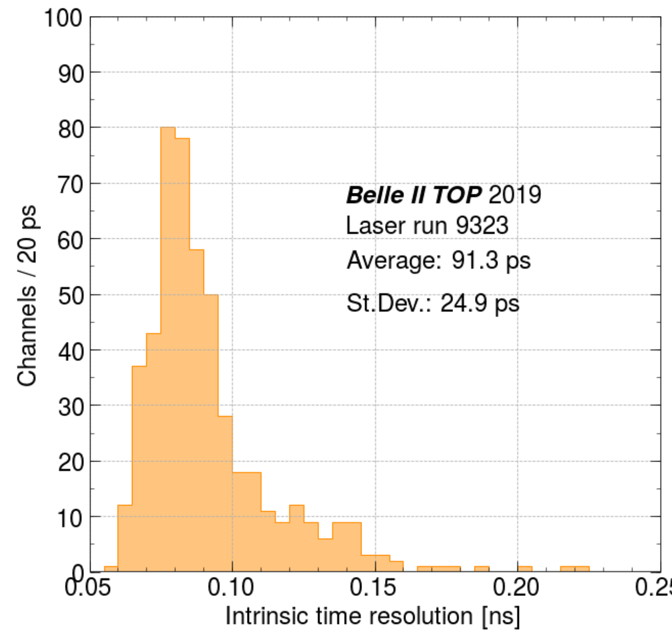
Data Acquisition Systems

isar@naluscientific.com

# Single Photon Time Resolution

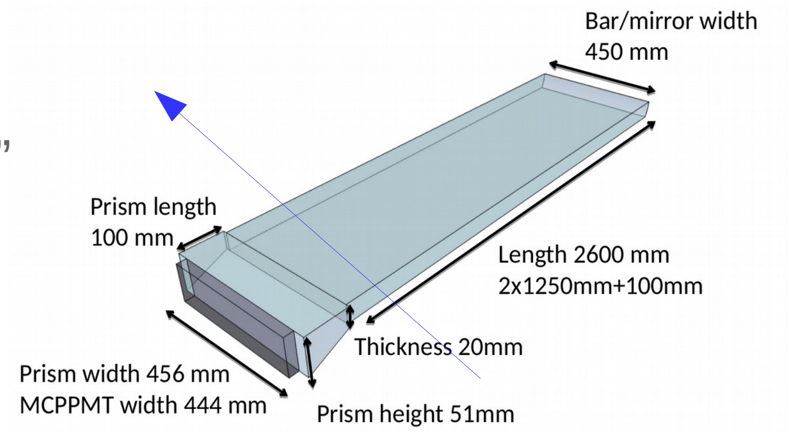
- Intrinsic resolution <100ps on most channels
  - Laser jitter, pulser reference included (but small)
- Dominated by electronic noise in signal chain due to PMT operation at low gain

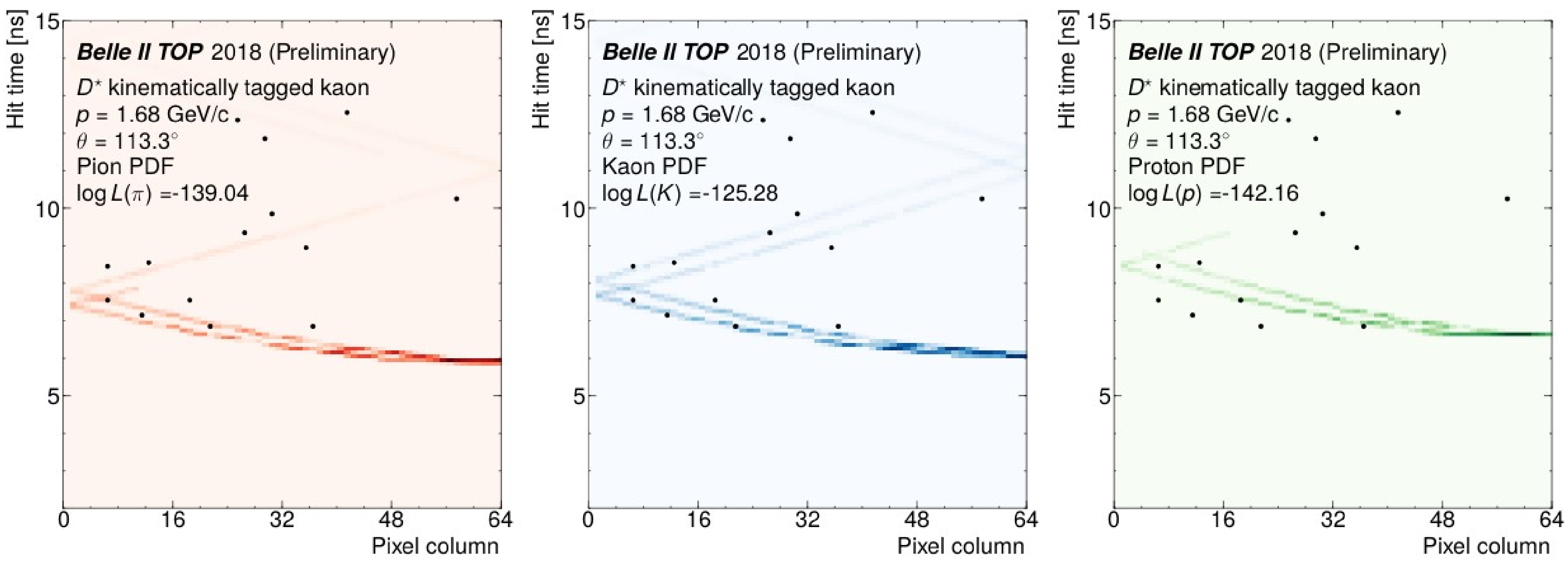


# TOP “Cherenkov Rings” I

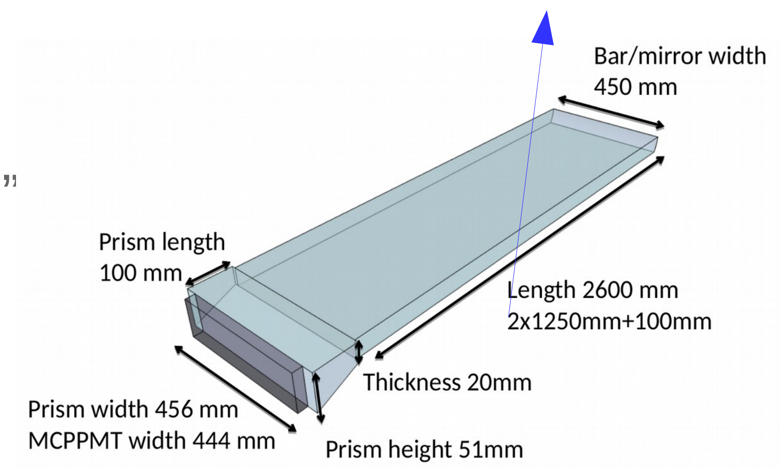
- $D^{*+} \to D^0 \pi_s^+; D^0 \to K^- \pi^+$ “Nature’s MC truth”
- Kaon facing prism-side of TOP bar
  - Little room for Cherenkov cone to open up
  - PDF differences dominated by ToF offset

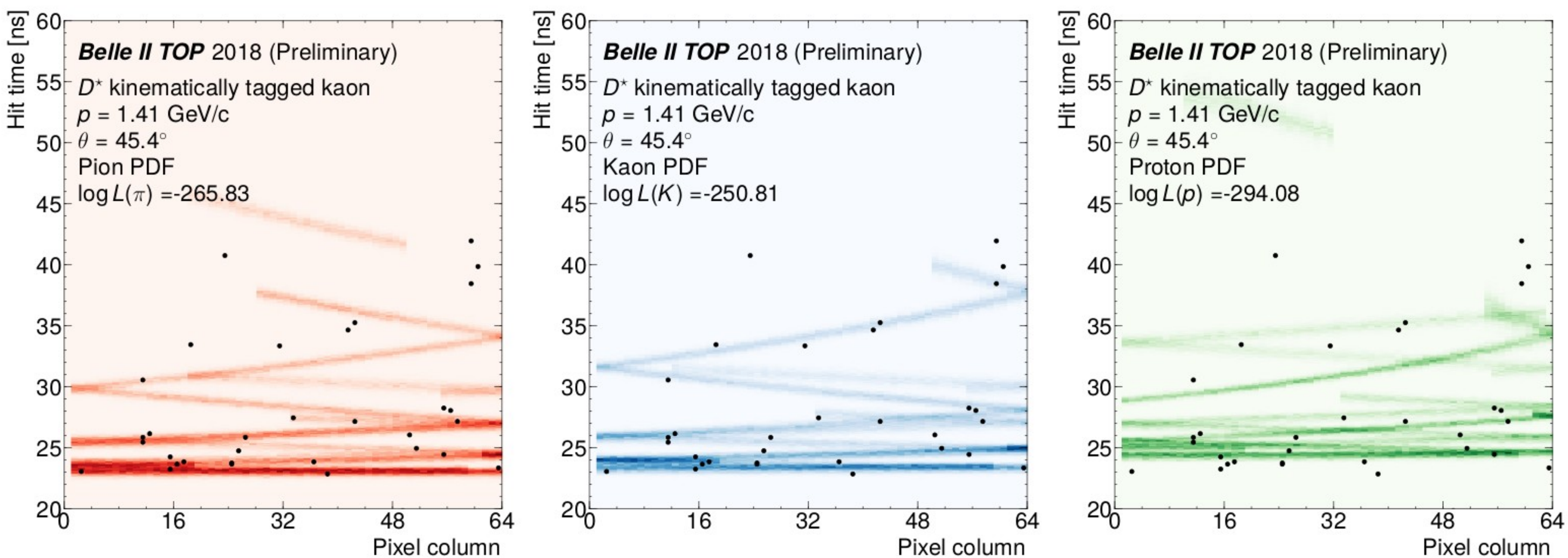


# TOP "Cherenkov Rings" II

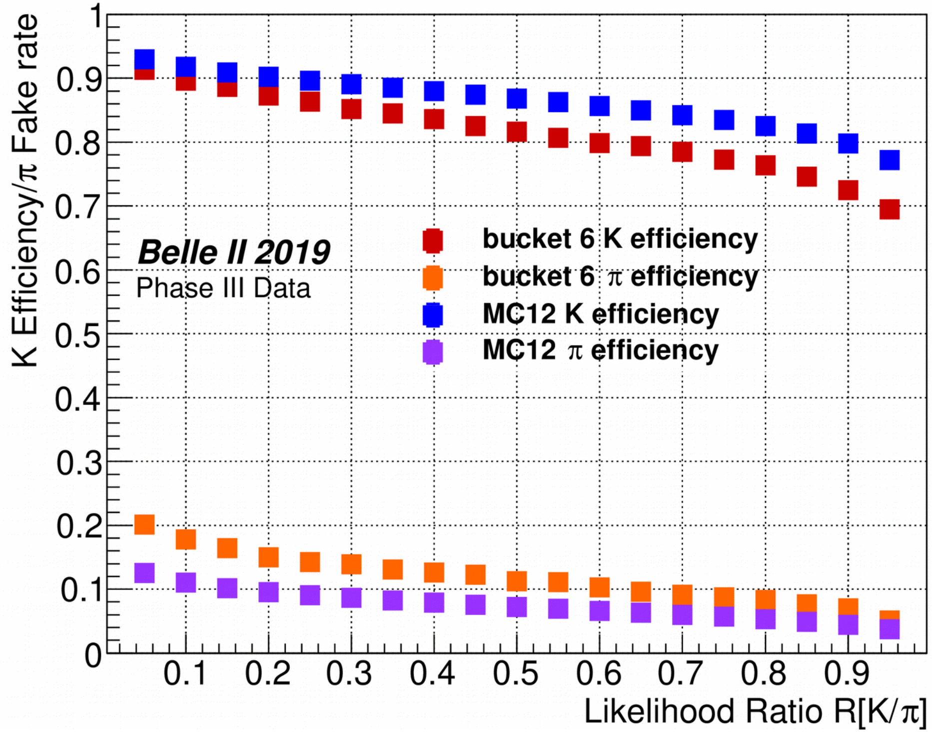
- $D^{*+} \to D^0 \pi_s^+ ; D^0 \to K^- \pi^+$ "Nature's MC truth"
- Kaon facing mirror-side of TOP bar
  - PDF differences dominated by shape



# TOP PID Peformance: K-π Separation

**VERY PRELIMINARY**

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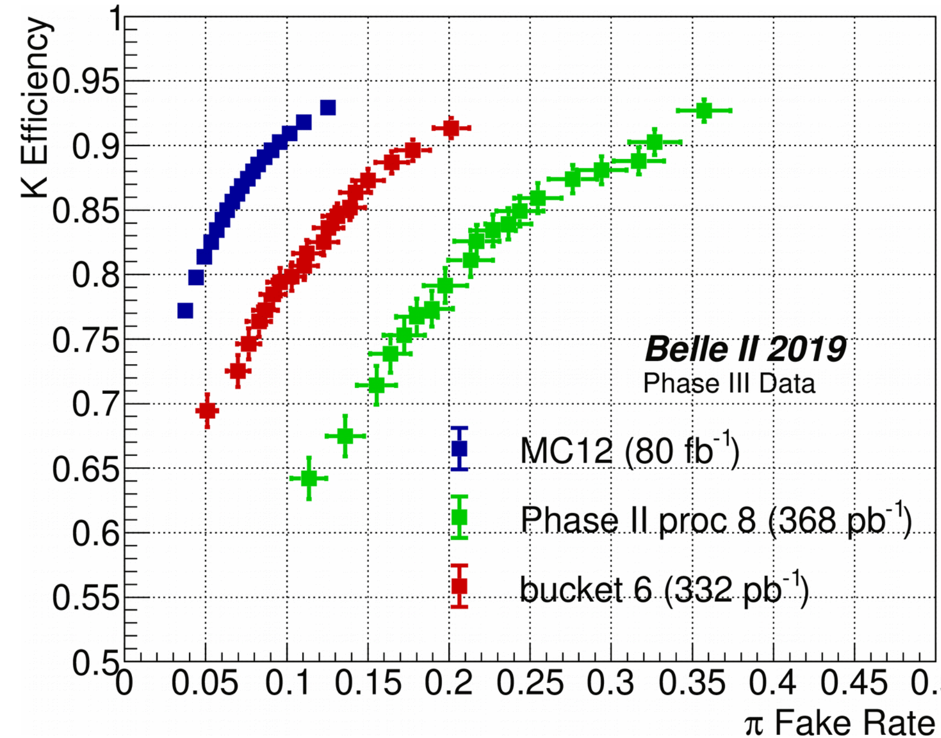

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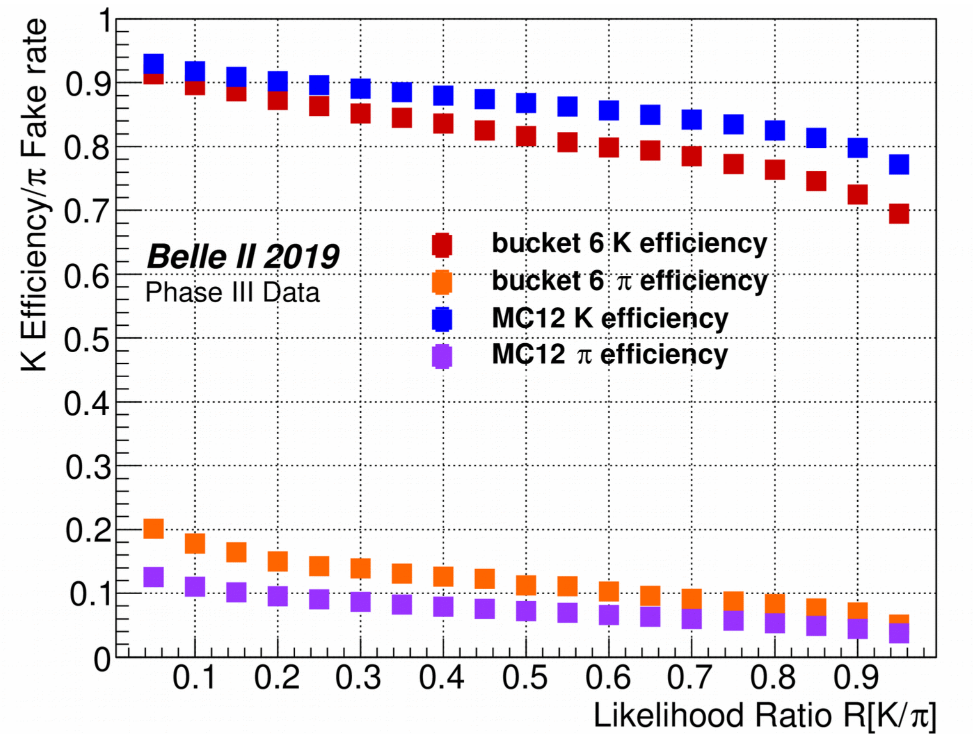


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