Status of ECL DAQ

Trigger DAQ workshop, 2019.08.26

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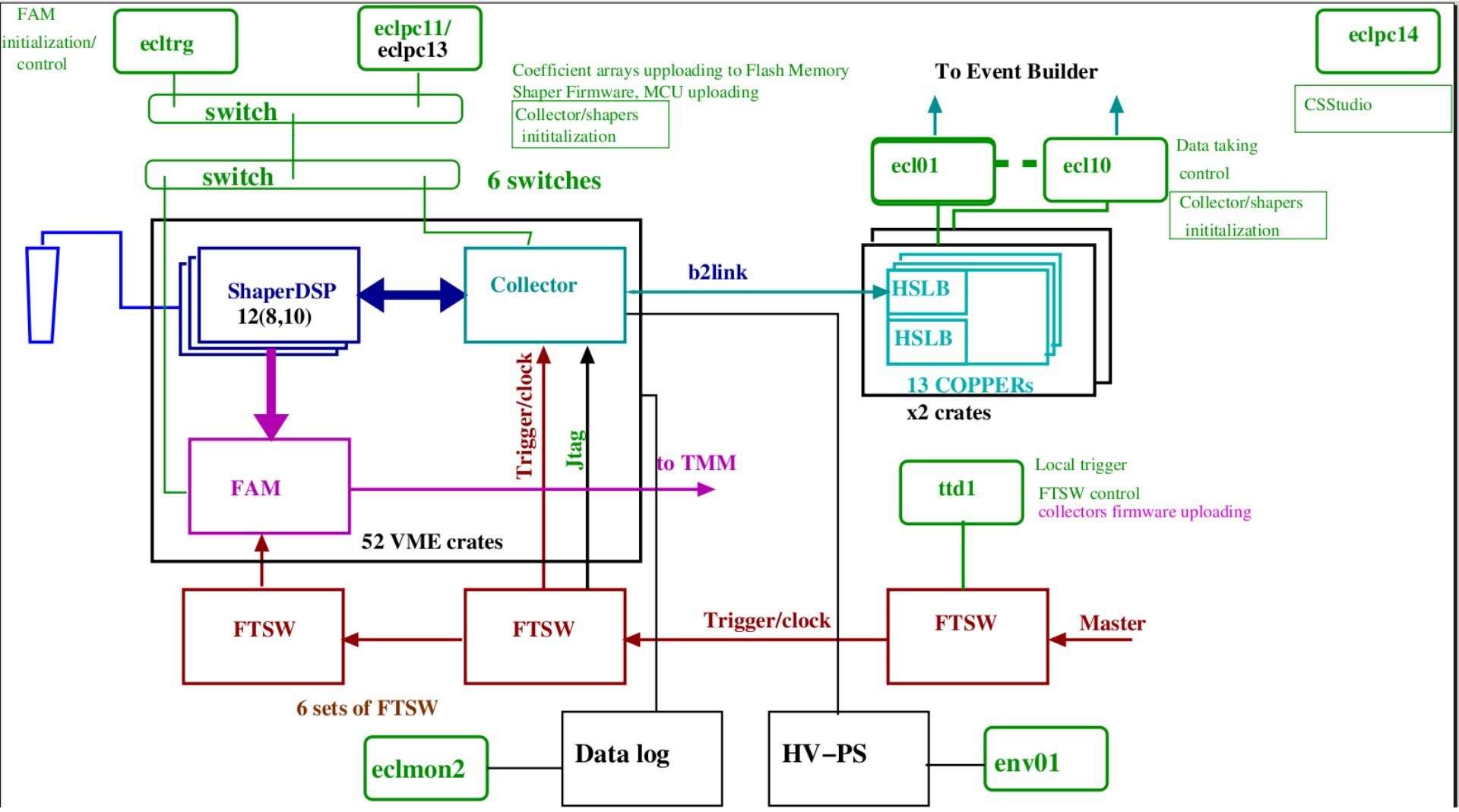
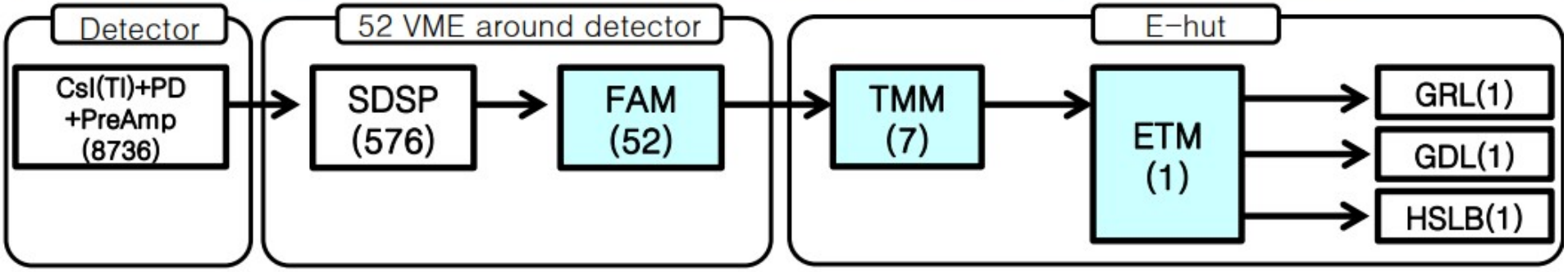
- **Belle II calorimeter DAQ**
- **Status of ECL DAQ and electronics**
- **On-line calibrations**
- **DQM**
- **Problems in phase 3**
- **Summary**

ECL DAQ scheme



Belle2 ECL trigger system

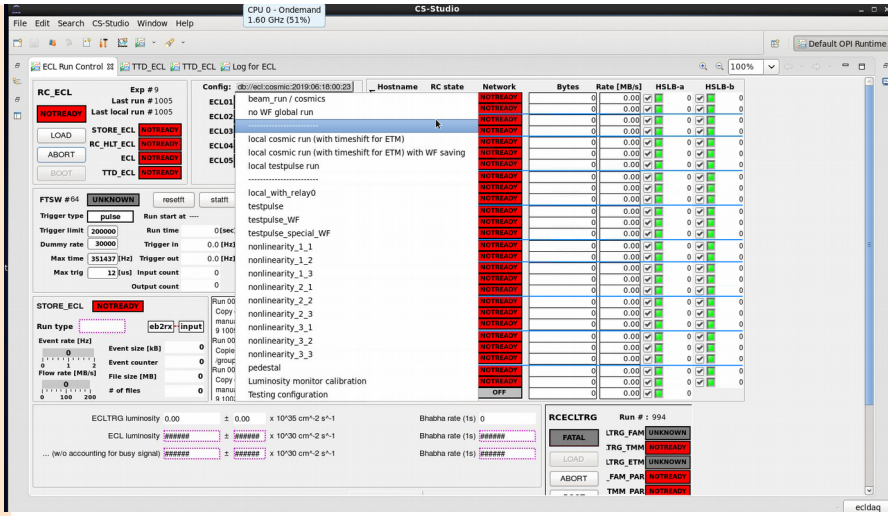


- FAM
  - Receive 576TC analog data from ShaperDSP
    - 1TC consists of 4x4=16Xtals
  - Digitization with FADC
  - TC E&T rec. by waveform analysis(χ^2 fit) on kintex7
- TMM
  - Play an role of merger on kintex7
- ETM
  - ECL trigger decision by all TC E&T on virtex6
  - Send ECL trigger summary to GDL
  - Send cluster data to GRL
  - Send fired TC E&T and trigger summary to HSLB

ECL preparation for data taking

-Upload coefficients array and shaperDSP firmware to collector flash memory (~once a month procedure)

-Upload collector firmware:
  -After power cycle from flash memory
  -via FTSW on ttd11 to flash memory or to FPGA directly.

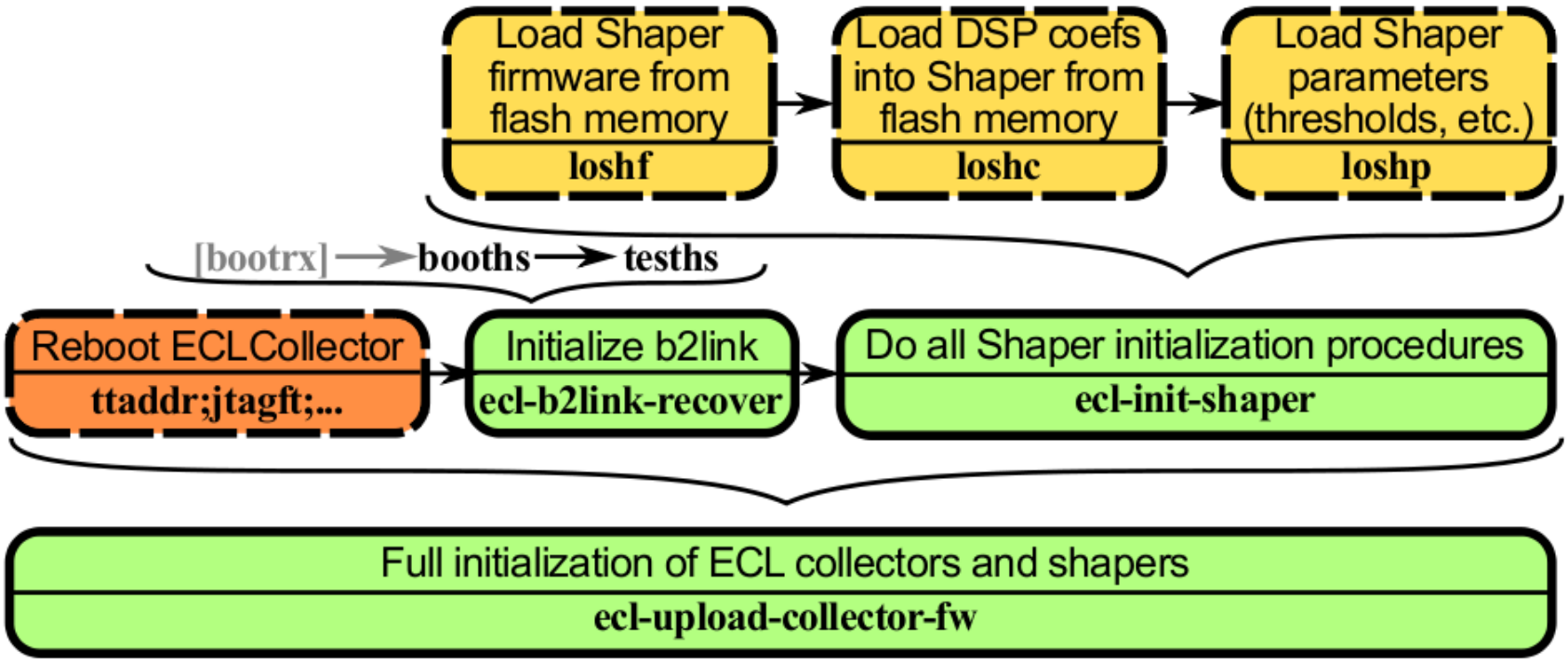


-Establish b2links with HSLB

-Upload shaperDSP firmware from FM to shaperDSP
-Upload coefficient array for FPGA algorithm to shaperDSP
-Set ShaperDSP parameters (ADC work, attenuation coefficients etc.)

-Select data taking configuration
-Load specific collector and shapers paramenters (signal location, energy thresholds,)

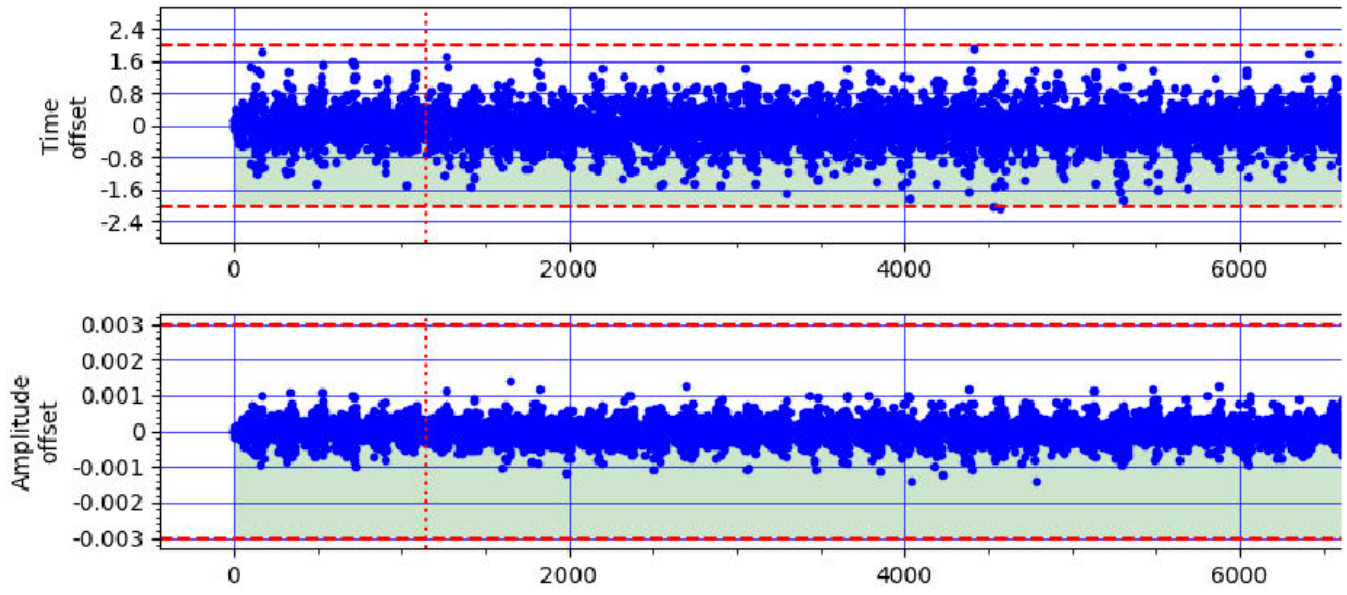
ECL initialization



- ECL expert shifters normally use utilities listed in green rectangles.
  - There is also a script to restart SLC processes, should be switched to "official"restart scripts.
- ECL initialization tools support custom masking (like `ttaddr -m` option)
  - Masks can be set by crate, copper and trigger group numbers.
  - Example: `ecl-init-shaper cpr5001-5003,cpr5005b,FE1`
- Full initialization takes 3-5 minutes.
- Initialization procedure is documented on Confluence, in ECL expert manual.

Local run

ECL electronics calibration

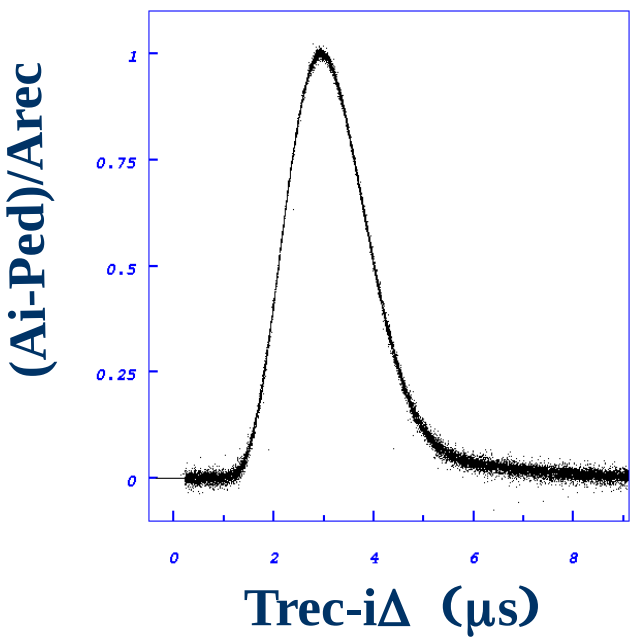


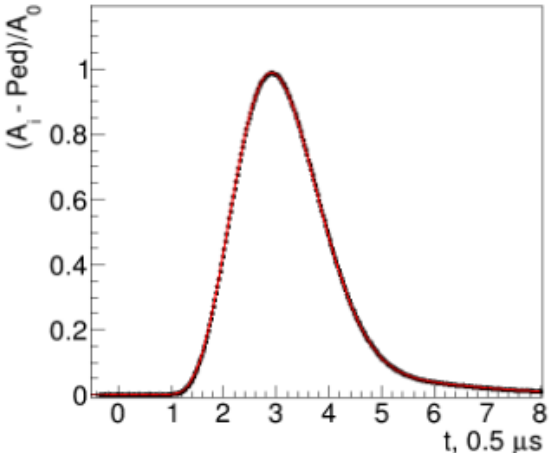
- Sergei Gribanov has provided newer version of ecl calibration shell.
- It mostly focuses on improved usability, the latest version is available at https://stash.desy.de/users/remnev/repos/ecl-local-run-calib/browse
- It's not currently used by ECL expert shifters, plan to switch to it after more careful testing.

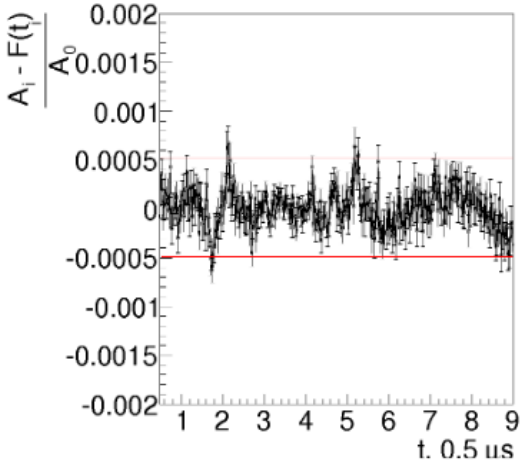
Test pulse calibrations are carried out every day.
In case time changed > 1 ns (2 bins) or amplitude changed >0.3% calibration coefficients are updated

Signal shape calibration

-Taking data with waveform for every hit with E>Eth(50 MeV)
-Calibration of each counter was performed
-Using reconstruction Trec and Arec the shape can be obtained and parameterized







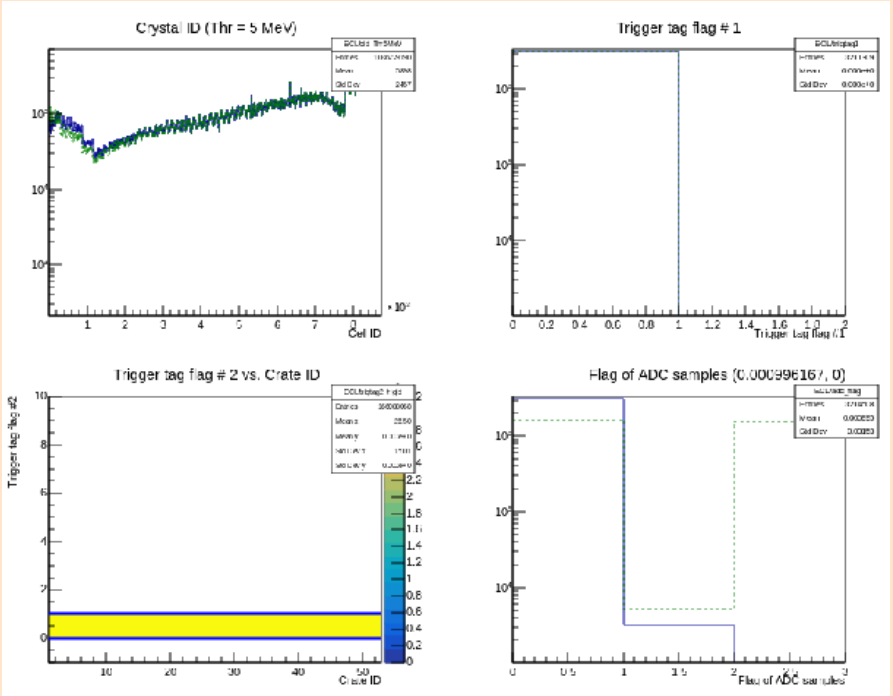
Using the obtained shape parameters +
Covariance noise matrix obtained for beam data
The coefficients arrays for each shaper are obtained

ECL DQM

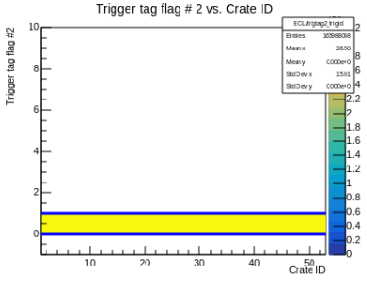
- https ://confluence.desy.de/display/BI/DQM+Manual+for+Shifters

-Test each counters provides signal
-Time of the signal is correct
-Shapers headers are consistent
-FPGA logic works correctly
-Triggers come uniformly
-Hit number in event is reasonable
-Energy distribution is reasonable
-Fraction of ADC data is reasonable

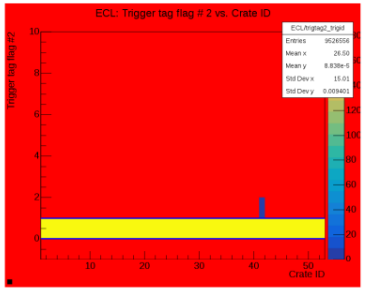
Problematic case – call to ECL expert



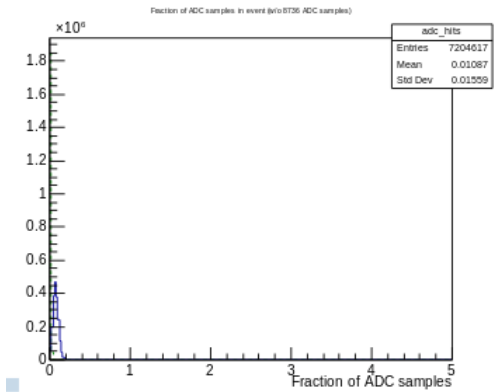
- Tag flag # 2 controls transition of event number from ECLCollector t shapers.
- Flag "0" - correct event number
- Flag "1" - problem

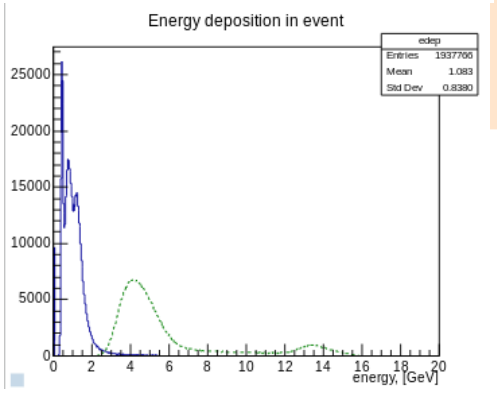


Good run



Bad run



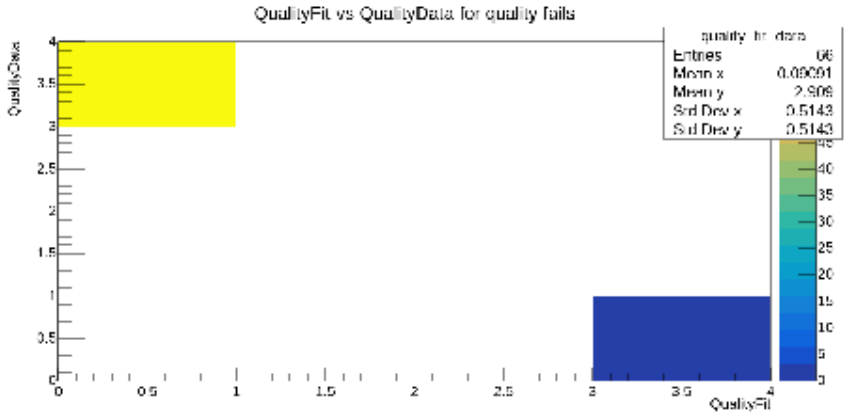


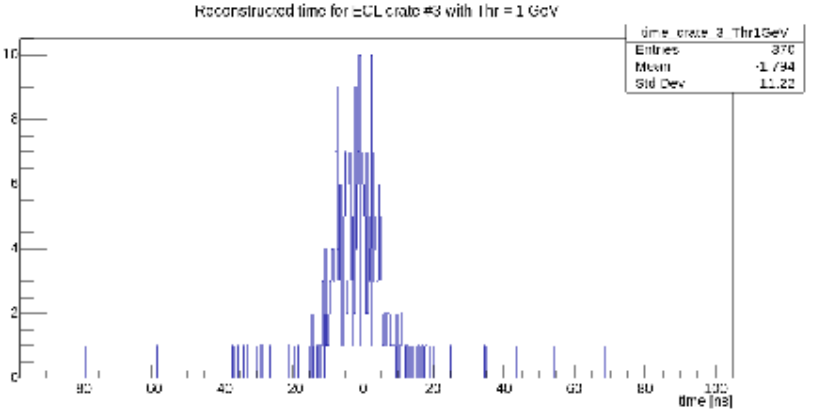
ECL DQM expert histograms

- We have many expert plots which control timing, logic, pedestals.
- A detailed manual is available at :
  https ://confluence.desy.de/display/BI/ECL+DQM+instructions

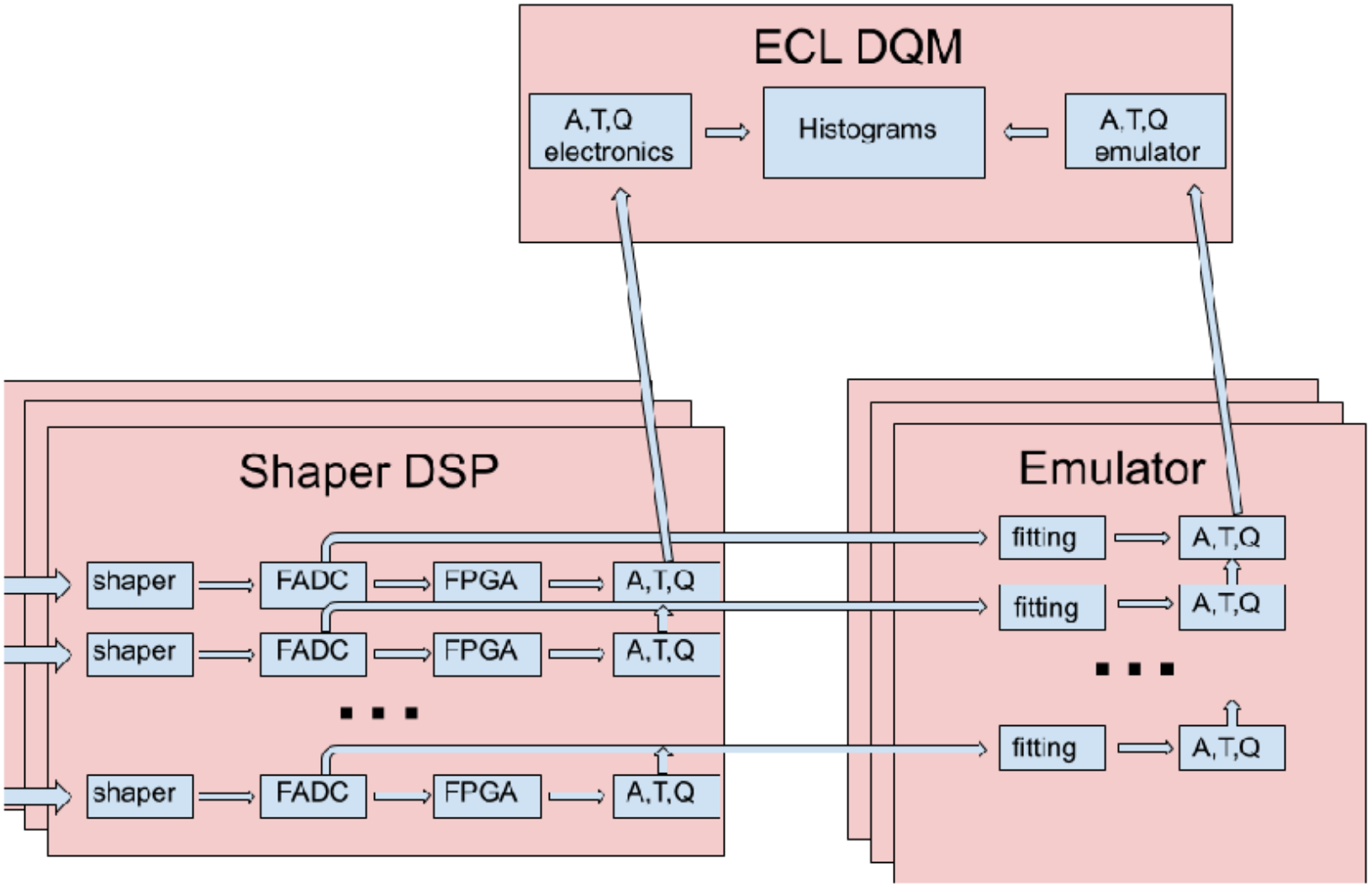
ECL

- ECL_Main
- ECL_Pedestals
- ECL_Timing_Barrel_Endcaps
- ECL_Timing_Crate_1-24
- ECL_Timing_Crate_25-48
- ECL_Timing_Crate_49-52
- ECL_Logic_Overview
- ECL_Logic_Amplitude
- ECL_Logic_Time
- ECL_Logic_Mismatches

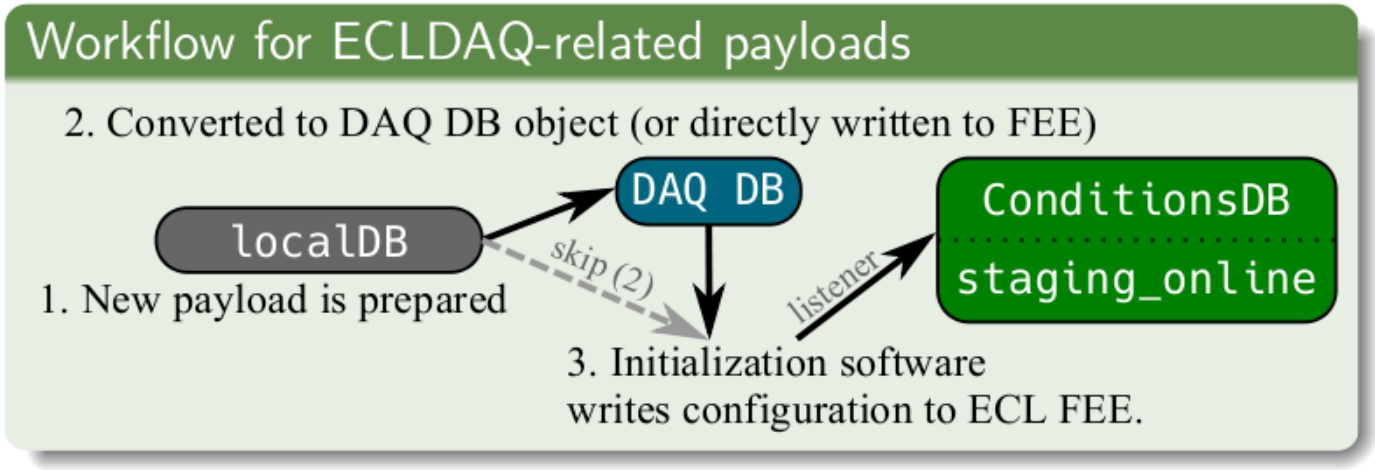




ECL logic test



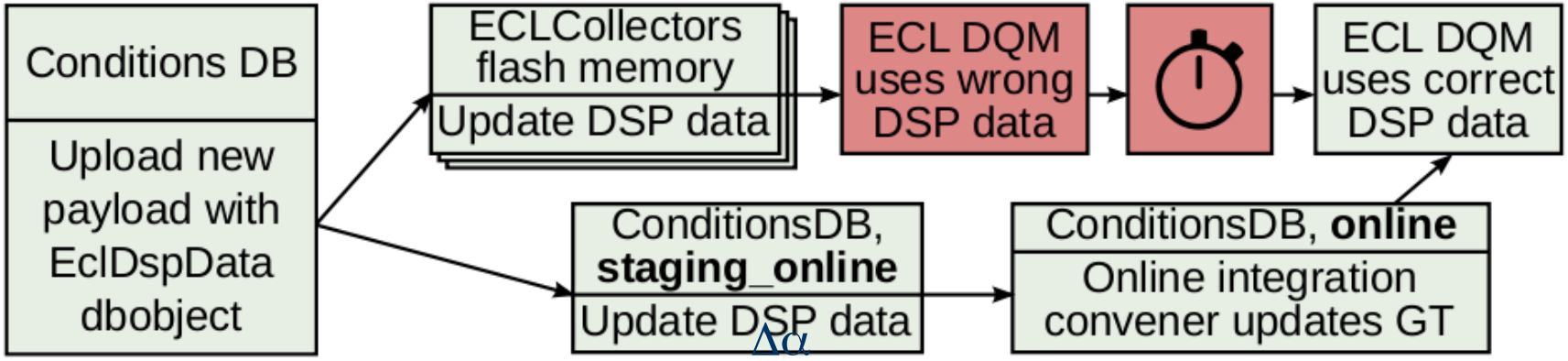
Management of ECL configuration



ECLDAQ-related payloads in Conditions DB.

- ! ECL DSP data.
  Updated if: New DSP coefficients are uploaded to Shaper flash memory. Update procedure is not very clear. **It is important to use the same set of DSP coefficients in front-end electronics and in DQM**. Otherwise, DQM will show false positives on data corruption detection.
- ECL channel map.
  Updated if: Cable swaps are detected.
- ECL energy thresholds.
  Updated if: New energy calibration is available.
- ECL attenuator coefficients.
  Updated if: New version is generated by ECLTRG experts.

Data base synchronization



- ShaperDSP logic check in ECL DQM depends on the version of DSP coefficients written to electronics.
- Thus, it is crucial to synchronize versions between DQM and electronics.

Problems in run 3

-Hardware problems with 4 counters + 1 collector (were solved)

-Not all crates were recorded ADC data and random trigger data

-ttlost for crate #4

-wrong TAG problem

-ECL busy for beam bursts when ADC data are stored

-ECL background overlay data were stored for random trigger only

Hardware problems

Two counters showed instability

-Junk was found in connector - cleaned

-One preamp is dead - was disconnected, ½ amplitude

Two unstable shaperDSPs were replaced

-One capacitor replaced

-No reason found – under study

Collector was replaced

-workable, problem was in TTD cable connection

Run initialization problem

To initialize the record of ADC data bit should be recorded in certain register:

-first the value 0 was recorded

-depending on the run type proper bit mask was set

Sometimes the mask was written incorrectly.

It was reason why ADC data and random trigger data were not recorded for some crates.

Was modified:

-depending on the run type bit mask was set

-error analysis was added

In the end of run3 everything have been working properly

The careful test of the registers is under study

ttlost problem

ttlost happened for crate #4 just after power cycle or collector firmware reload.

After several ttlosts the connection became stable.

After cable unplug/plug the problem has disappeared.

We continue to monitor the stability

ECL background overlay data

Firmware we had in phase 3 allowed to store ADC data for random trigger type 7 only.

New version of firmware allows to store ADC data for any trigger types combination .

The trigger types which will be stored are set by 16-bit word

1 bit corresponds to certain trigger type (0 - 15)

Wrong TAG problem new firmware features

Wrong TAG problem:

Sometime the shaper data of previos event were combined with current event. It was monitored in DQM.

Bug in firmware was found and fixed.

New firmware features:

Possibility to read the shaper relays status from ShaperDSP was added.

Easy to know the status of ECL calibration/normal state.

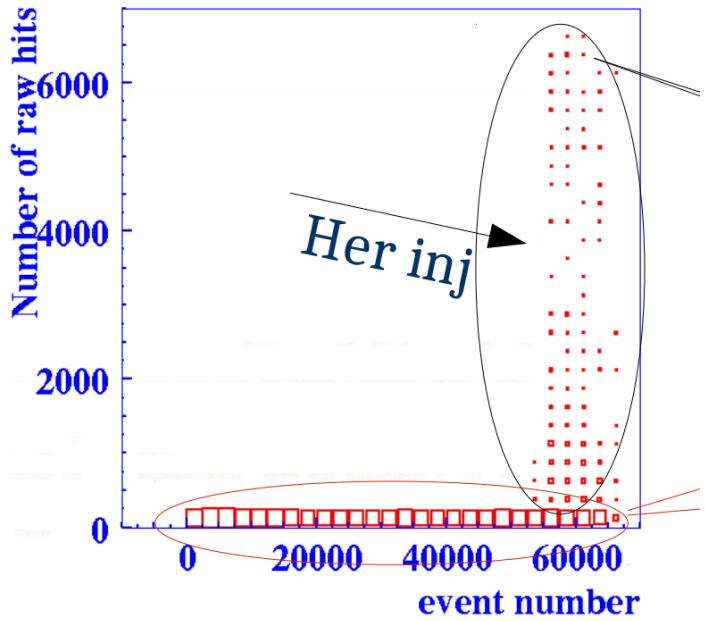
Possibility to read the attenuation coefficients from ShaperDSP has been added.

Beam burst problem

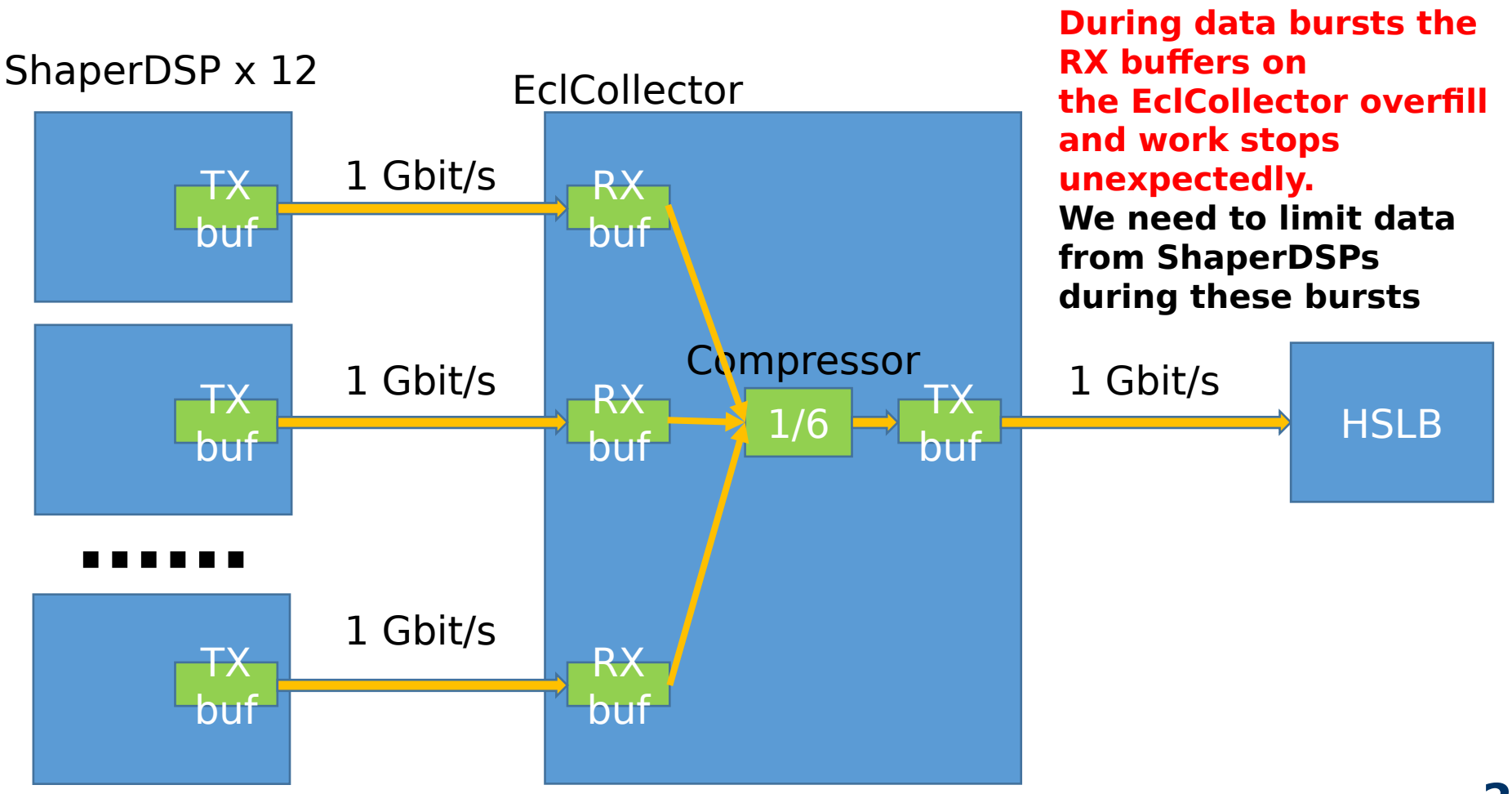
-If no ADC data recorded – no problem

-If steady run with ADC data record – no problem

-In case of bad injection or beam burst +ADC data record – ECL busy



ECL Infrastracture

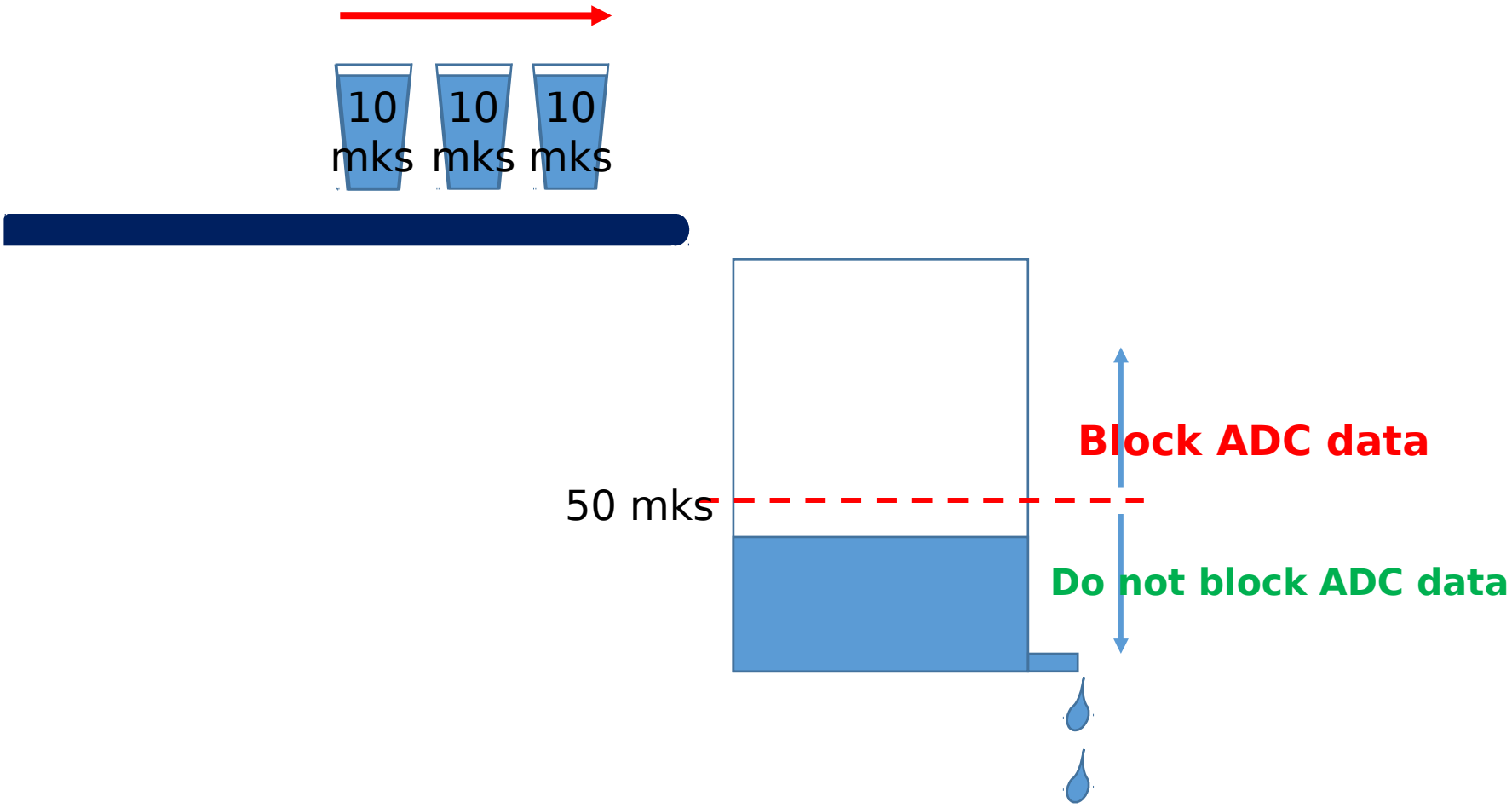


During data bursts the RX buffers on the EclCollector overfill and work stops unexpectedly.
We need to limit data from ShaperDSPs during these bursts

Burst data suppression algorithm on ShaperDSP side

- The ECL system can output 1 event with all ADC data without stop but there should no ADC data requested for some time after that till all buffers are empty (or almost empty)
- The most recent Shaper firmware contains a Timer that blocks the ADC data output.
- Every waveform increases this timer by NSTEP mks (NSTEP (10) is set by register). If there are several waveforms output for some event the total increase = NSTEP x HIT_NUMBER, where HIT_NUMBER – number of channels with ADC data appended for this event.
- The ADC data saving suppresed while timer is higher than some threshold NTHR mks (30 - 50 for an example). This threshold is needed to pass ADC data for sparse hits during normal operation. Otherwise even 1 hit will block ADC data for the next event
- Events with suppresed ADC data are marked in the header of the ShaperDSP data packets

Algorithm diagram

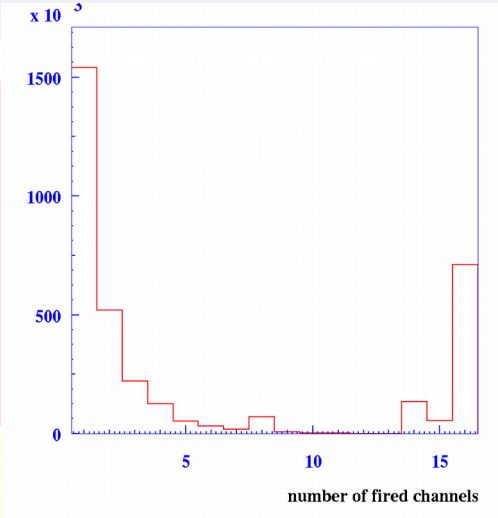


Beam burst test/simulation

-The algorithm was tested with testpulse data 30 kHz poison trigger

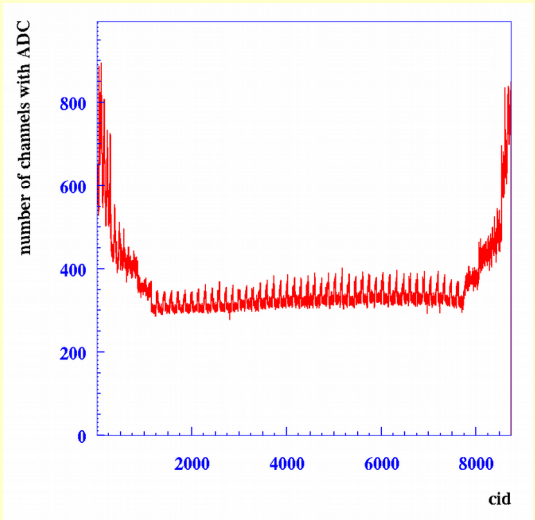
-DAQ works stably for value of NSTEP=10 mks NTHR < 60 mks

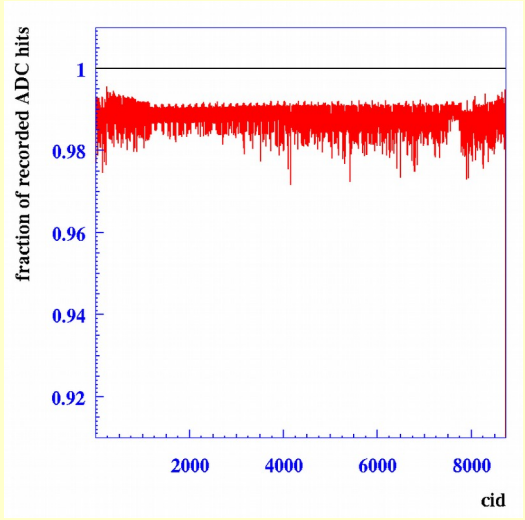
-We select NSTEP=10 mks NTHR = 30 mks

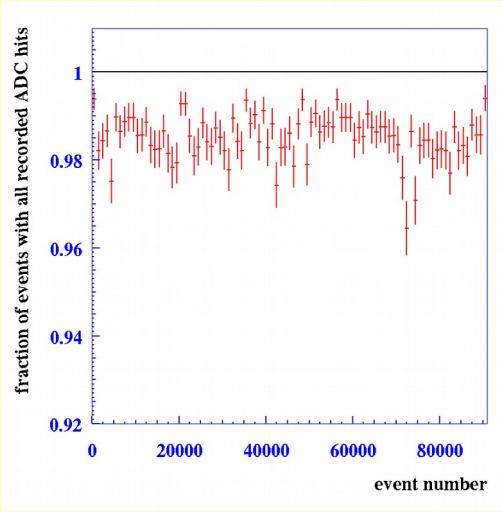


-Run #1131 with ADC record was taken

-The described algorithm was implemented + scale to 30 kHz trigger







-The lost of the ADC data ~1.2% at 30 kHz

DAQ software modification

-Update software to fit new firmware

-New options:

  -indication of normal/calibration mode (relay status)

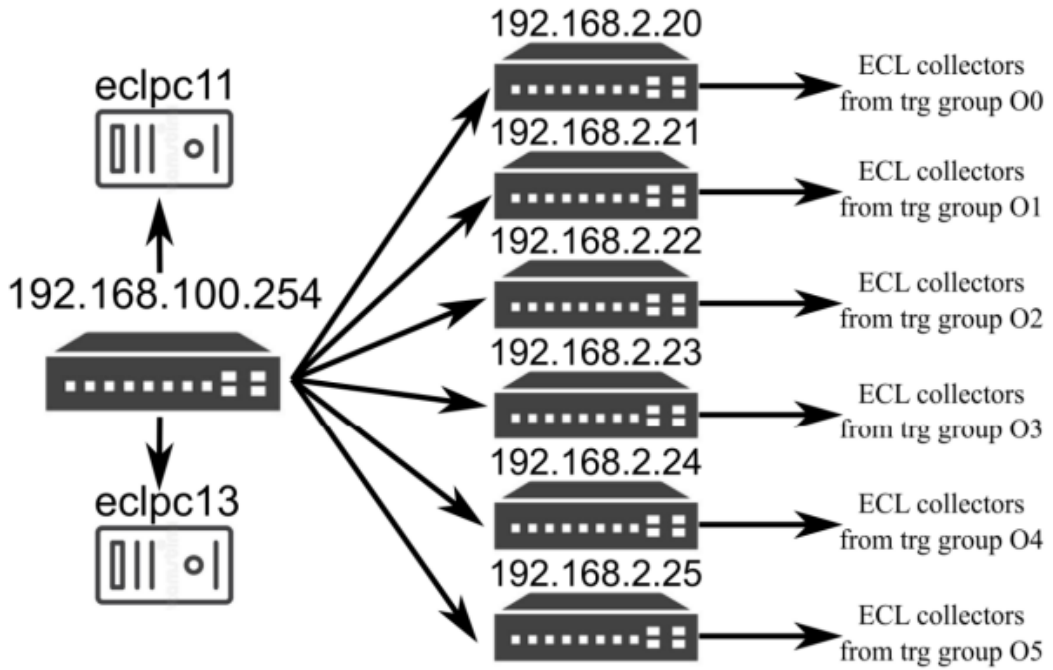
  -test of the attenuation coefficients set in ShaperDSP

-To improve work with network switches for collector

ECLDAQ, Ethernet-related problems

Since ECL initialization is partially done over Ethernet, these problems can create unexpected delays.

- On some versions of ECL collector firmware, Ethernet requests during data-taking cause data corruption.
  Possible solution: Simple Selenium-based command-line utility was implemented to block/unblock connection to ECL collectors over 7 network switches.
- Sometimes, after the reboot, ECL collectors become inaccessible over Ethernet for ∼10-15 minutes (this problem is rare and hard to reproduce).
  Possible solution: Disable DHCP, assign static addresses to the collectors.



Summary

-ECL DAQ works stably

-DQM histograms allow to monitor stable data taking

-Most of phase 3 problems have been solved

-Collector and shaper firmware have been updated and its stability is being tested

-Update of the ECL DAQ software is under work