# TRG DAQ, SLC and monitoring

T.Koga

# TRG readout

-GDL, GRL and CDCTRG are in TRG readout

-22 UT3 boards

-CDCTRG: only 1/x events are recorded (event supression)

2019 Spring, x=256

-In total, ~20MB/sec @ 5kHz

| UT3 | copper | #bit | clk window | byte/event/UT3 |
|---|---|---|---|---|
| 2D0,1,2,3 | 11001,2 | 4096 | 48 | 24588/x |
| 3D0,1,2,3 | 11003,4 | 2048 | 48 | 12300/x |
| NN0,1,2,3 | 11005,6 | 2048 | 48 | 12300/x |
| TSF0,4 | 11007 | 2048 | 48 | 12300/x |
| TSF1,2,3,5,6 | 11008,9,10 | 4096 | 48 | 24588/x |
| GDL | 15001 | 640 | 32 | 2584 |
| GRL | 15002 | 1024 | 1 | 128 |

-ECL(TOP)TRG is in ECL(TOP) readout

# TRG B2L problem in phase3

-Bug of event suppression logic for CDCTRG
- -Taken CDCTRG data has problems: event slip etc.
- -Fixed the bug in the last month. No problem in local test.
- -All CDC modules will be re-compile with new TRG B2L library.

-B2L error of ETF
- -ETF data reach HSLB later than others. Reason is unknown.
- -June 2019, ETF is masked. Keep to mask in Autumn.

-Bit shift of B2L data from GDL
- -Taken GDL data sometimes (<~0.3%) has bit shift problem
- -Fixed the bug in the last month (common bug as CDCTRG).

# TRG problem stopping DAQ for long time in phase3

-May 2019: VME parameter error

- -Wrong parameter is set to GDL through VME
- -Stop DAQ ~1day
- -Temporary solved by checking parameter automatically (if wrong parameter is set, TRG status cause error.)
- -Reason is still unknown. In GDL firmware, way to access VME is being modified.

-May 2019: LVDS connection error btw. GDL and GRL

- -Signal through LVDS is sometimes broken
- -Stop DAQ ~12hours
- -Solved by widen clock length of the signal

# TRG problem stopping DAQ short time (but many times)

-1. BUSY from GDL
 -Recovered by SALS.
 -Reason is unknown. Maybe back pressure, or Maybe TRG.
 -High rate test is needed for further investigation

-2. ttlost
 -Recovered by SALS.
 -Reason is unknown. No investigation is done so far.

-3. One of NSM node (TRGREADY) stuck in NOTREADY
 -Lost communication to other nodes and cause error
 -Fixed by allocating non-continuous communication error
 in June 2019

# TRG problem stopping DAQ short time (but many times)

-4. CDCTRG dataflow is down due to CDCFE or merger

- -Reason is unknown. Recovered by masking problematic CDCFE/merger.
- -Automatic masking script is prepared for TRG expert (but still need help of TRG expert. not recovered by SALS.)

-5. GDL lost signal from ETM.

- -Reason is unknown. Recovered by rebooting GDL. (Need help of TRG expert. not recovered by SALS.)
- -We replaced GDL<->ETM connection from GTX to GTH in the last month. Stability test will be done.

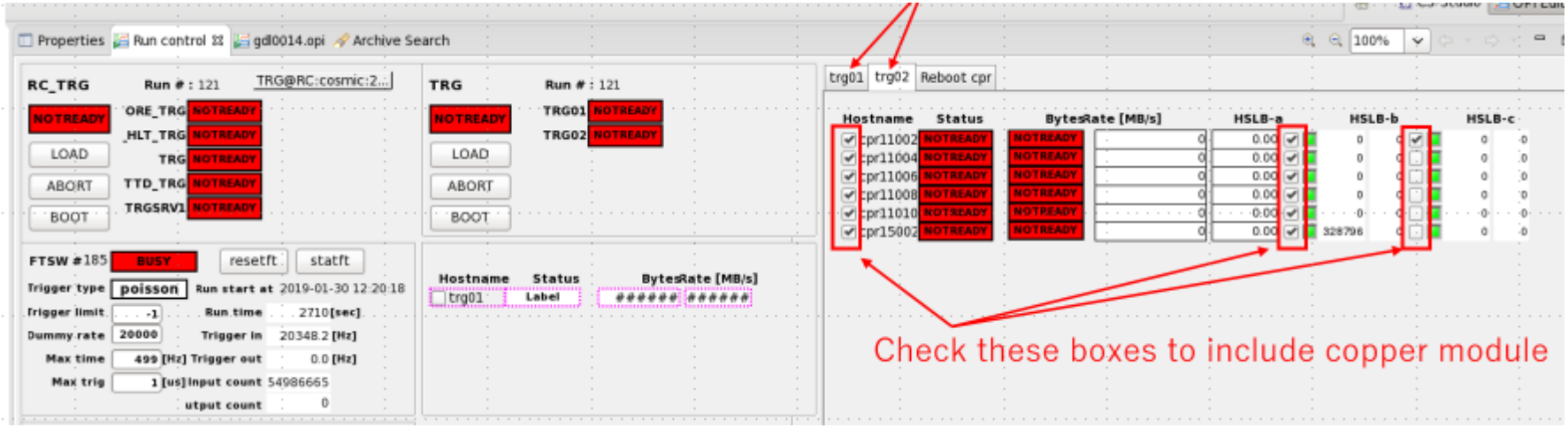
# GDL full readout plan in Autumn run

-GDL readout data is time integrated at present.
4bit(127MHz) -> 1bit(32MHz) to reduce data size.

-Full readout will be added in debug mode in Autumn run
- -4 B2L lines from one UT3 board
- -4 more HSLB (cpr15003ab,4ab), 2 or more ropc, and 4 more FTSW are needed
- -firmware is being tested
- -apply scale factor to reduce datasize

# Status of TRG slow control : GUI

-Many GUIs are newly added in 2019 Spring:
local run control, TRG status, GDL control, TRGECL status




-Plan:

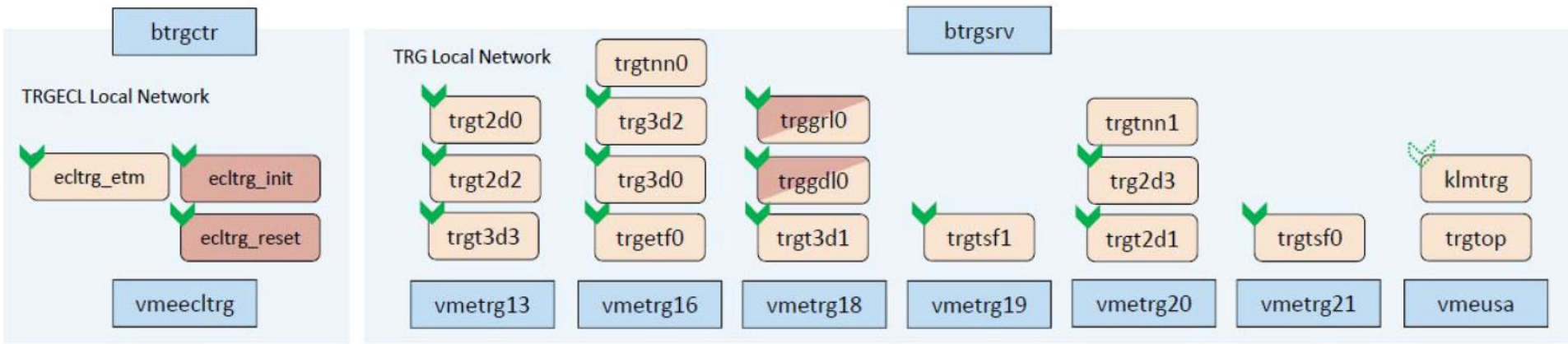
- -Basic GUI panels are all prepared. No big change.
- -Configure GDL based on run type set in global run panel
- -Add reboot button to initialize TRG module and SLC (?)

# Status of TRG slow control: NSM

-NSM is prepared for each trigger module to record/control parameters with VME

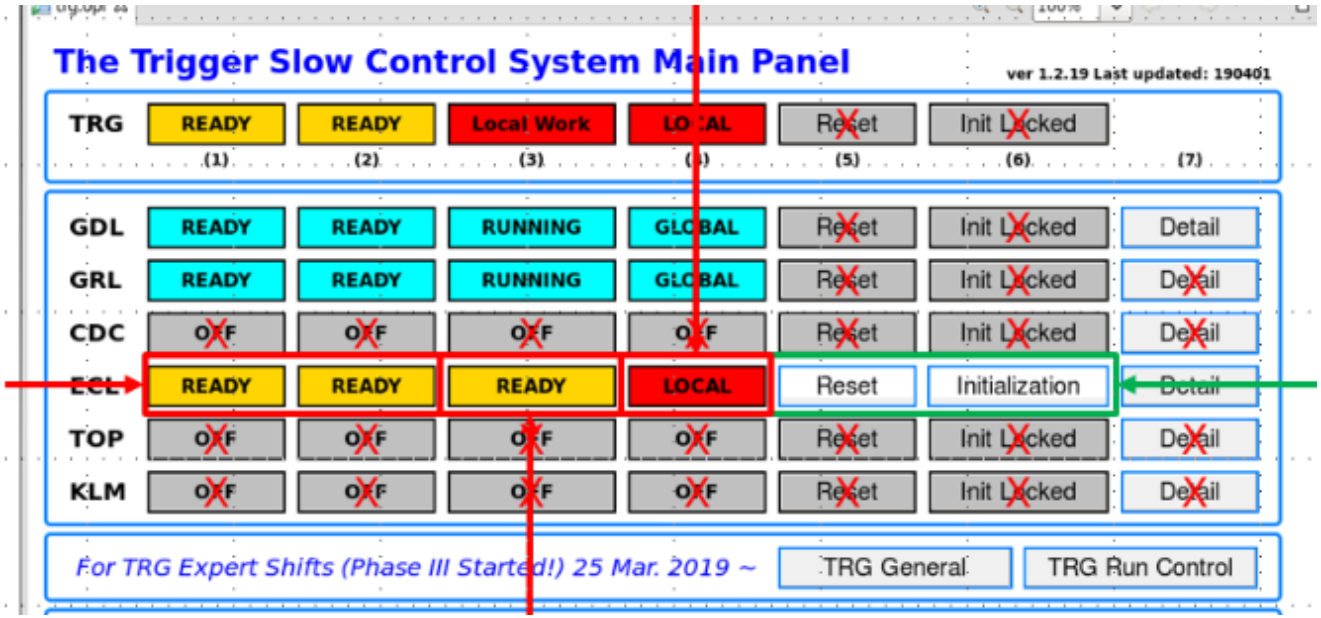
-Followings are still missed: NSM for CDCNN, TOP

Map of NSM nodes and VME



# Status of TRG slow control: NSM

-A NSM node, TRGREADY, is prepared to see TRG status.
Cause TRG error if CDCTRG/ECLTRG/GDL have problem.
Followings are checked:
-CDCTRG dataflow, ECLTRG parameter, GDL configuration

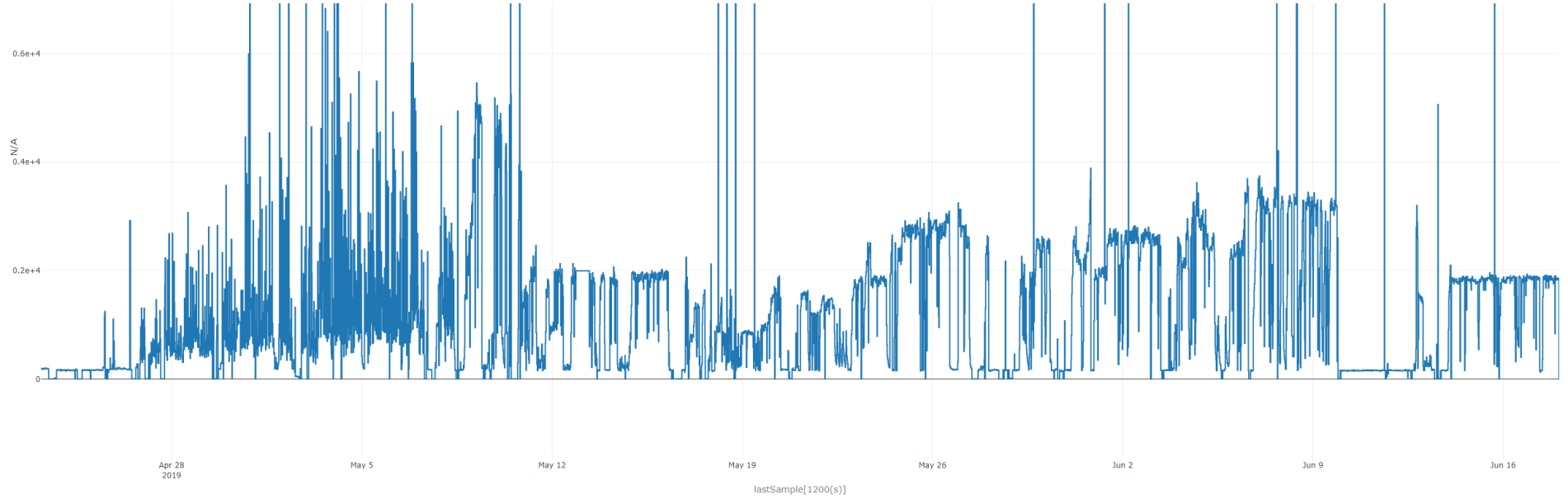



-Plan:
-Error sound is not working properly
-Add TOP and KLM once they are ready
-Prepare reset/recover button (?)

# Status of TRG slow control : archiver

- Archiver is added for TSF, GDL, GRL, ECL to record trigger rate

Example of archived L1 rate




-Plan: followings are still missed

-output hit/track rate monitoring for CDC2D, 3D, KLM, TOP

# Status of TRG DQM

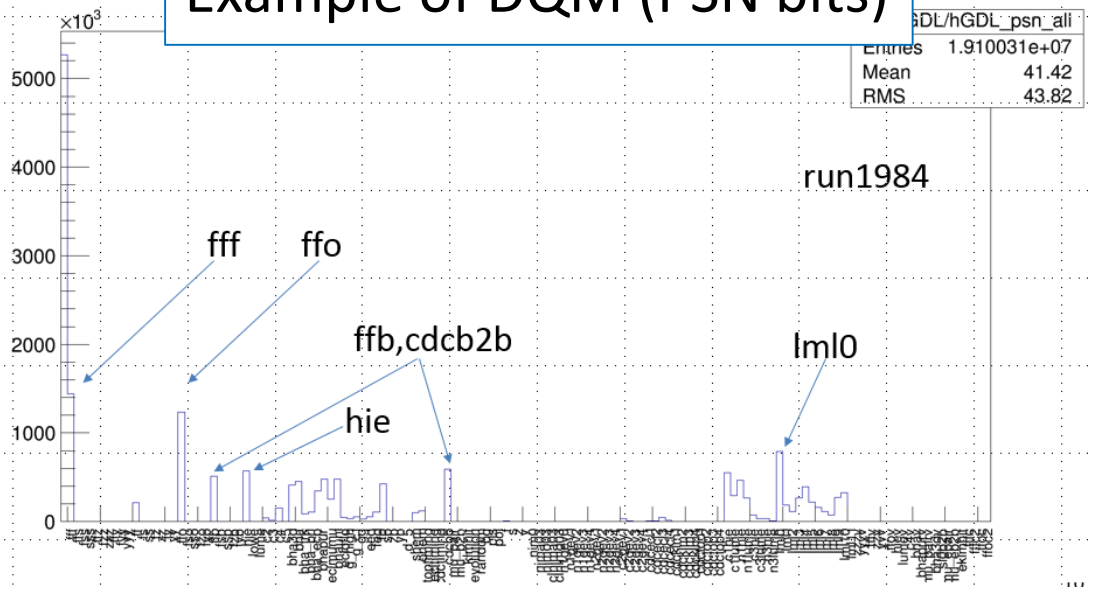
-Following DQMs are added to monitor TRG output:

-2019 spring: GDL,CDCTSF, 3D (TRGECL had been existed)

-2019 autumn: NN, GRL

-Still missed: CDC2D, TOP

Example of DQM (PSN bits)




-Plan

-More simpler DQM plots for CR shifter

-automatic error caution

-Add missed plots

# Status of TRG QAM

-QAM (rundependency )is being prepared

-following ARICH local QAM

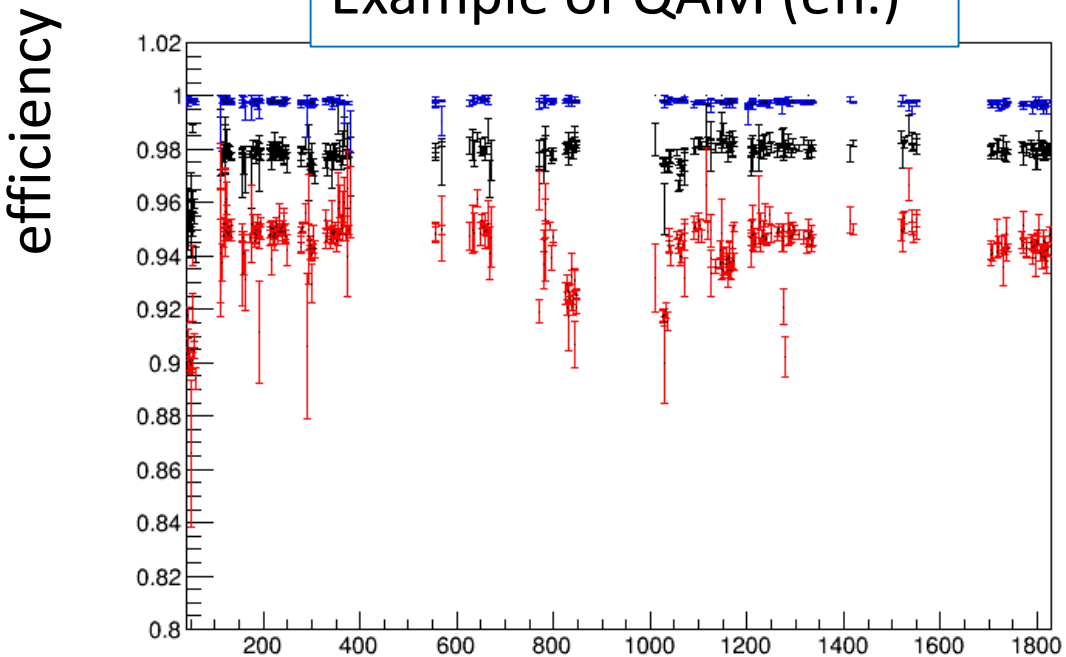
-trigger efficiency, trigger rate, hadron/Bhabha

-quite useful for online monitoring of TRG performance

-High purity skims (HadronB and Dimuon) are needed on HLT

-HLT group (Karim) is working to add them

Example of QAM (eff.)



# Summary

-Status of TRG DAQ, SLC and monitoring are presented

-DAQ
  -status of each TRG DAQ  error and measures
  -new GDL readout will be added for Autumn run

-SLC
  -GUI: required panels are added.
  -NSM: NN and TOP are missed. TRGREADY is added.
  -Archiver: GDL, GRL, TSF, ECL are archived. Others should be implemented.

-Monitoring
  -DQM is added and used for online monitoring
  -QAM will be added for Autumn run

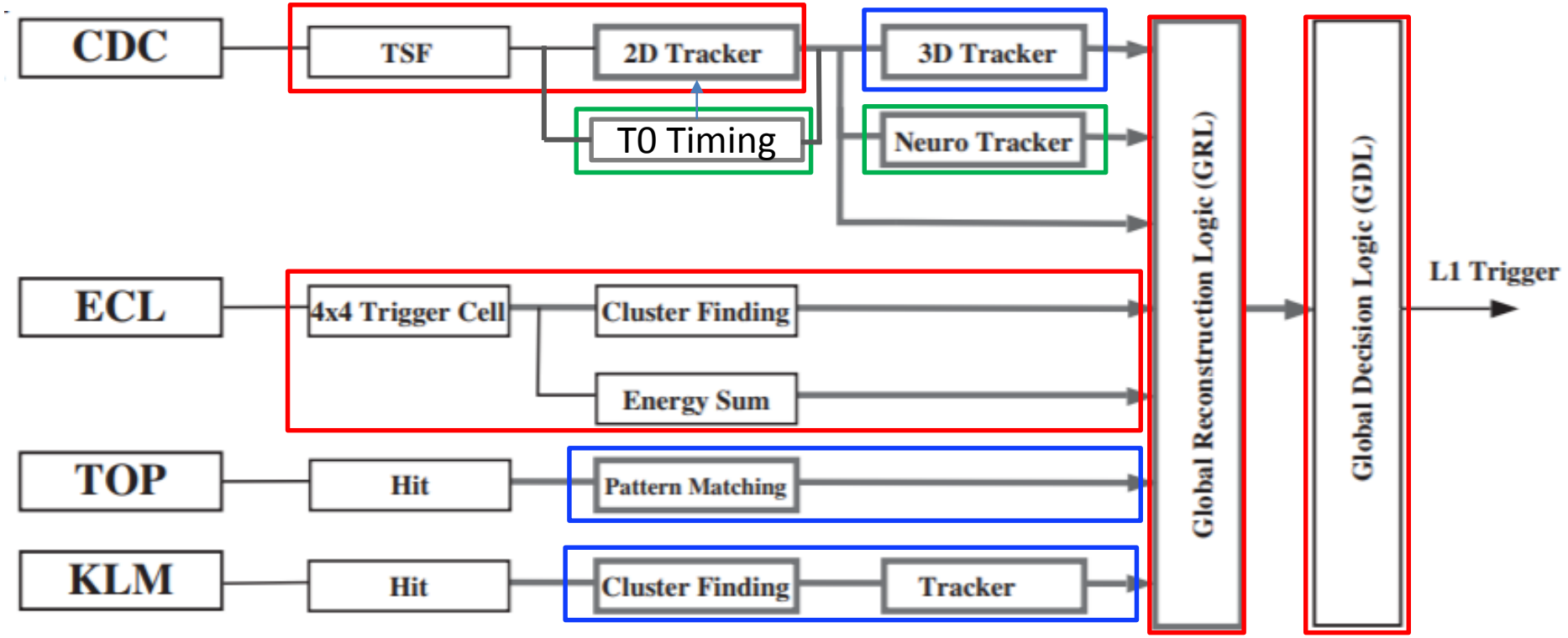
# Backup

# Status of trigger system in phase3

-2019 spring: CDC2D, ECL, GRL, GDL

-2019 Autumn: CDC3D Neuro, CDC timing on 2D

-Under development: CDC3D tracker, TOP, KLM



# L1 rate and efficiency in 2019 Spring

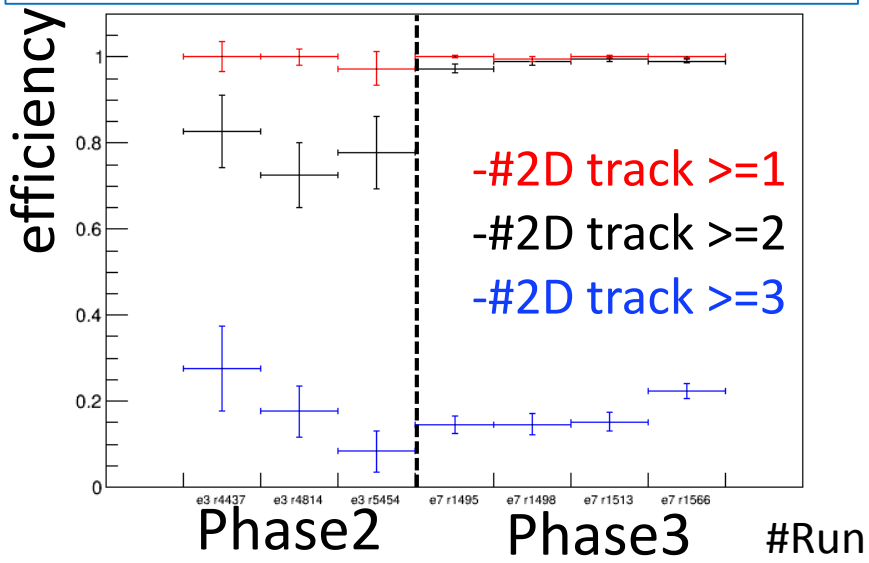
-L1 rate: 2~4kHz, depends on beamBG

-HadronB efficiency: >~99%

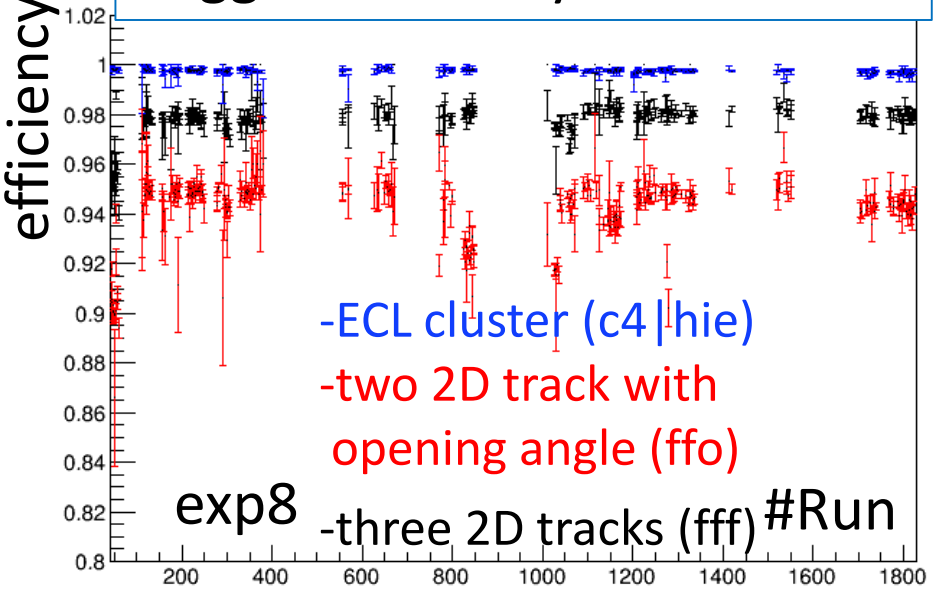
-Dimuon efficiency: ~95%

-Tau efficiency: ~

2D efficiency with Dimuon skim




Trigger efficiency for HadronB



# Status of ECL trigger

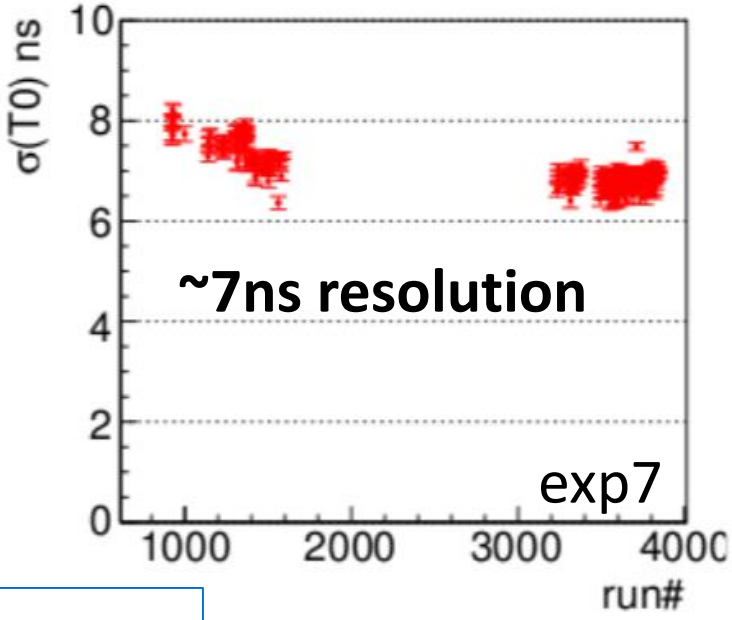
**-2019 Spring: working stably**

- -Improved calibration
- -Improved timing resolution
- -New bits: low multi cluster, μ pair, pur bhabha

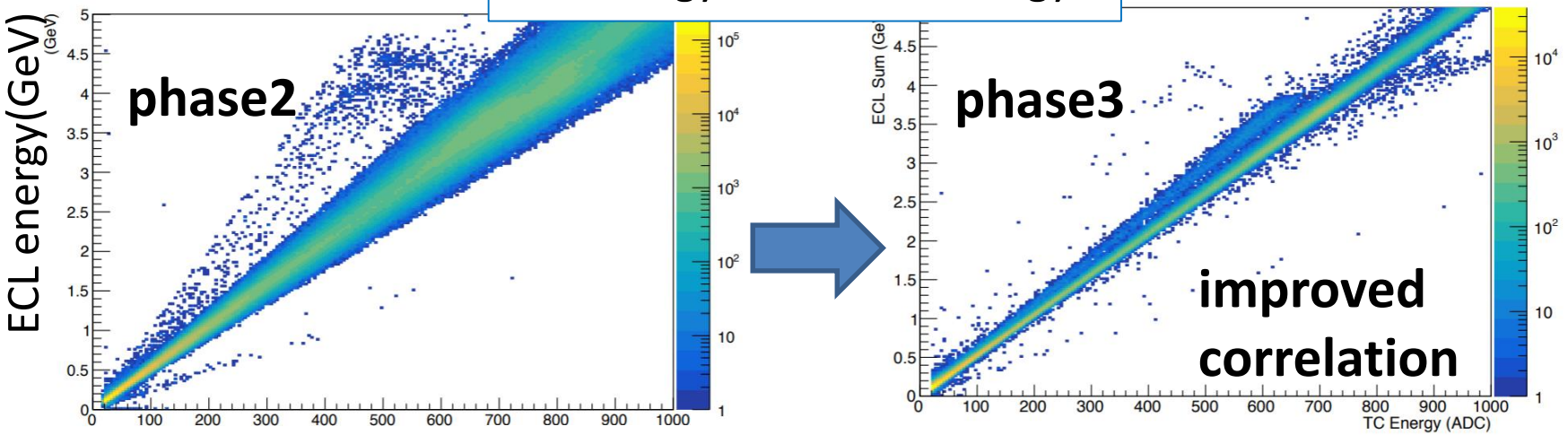
**-2019 Autumn:**

- -New bits: ecl burst, tighten low multi0
- -2D Bhabha is replaced to 3D Bhabha

Timing resolution with hadron skim




ECL energy vs TRGECL energy



# Status of CDC TSF, 2D tracker

**-2019 Spring**

-Improved efficiency by firmware bug fix and fix of dead channel

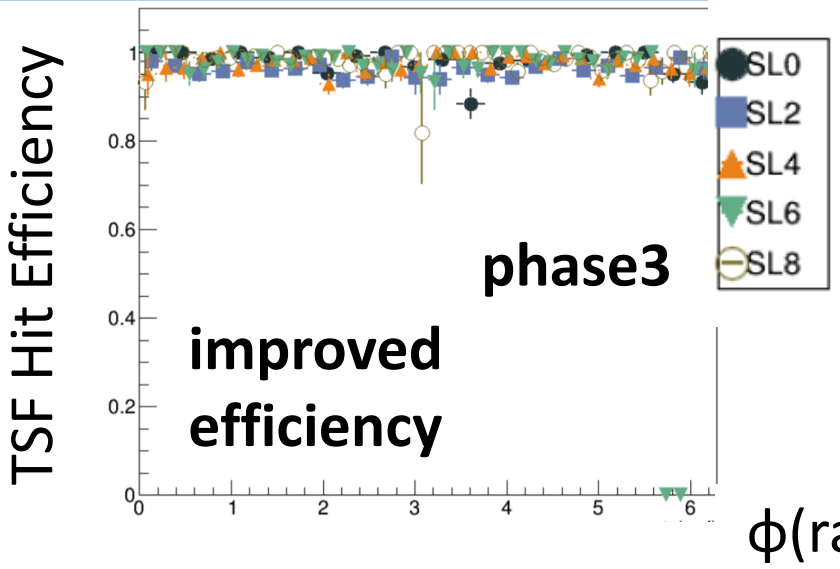
-CDC threshold is increased 50mV to reduce noise and L1 rate

**-2019 Autumn**

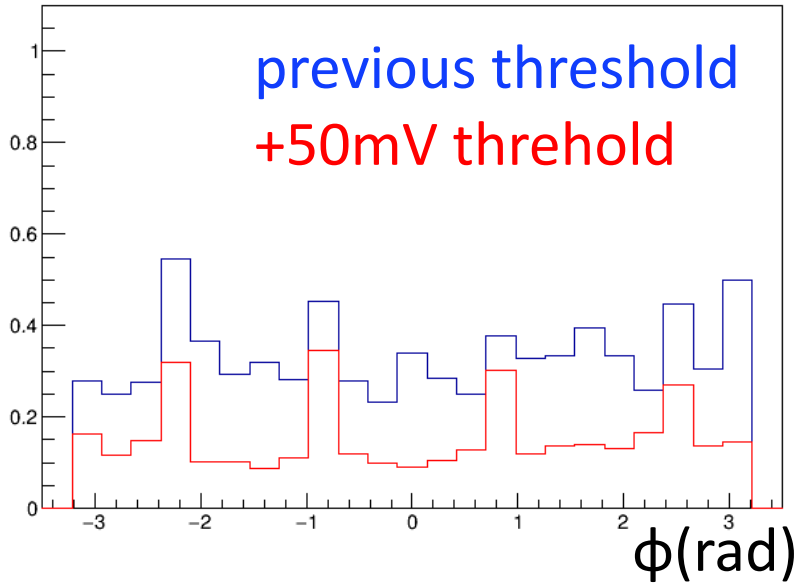
-Apply ADC cut on CDCFE -> postponed due to latency issue
(need additional ~300ns, although only ~100ns is allocated)

-Maximum number of TS per clock is increased from 10 to 15

TSF hit efficiency compared with CDC hit




2D trigger track overcounting rate





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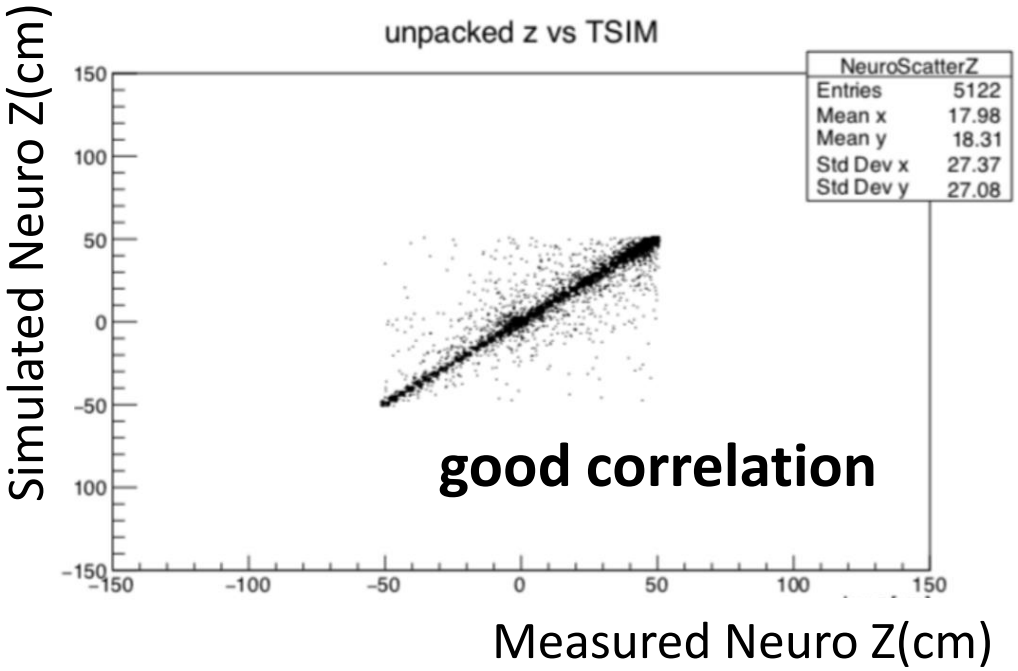
# Status of CDC 3D tracker

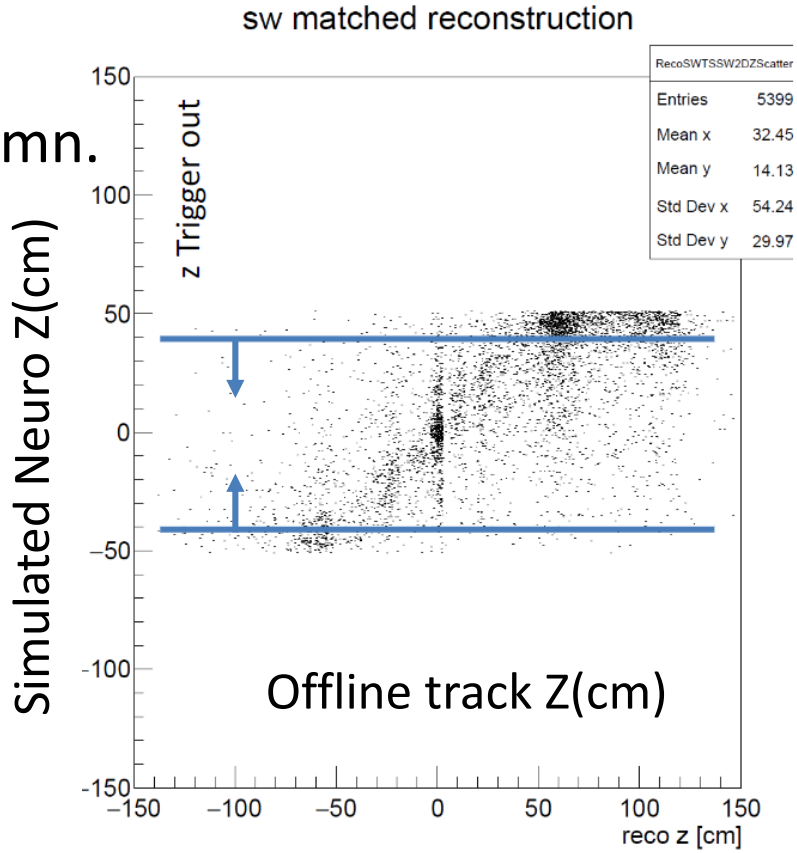
**-3DNeuro**

-Performance evaluation has been continued from 2019 Spring.
  -study difference btw. firmware and simulation. efficiency.
  -more study is needed.
-Should be ready by Autumn. Schedule is discussed in this workshop.
-We expect CDC trigger rate is reduced to ~ 1/5, by requiring z<40cm.

**-3D tracking**

-debugging is delayed. not ready by Autumn.



# Status of CDCtiming

**-2019 Autumn**

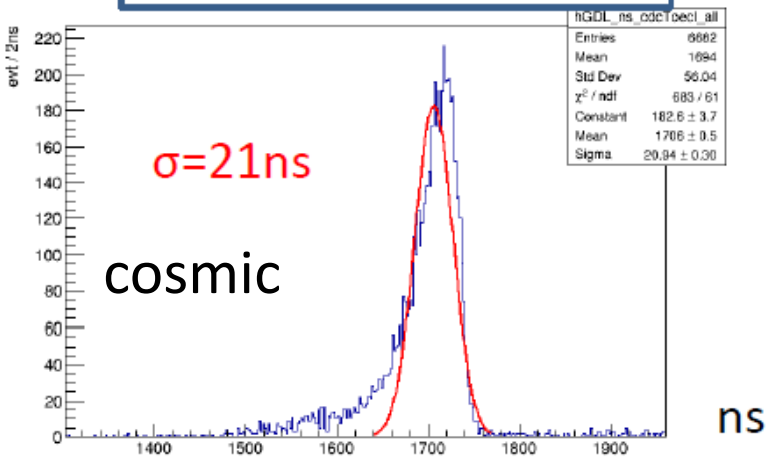
-Newly provide CDCtiming from 2D module.

-fastest priority timing among 2D tracked TSF

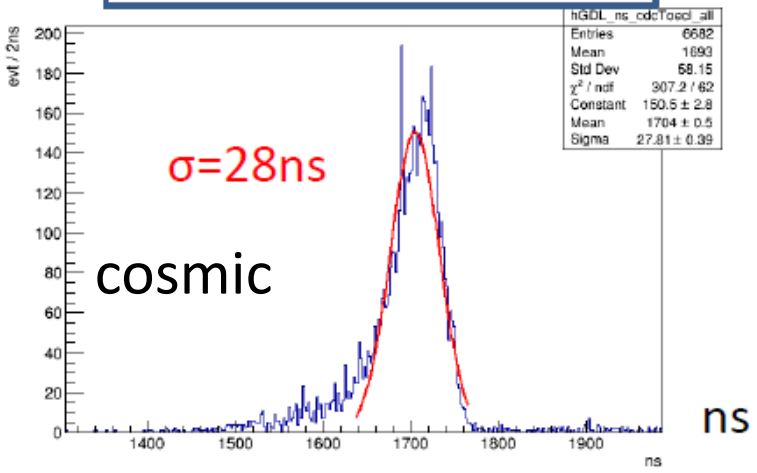
-Data will be taken with ECL and CDC timing

-L1 rate can be significantly increased. Will be used with 3D or improved track counting.

EventT0-CDCtiming




ECLtiming-CDCtiming



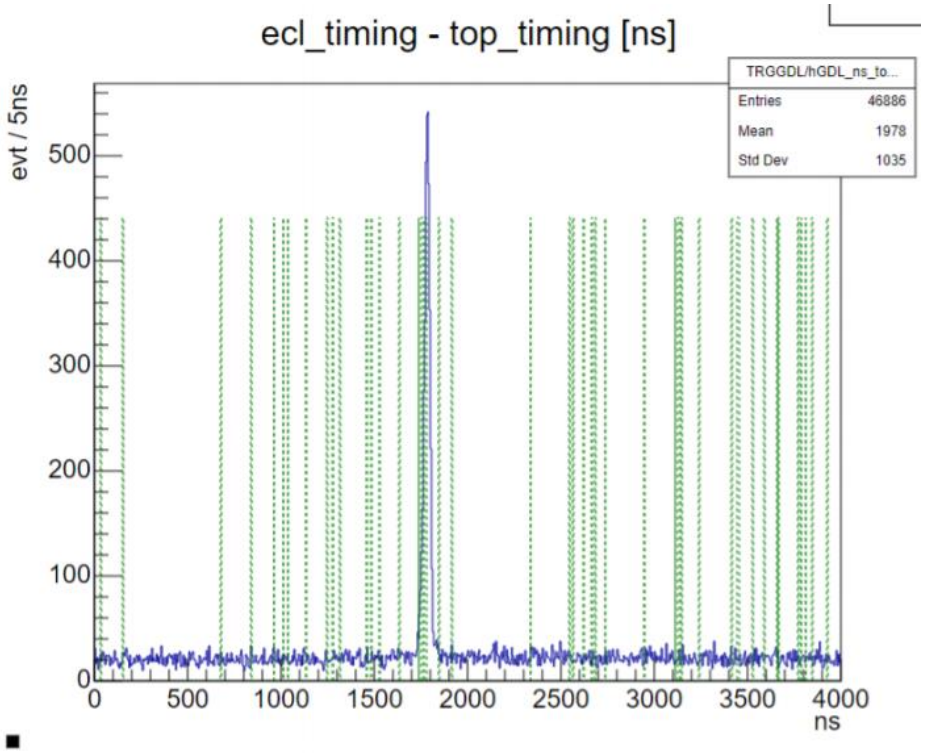

**-2020**

-Provide CDCtiming with fastest timing. Expected resolution is a few ns.

# Status of TOP trigger

-Problem of low efficiency and timing resolution with collision data
  -Parameters are adjusted during 2019 Spring
  -Reason is not clear due to limited information: no B2L readout

-B2L readout of TOP trigger was implemented in the end of June.
  -Unpacker is being developed
  -Analysis is not done yet.

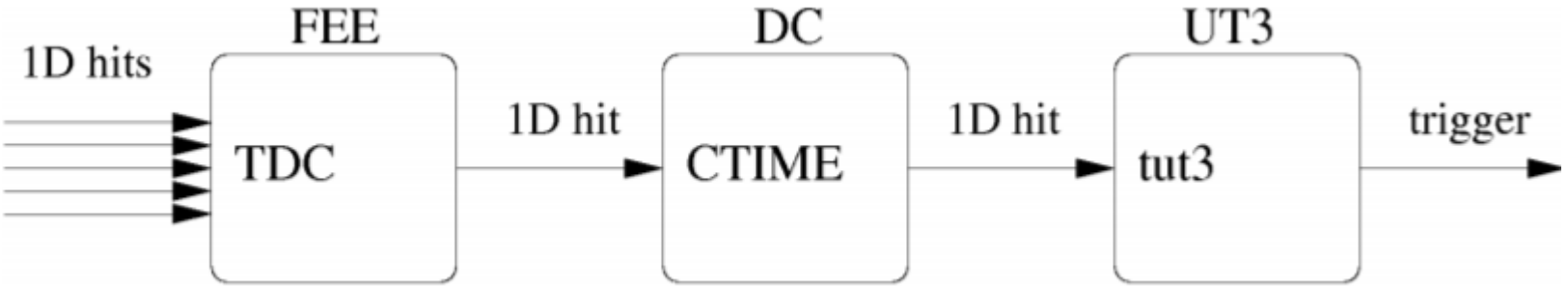



σ~15ns
low efficiency

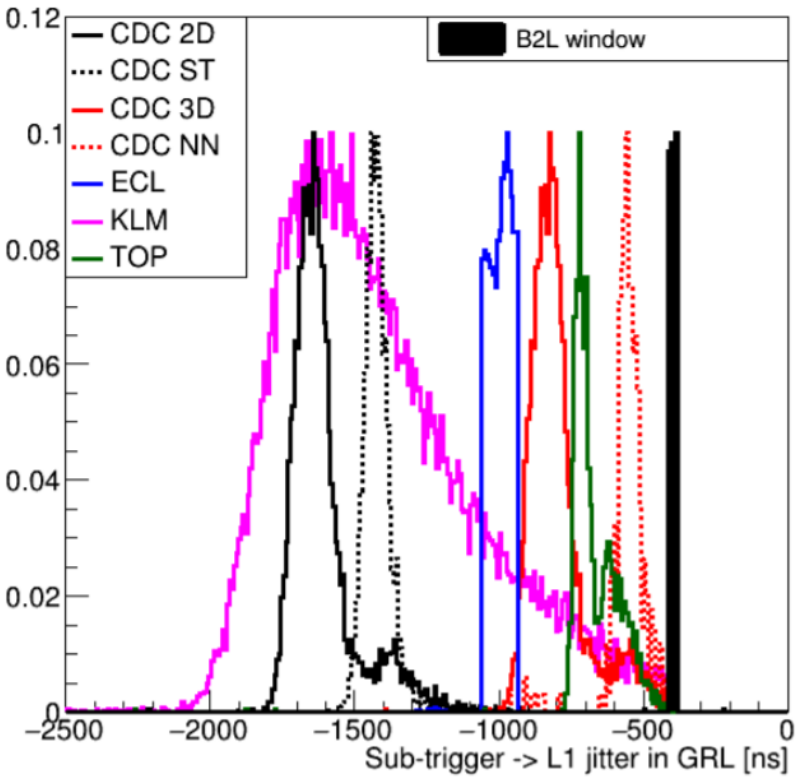
ns

# Status of KLM trigger

KLM trigger path




Input signal timing in GRL




-Not working due to large jitter
  -Originated from serial data transfer.
   DC take ~40ns/hit.

-Plan to delay signal to GRL to fix jitter
  -~2μsec latency is increased
  -No update since June.
   Need discussion in this workshop.

# Status of GRL

**-2019 Spring**

- -New logics:
  - -cdc-ecl matching
  - -cdc-ecl back to back
  - -short tracking with axial layer
- -Latency reduction: LVDS is used instead of optical to send data to GDL

**-2019 Autumn**

- -New logics:
  - -Improved 2D track counting to merge tracks with small $\Delta\phi$, $\Delta$pt
  - -Short tracking with axial+stereo layer
  - -endcap-barrel cdcd-ecl back to back

# Status of GDL

**-2019 Spring**

- -Injection veto is added
- -Stable firmware: file is provided with mcs, many bug fix/modification

**-2019 Autumn (plan)**

- -New bit: delayed Bhabha (bug fixed)
- -GDL<->ETM connection with GTH to solve ECL signal lost error
- -Fine time tuning for CDC timing
- -VME access logic is improved to solve VME read/write error

# Summary

| item | 2019 april | 2019 autumn |
|---|---|---|
| Main trigger | CDC2D + ECL cluster | CDC2D + CDC3D + ECL cluster |
| New trigger bits | ECL low energy multi clusters<br>ECL μ pair<br>CDC-ECL matching | ECL burst<br>Delayed Bhabha<br>Improved 2D track counting |
| Timing source | ECL | ECL + CDC |
| Bhabha prescale | 1 with 2D bhabha | <=1 with 3D bhabha |
| L1 trigger rate | 2~4kHz | <10kHz of DAQ limit |
| Hadron efficiency | >99% | >99% |