TRG DAQ, SLC and monitoring

T. Koga
TRG readout

- GDL, GRL and CDCTRG are in TRG readout
- 22 UT3 boards
- CDCTRG: only 1/x events are recorded (event suppression)
  2019 Spring, x=256
- In total, ~20MB/sec @ 5kHz

<table>
<thead>
<tr>
<th>UT3</th>
<th>copper</th>
<th>#bit</th>
<th>clk window</th>
<th>byte/event/UT3</th>
</tr>
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<tbody>
<tr>
<td>2D0,1,2,3</td>
<td>11001,2</td>
<td>4096</td>
<td>48</td>
<td>24588/x</td>
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<tr>
<td>3D0,1,2,3</td>
<td>11003,4</td>
<td>2048</td>
<td>48</td>
<td>12300/x</td>
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<tr>
<td>NN0,1,2,3</td>
<td>11005,6</td>
<td>2048</td>
<td>48</td>
<td>12300/x</td>
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<tr>
<td>TSF0,4</td>
<td>11007</td>
<td>2048</td>
<td>48</td>
<td>12300/x</td>
</tr>
<tr>
<td>TSF1,2,3,5,6</td>
<td>11008,9,10</td>
<td>4096</td>
<td>48</td>
<td>24588/x</td>
</tr>
<tr>
<td>GDL</td>
<td>15001</td>
<td>640</td>
<td>32</td>
<td>2584</td>
</tr>
<tr>
<td>GRL</td>
<td>15002</td>
<td>1024</td>
<td>1</td>
<td>128</td>
</tr>
</tbody>
</table>

-ECL(TOP)TRG is in ECL(TOP) readout
TRG B2L problem in phase3

-Bug of event suppression logic for CDCTRG
- Taken CDCTRG data has problems: event slip etc.
- Fixed the bug in the last month. No problem in local test.
- All CDC modules will be re-compile with new TRG B2L library.

-B2L error of ETF
- ETF data reach HSLB later than others. Reason is unknown.
- June 2019, ETF is masked. Keep to mask in Autumn.

-Bit shift of B2L data from GDL
- Taken GDL data sometimes (<~0.3%) has bit shift problem
- Fixed the bug in the last month (common bug as CDCTRG).
TRG problem stopping DAQ for long time in phase3

-May 2019: VME parameter error
  -Wrong parameter is set to GDL through VME
  -Stop DAQ ~1day
  -Temporary solved by checking parameter automatically (if wrong parameter is set, TRG status cause error.)
  -Reason is still unknown.
    In GDL firmware, way to access VME is being modified.

-May 2019: LVDS connection error btw. GDL and GRL
  -Signal through LVDS is sometimes broken
  -Stop DAQ ~12hours
  -Solved by widen clock length of the signal
TRG problem stopping DAQ short time (but many times)

-1. BUSY from GDL
   -Recovered by SALS.
   -Reason is unknown. Maybe back pressure, or Maybe TRG.
   -High rate test is needed for further investigation

-2. ttlost
   -Recovered by SALS.
   -Reason is unknown. No investigation is done so far.

-3. One of NSM node (TRGREASY) stuck in NOTREADY
   -Lost communication to other nodes and cause error
   -Fixed by allocating non-continuous communication error in June 2019
TRG problem stopping DAQ short time (but many times)

-4. CDCTRG dataflow is down due to CDCFE or merger
   - Reason is unknown. Recovered by masking problematic CDCFE/merger.
   - Automatic masking script is prepared for TRG expert
     (but still need help of TRG expert. not recovered by SALS.)

-5. GDL lost signal from ETM.
   - Reason is unknown. Recovered by rebooting GDL.
     (Need help of TRG expert. not recovered by SALS.)
   - We replaced GDL<->ETM connection from GTX to GTH
     in the last month. Stability test will be done.
GDL full readout plan in Autumn run

-GDL readout data is time integrated at present. 4bit(127MHz) -> 1bit(32MHz) to reduce data size.

-Full readout will be added in debug mode in Autumn run
  -4 B2L lines from one UT3 board
  -4 more HSLB (cpr15003ab,4ab), 2 or more ropc, and
  -4 more FTSW are needed
  -firmware is being tested
  -apply scale factor to reduce datasize
Status of TRG slow control : GUI

-Many GUIs are newly added in 2019 Spring:
  local run control, TRG status, GDL control, TRGECL status

-Plan:
  -Basic GUI panels are all prepared. No big change.
  -Configure GDL based on run type set in global run panel
  -Add reboot button to initialize TRG module and SLC (?)
Status of TRG slow control: NSM

- NSM is prepared for each trigger module to record/control parameters with VME

- Followings are still missed: NSM for CDCNN, TOP
Status of TRG slow control: NSM

-A NSM node, TRGREADY, is prepared to see TRG status. Cause TRG error if CDCTRG/ECLTRG/GDL have problem. Followings are checked:
  -CDCTRG dataflow, ECLTRG parameter, GDL configuration

-Plan:
  -Error sound is not working properly
  -Add TOP and KLM once they are ready
  -Prepare reset/recover button (？)
Status of TRG slow control : archiver

- Archiver is added for TSF, GDL, GRL, ECL to record trigger rate

- Plan: followings are still missed
  - output hit/track rate monitoring for CDC2D, 3D, KLM, TOP

Example of archived L1 rate
Status of TRG DQM

- Following DQMs are added to monitor TRG output:
  - 2019 spring: GDL, CDCTSF, 3D (TRGECL had been existed)
  - 2019 autumn: NN, GRL
  - Still missed: CDC2D, TOP

- Plan
  - More simpler DQM plots for CR shifter
  - Automatic error caution
  - Add missed plots

Example of DQM (PSN bits)
Status of TRG QAM

-QAM (rundependency) is being prepared following ARICH local QAM
-Trigger efficiency, trigger rate, hadron/Bhabha quite useful for online monitoring of TRG performance

-High purity skims (HadronB and Dimuon) are needed on HLT
-HLT group (Karim) is working to add them

Example of QAM (eff.)
Summary

- Status of TRG DAQ, SLC and monitoring are presented

- DAQ
  - status of each TRG DAQ error and measures
  - new GDL readout will be added for Autumn run

- SLC
  - GUI: required panels are added.
  - NSM: NN and TOP are missed. TRGREADY is added.
  - Archiver: GDL, GRL, TSF, ECL are archived. Others should be implemented.

- Monitoring
  - DQM is added and used for online monitoring
  - QAM will be added for Autumn run
Backup
Status of trigger system in phase 3

- **2019 spring**: CDC2D, ECL, GRL, GDL
- **2019 Autumn**: CDC3D Neuro, CDC timing on 2D
- **Under development**: CDC3D tracker, TOP, KLM
L1 rate and efficiency in 2019 Spring

- L1 rate: 2~4kHz, depends on beamBG
- HadronB efficiency: >~99%
- Dimuon efficiency: ~95%
- Tau efficiency: ~

2D efficiency with Dimuon skim

- #2D track >=1
- #2D track >=2
- #2D track >=3

Trigger efficiency for HadronB

- ECL cluster (c4|hie)
- two 2D track with opening angle (ffo)
- three 2D tracks (fff)

exp8 #Run
Status of ECL trigger

- **2019 Spring**: working stably
  - Improved calibration
  - Improved timing resolution
  - New bits: low multi cluster, μ pair, pur bhabha

- **2019 Autumn**:  
  - New bits: ecl burst, tighten low multi0  
  - 2D Bhabha is replaced to 3D Bhabha

Timing resolution with hadron skim

~7 ns resolution

ECL energy vs TRGECL energy

Improved correlation
Status of CDC TSF, 2D tracker

- **2019 Spring**
  - Improved efficiency by firmware bug fix and fix of dead channel
  - CDC threshold is increased 50mV to reduce noise and L1 rate

- **2019 Autumn**
  - Apply ADC cut on CDCFE  -> postponed due to latency issue
    (need additional ~300ns, although only ~100ns is allocated)
  - Maximum number of TS per clock is increased from 10 to 15

**TSF hit efficiency compared with CDC hit**

**2D trigger track overcounting rate**

*previous threshold +50mV threshold*

*improved efficiency*
Status of CDC 3D tracker

- 3DNeuro
  - Performance evaluation has been continued from 2019 Spring.
  - study difference btw. firmware and simulation, efficiency.
  - more study is needed.
  - Should be ready by Autumn. Schedule is discussed in this workshop.
  - We expect CDC trigger rate is reduced to $\sim 1/5$, by requiring $z < 40\text{cm}$.

- 3D tracking
  - debugging is delayed. not ready by Autumn.

![Simulated Neuro Z(cm) vs Measured Neuro Z(cm)](image1)

**good correlation**

![Offline track Z(cm)](image2)

- [Table: Simulated Neuro Z(cm)](table1)
- **2019 Autumn**
  - Newly provide CDC timing from 2D module.
  - Fastest priority timing among 2D tracked TSF.
  - Data will be taken with ECL and CDC timing.
  - L1 rate can be significantly increased. Will be used with 3D or improved track counting.

**EventTO-CDC timing**

\[ \sigma = 21 \text{ns} \]

**Cosmic**

- **2020**
  - Provide CDC timing with fastest timing. Expected resolution is a few ns.
Status of TOP trigger

- Problem of low efficiency and timing resolution with collision data
  - Parameters are adjusted during 2019 Spring
  - Reason is not clear due to limited information: no B2L readout

- B2L readout of TOP trigger was implemented in the end of June.
  - Unpacker is being developed
  - Analysis is not done yet.

\[ \sigma \approx 15 \text{ns} \]

low efficiency
Status of KLM trigger

- Not working due to large jitter
- Originated from serial data transfer. DC take ~40ns/hit.

- Plan to delay signal to GRL to fix jitter
  - ~2μsec latency is increased

- No update since June.
Need discussion in this workshop.
Status of GRL

-2019 Spring
- New logics:
  - cdc-ecl matching
  - cdc-ecl back to back
  - short tracking with axial layer
- Latency reduction: LVDS is used instead of optical to send data to GDL

-2019 Autumn
- New logics:
  - Improved 2D track counting to merge tracks with small $\Delta \phi$, $\Delta pt$
  - Short tracking with axial+stereo layer
  - endcap-barrel cdc-ecl back to back
Status of GDL

- **2019 Spring**
  - Injection veto is added
  - Stable firmware: file is provided with mcs, many bug fix/modification

- **2019 Autumn (plan)**
  - New bit: delayed Bhabha (bug fixed)
  - GDL<->ETM connection with GTH to solve ECL signal lost error
  - Fine time tuning for CDC timing
  - VME access logic is improved to solve VME read/write error
## Summary

<table>
<thead>
<tr>
<th>Item</th>
<th>2019 April</th>
<th>2019 Autumn</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Main trigger</strong></td>
<td>CDC2D + ECL cluster</td>
<td>CDC2D + CDC3D + ECL cluster</td>
</tr>
<tr>
<td><strong>New trigger bits</strong></td>
<td>ECL low energy multi clusters, ECL μ pair, CDC-ECL matching</td>
<td>ECL burst, Delayed Bhabha, Improved 2D track counting</td>
</tr>
<tr>
<td><strong>Timing source</strong></td>
<td>ECL</td>
<td>ECL + CDC</td>
</tr>
<tr>
<td><strong>Bhabha prescale</strong></td>
<td>1 with 2D bhabha</td>
<td>&lt;=1 with 3D bhabha</td>
</tr>
<tr>
<td><strong>L1 trigger rate</strong></td>
<td>2~4kHz</td>
<td>&lt;10kHz of DAQ limit</td>
</tr>
<tr>
<td><strong>Hadron efficiency</strong></td>
<td>&gt;99%</td>
<td>&gt;99%</td>
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