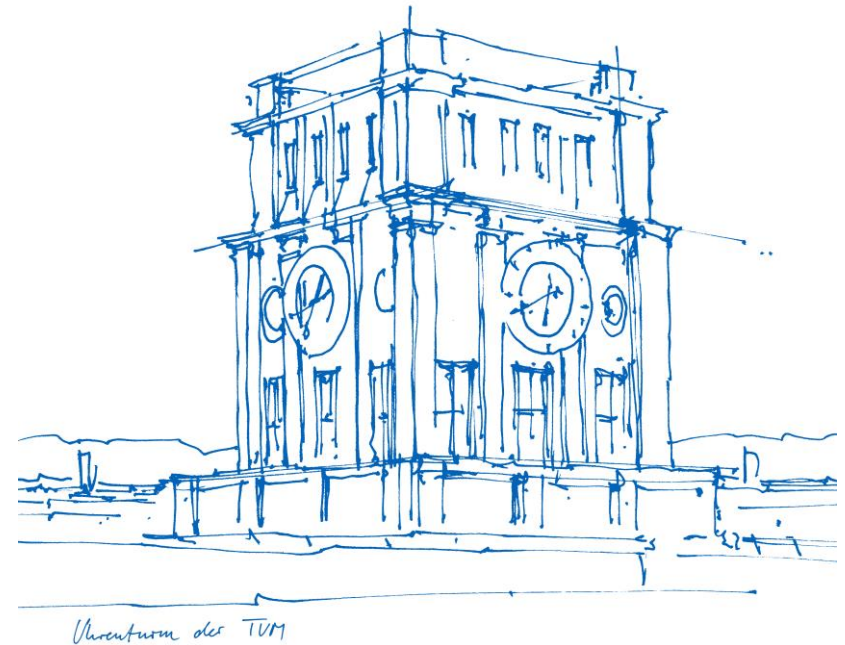# DHH Status

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Belle 2 DAQ Workshop

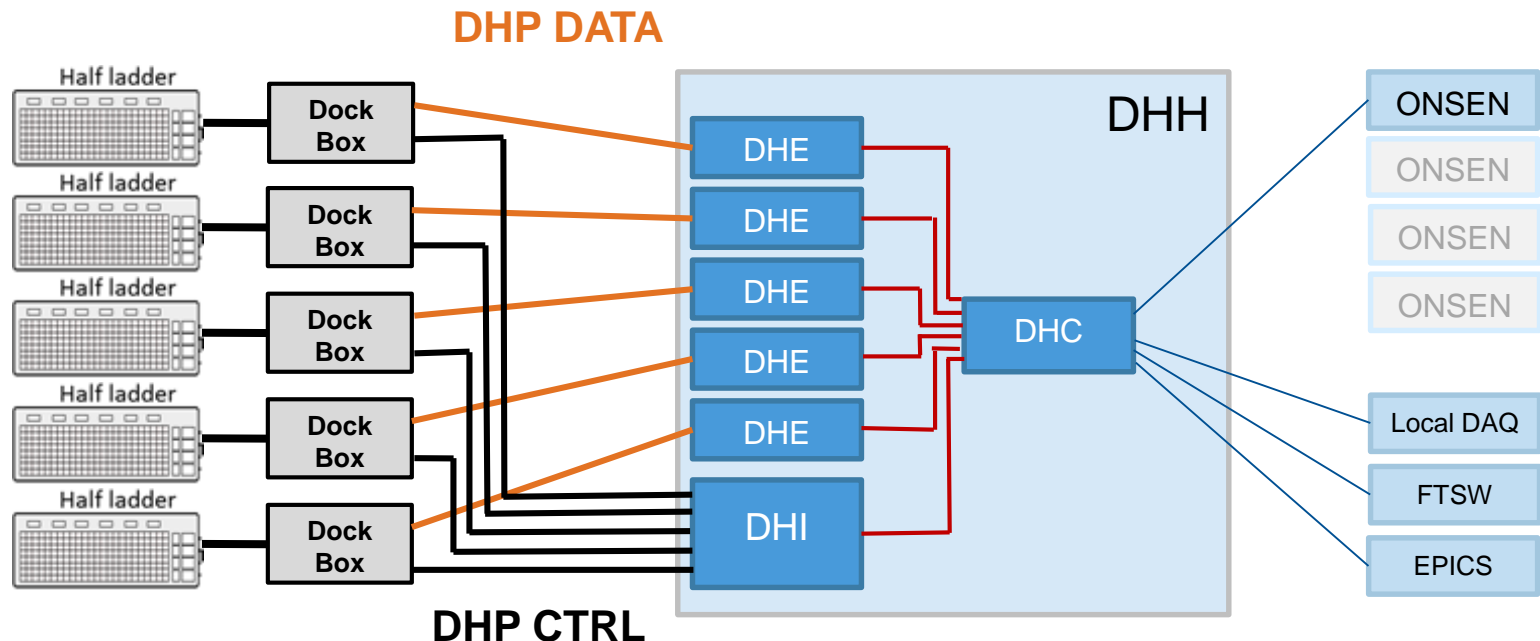Seoul August 26-29, 2019

Overview

- DHC firmware in phase 3
- Gated mode
- DHE firmware in phase 3
- Observed problems and fixes
- Load balancing DHC firmware
- Test results
- Cross-point switch
- Summary

DHH Setup at Phase 3

Phase 3 PXD setup :

- 8x inner layer ladders + 2x outer layer ladders
- 4x DHH systems

- 4x ONSEN (25% of bandwidth)
- No GATED mode

DHH

Phase 3 DHC Firmware

- Single ONSEN link
- UDP data throttling for Local DAQ
  - DHC data rate > 1Gbps
  - UDP Data throttled by programmable parameters either by number of events per second or amount of data per second
- Synchronization of all DHC in local run mode(without common start of run signal) using FTSW revo9 signal
- Backpressure to DHE, needed for final DHC firmware with 4 ONSENs
- Diagnostics of FTSW's link loss
- GATED mode implementation
- Configurable DHE readout order

For ROI selection, ONSEN requires data to be organized in the same order as HLT ROIs i.e. incremental IDs. Due to cable layout the detectors can't be connected to DHH in required order.
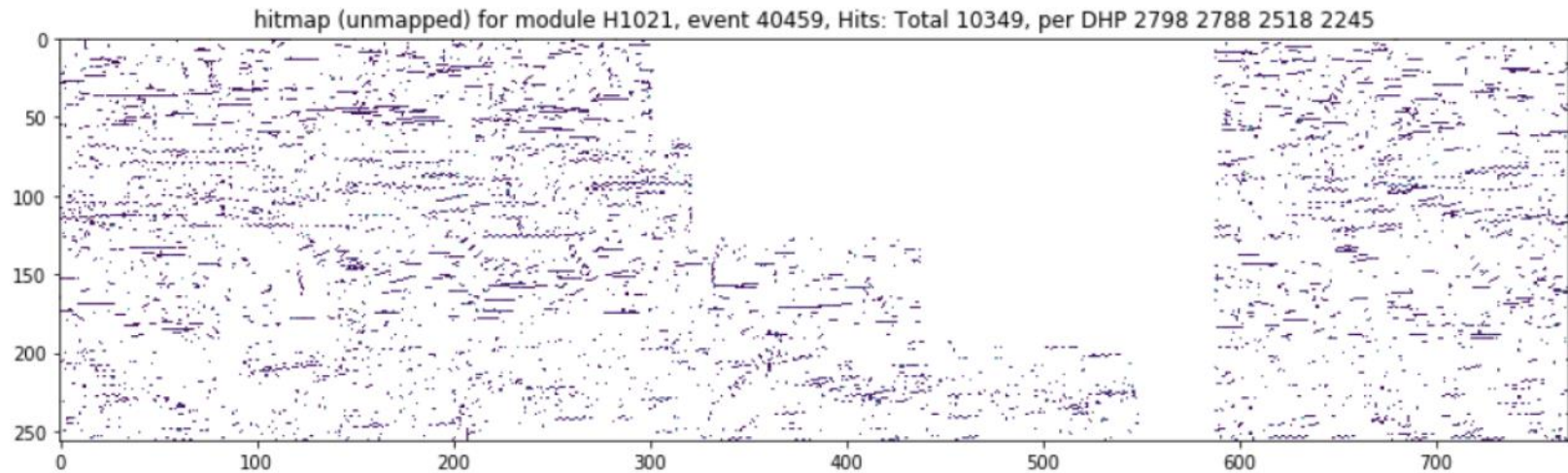
Gated Mode

- DHC/DHI firmware versions support Gated Mode
- Extensive tests and optimization of Gated Mode were performed at DESY
- DESY setup was not identical to KEK because FTSW module was programmed with version 2 while at KEK version 3 was used
- During tests at KEK the Noise after gated mode was much too high therefore we didn't manage to complete the test during the run
- Further optimization of Gated Mode operation is being done at DESY now
- Test at KEK will follow
- DHC firmware problem : the delay relative to the KICK signal could not be tuned => fixed shortly after
- FTSW always indicated injection as HER => no individual tuning of parameters possible
        => Fixed by Nakao last week, it was verified at DESY
- Gated mode will be tested in September at KEK.

DHE Firmware at Phase 3
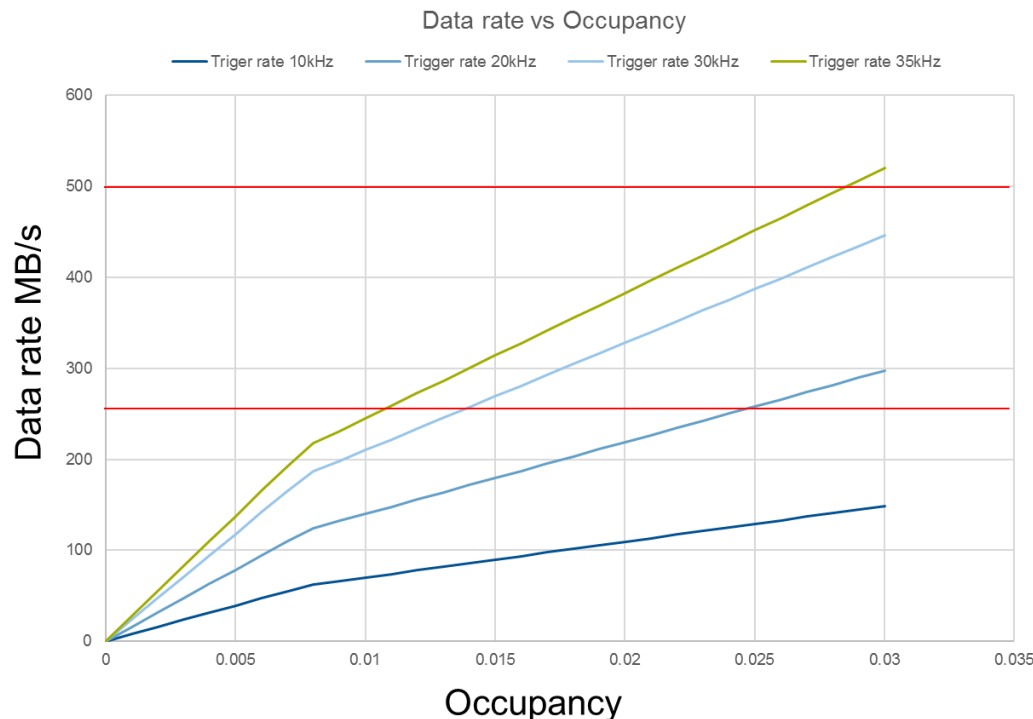
DHE Firmware at Phase 3

Full feature version 30kHz capable deployed on May 12

- Data truncation when DHP frame size exceeds 2000 words or more than 3.3% occupancy
  - ✓ 1616 pixels/DHP frame => not less than 3.3% occupancy

hitmap (unmapped) for module H1021, event 40459, Hits: Total 10349, per DHP 2798 2788 2518 2245

DHE Firmware at Phase 3

- High trigger rate capable => Trigger throttling
  - ✓ trigger rate is limited by bandwidth of DHE=>DHC or DHC=>ONSEN data links
  - ✓ DHE firmware limits : @10kHz no limit, @20kHz 2.5% occupancy, @30kHz 1.4% occupancy
  - ✓ Current PXD averaged occupancy below 0.1%

Data rate vs Occupancy

Trigger rate 10kHz — Trigger rate 20kHz — Trigger rate 30kHz — Trigger rate 35kHz

Possible link speed improvement
DHE=>DHC link 500 MB/s

Current limit
DHE=>DHC link 250 MB/s

DHE Firmware at Phase 3

- Possibility to issue "short reset" during run to recover DHP links

- Extended built-in diagnostics (DHE and DHC)
  - Check of received and processed triggers
  - Multiple test points of data consistency check, CRC errors => PVs
  - Private storage of PV trending
  - Problem of diagnostics of crashed runs because ABORT signal stops FTSW and resets PVs in the same time.
    - Would it be possible to ABORT run in two steps : 1. stop triggers 2. issue ABORT?

- Tests performed at TUM lab and DESY
  - ✓ Minimum time interval between triggers 100 ns
  - ✓ Trigger rate test up to 1 MHz, Trigger throttling reduces effective trigger rate to expected value according to amount of data.
  - ✓ Long term tests

PXD Issues

- Occupancy drop caused by few consecutive very high occupancy events
    - Run continuous
    - Amount of errors were significantly reduced by veto triggers during and shortly after injection
    - Origin of problem is not yet understood
        - ✓ DHP stop sending data at very high data rate
        - ✓ DHE and DHP are out of sync
        - ✓ Problem can be fixed by issuing DHP reset and resynchronizing DHPs with DHE
    - GATED mode will further reduce occupancy drop probability
- HLT trigger ahead of DHH trigger => Abort of RUN
    - Corrupted data in DHE or DHC
    - Origin of problem is not identified
    - Built-in diagnostic is not available because ABORT signal resets PVs
    - Further study is needed
- One DHPT link was lost due problem with optical link
- Otherwise table data taking

Stopped runs by PXD

Runs 1020-1335, 21.05-27.05
PXD Run Summary Elog

| Error Type	# of stopped runs	# Phy. runs	Comment
H1051 data drop	**19**		2 times/shift
Other modules data drop	8		
Others DHH errors	1		UCF link
DHP link(s) drop	3		No stop of run
HLT Ahead of DHH	7		
Total	35	174	

H1051 data drop error synchronous with CLOCK SYNC ERROR in DHI50
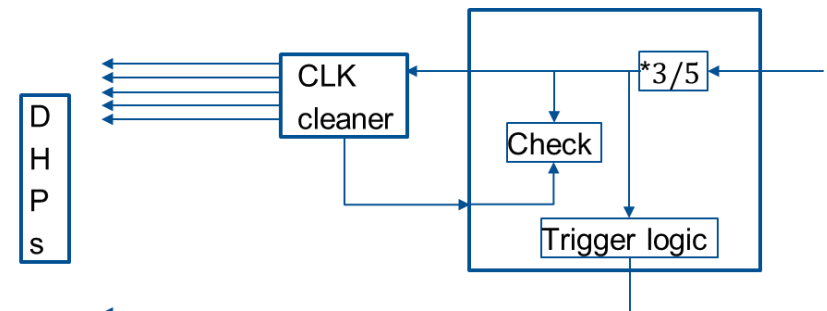Error was caused by a glitch on Clock line

DHI clock issue

- Glitch on clock line originated in CLK Cleaner IC

- Instabilities first observed during testing the gated mode
  - Implemented PVs to monitor expected and real REVO phase
    - Check if counters with different clocks run synchronously

Previous Scheme
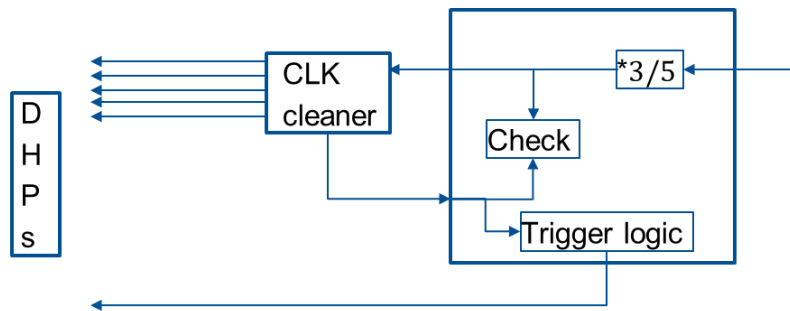
Current Scheme

Preparation for Phase 3.2

To Do List for Next Run

- Resolving problem with light yield of DHP Optical links

- Test of load balancing DHC firmware
  - ✓ Load balancing firmware can't support programmable DHE readout order needed for ROI

- Installation of Cross-point switch to provide correct data order for ONSEN ROI selection

DHPT Optical Links' Yield

22									
23	module / fiber cable	1041 - F12-A DB4				1042 - F12-D DB5			
24	fibers (mpo)	4 (2)	9 (7)	7 (5)	2 (0)	8 (6)	5 (3)	3 (1)	6 (4)
25	intensities before phase3	0.35	0.34	0.33	0.34	0.37	0.38	0.34	0.35
26	intensities 8.07.2019 (Summer shutdown)	0.39	0.144	0.33	0.158	0.34	0	0.34	0.35
27	Difference before PH3 - summer shutdown 2019	-0.04	0.196	0	0.182	0.03	0.38	0	0

47	module / fiber cable	1081 - 8A DB2				1082 - F8-5 DB7			
48	fibers (mpo)	4 (2)	3 (1)	5 (3)	2 (0)	4 (2)	3 (1)	5 (3)	2 (0)
49	intensities before phase3	0.35	0.35	0.35	0.35	0.33	0.36	0.34	0.47
50	intensities 8.07.2019 (Summer shutdown)	0.36	0.35	0.38	0.27	0.0668	0.36	0.35	0.35
51	Difference before PH3 - summer shutdown 2019	-0.01	0	-0.03	0.08	0.2632	0	-0.01	0.12
52									

# Result of Investigation

- Dead link was caused by broken transmitter
  - ✓ Dock box PCB was exchanged
  - ✓ Broken transmitter will be sent to Glenair for diagnostics
  - ✓ Transmitter shall sustain radiation dose above 250 kRad
  - ✓ No information about actual radiation dose yet
- Other links with reduced light yield were recovered by pushing optical connector
  - ✓ We assume it was a single failure unrelated to radiation
  - ✓ Clamps were installed to prevent lose connectors

Clamps to Fix Optical Connectors - Done
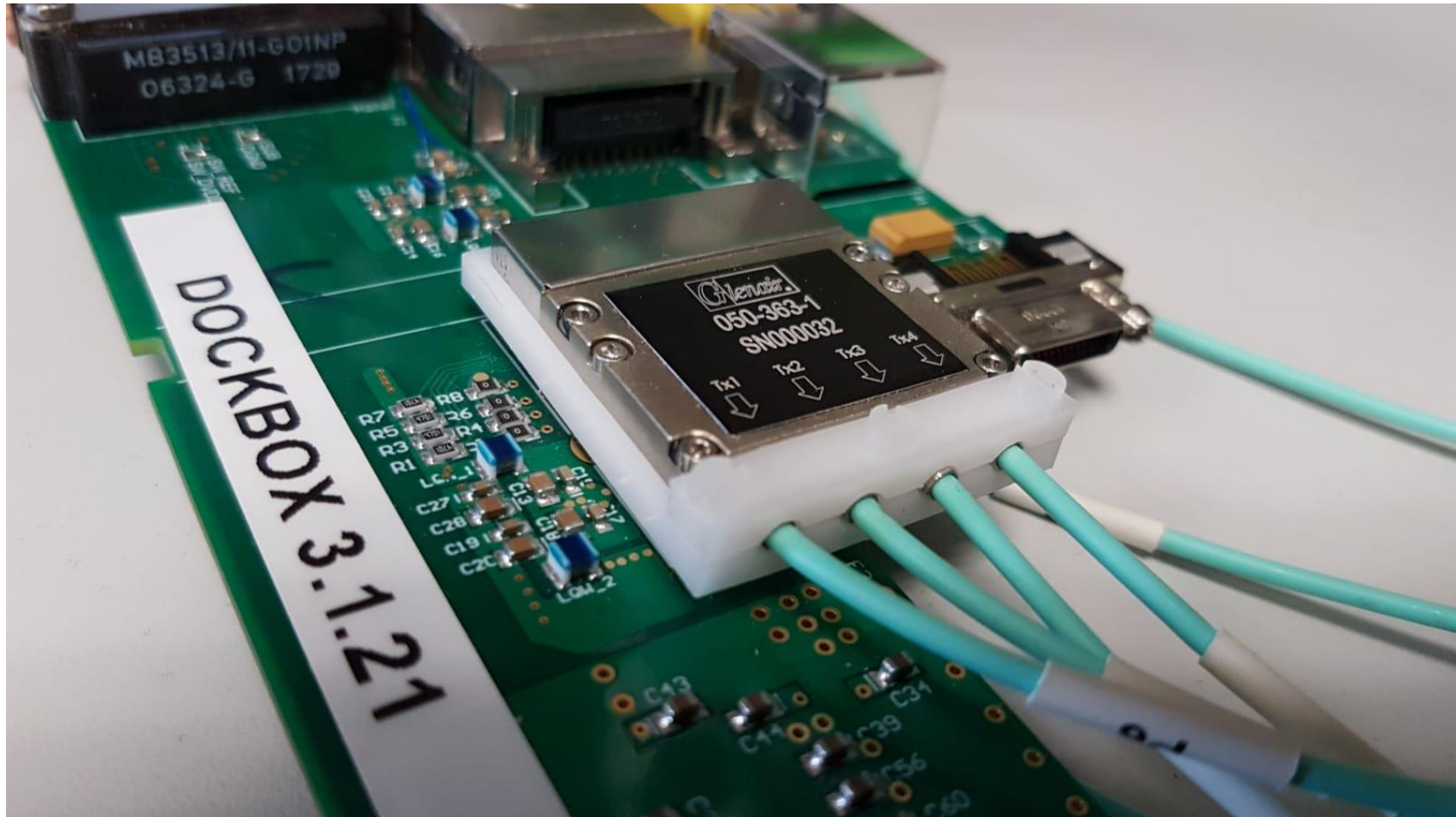
DHH Setup at Phase 3.2

DHH
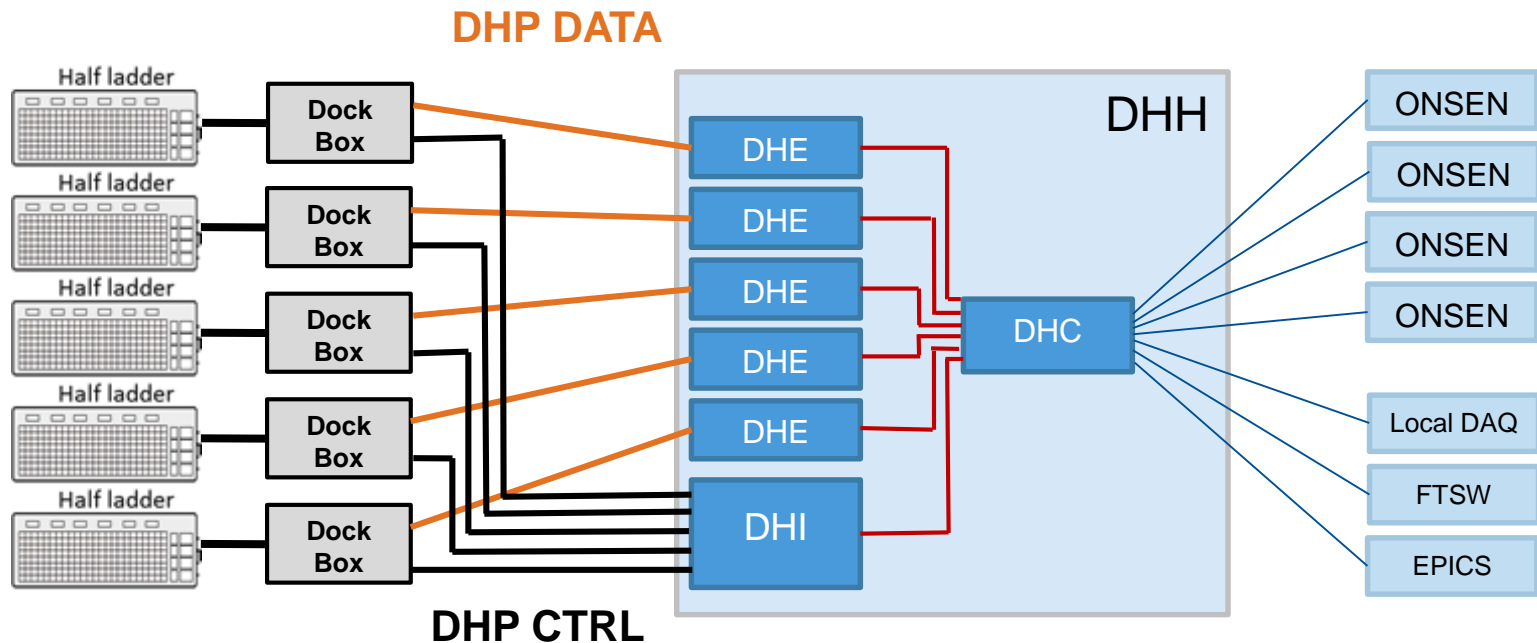
- 30 kHz capable DHH-ONSEN configuration
- Load balancing DHC firmware distributes data between 4 ONSEN modules
- 16 ONSEN modules are deployed

# Load balancing DHC Firmware
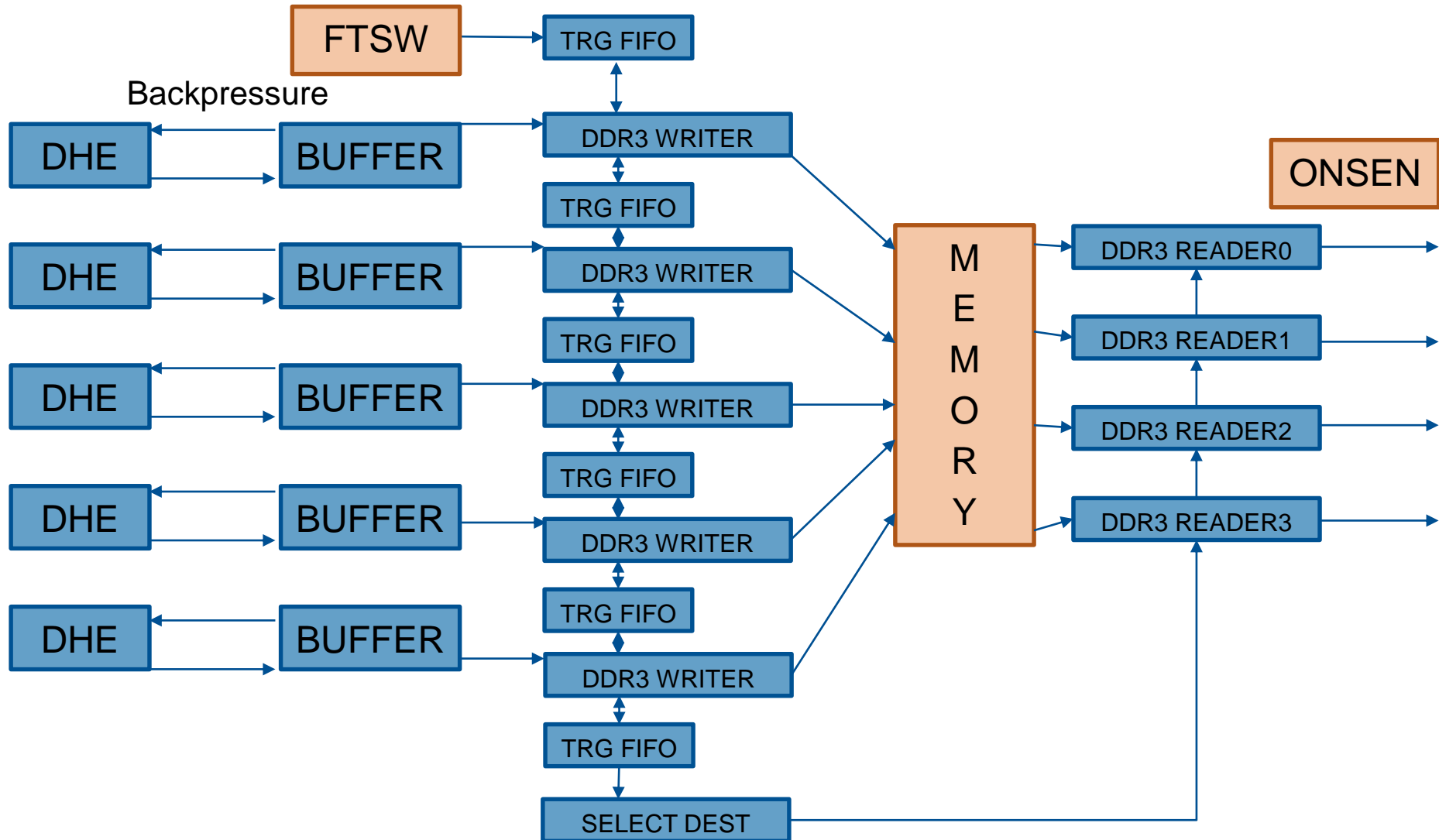
Load balancing Firmware

- Installed and tested in July at KEK

- High trigger/data rate tests

- During long term high data rate tests 3 DHE modules (always the same) produced corrupted data and crashed run. Such behavior could be provoked by cross-talk or hardware failure problem.

- Addition diagnostic was implemented in DHE and DHC

- More tests will be done this week

- Data order for ROI
  - Due to asymmetrical data processing between ports programmable change of DHE readout order is not possible within the firmware
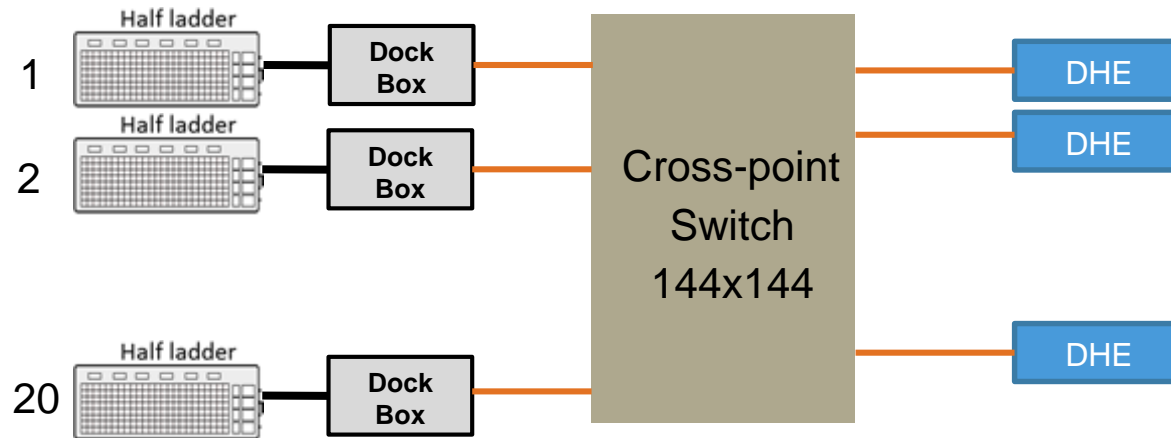 - We are installing cross-point switch to solve this problem

Cross-point switch

Cross-Point Switch

- IC VSC3144
- 144x144 non blocking cross-point switch
- 45x45 mm2
- Up to 6.5 Gbps/port, 1072 BGAwww
- Analogue circuits, no restriction on phase, frequencies, signal pattern
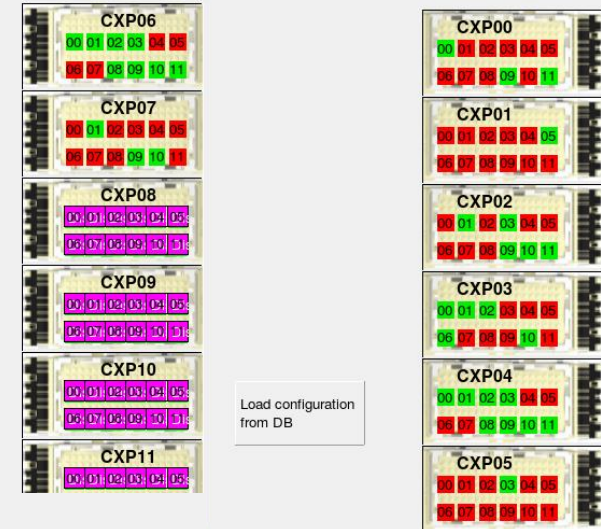- Programmed on port-by-port basis
- Configuration programmed via IPBUS
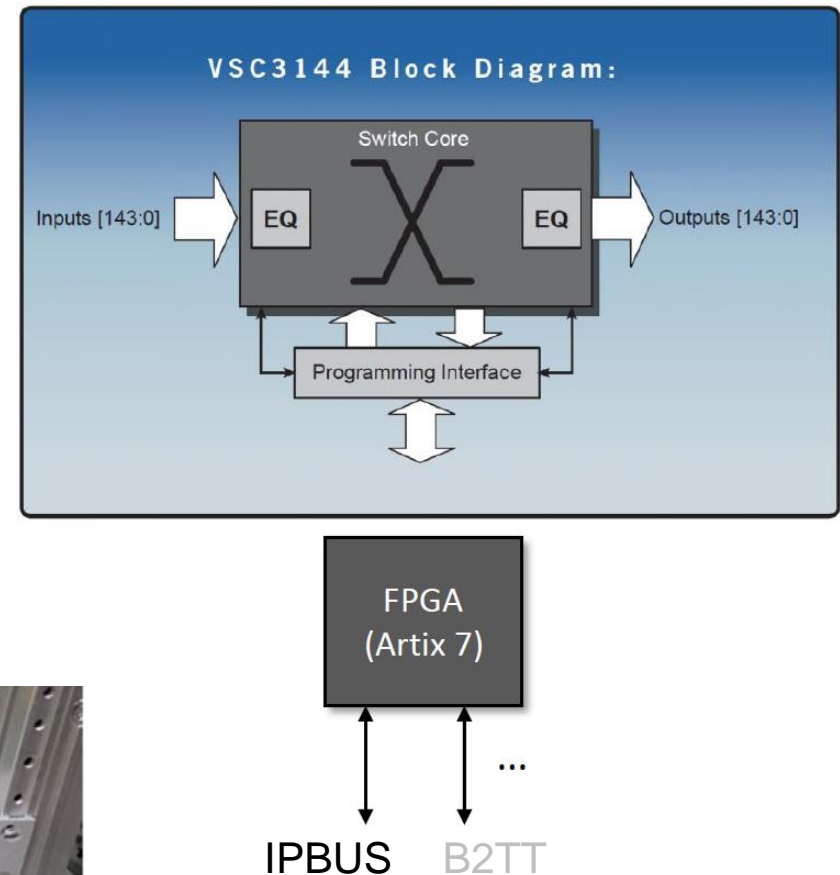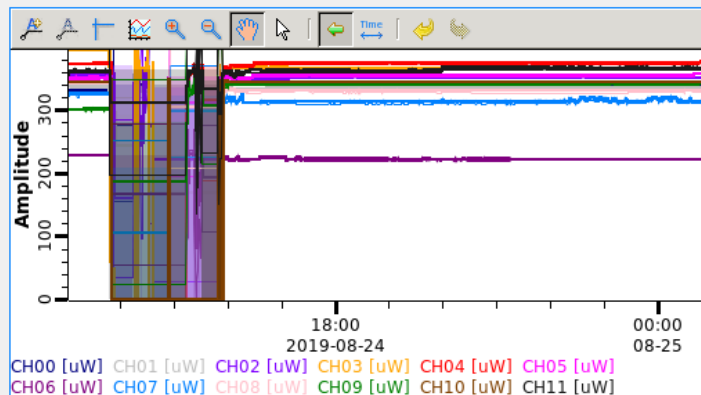
Cross-Point Switch

Cross-point Switch Software

- Cross-point switch fully integrated in EPICS
- Configuration stored in DB
- Optical receivers provide additional information
  - ✓ Light ON
  - ✓ Signal presence
  - ✓ Light power

Summary

- Full power DHE firmware was deployed and showed stable operation
- Few problems during data taking observed, fix is in progress
- Corrupted data problem still to be understood, more tests foreseen in September
- DHE/DHC final firmware versions were installed and successfully tested
- PXD can be read out at 20kHz with 2.5% occupancy and 30kHz with 1.4% occupancy
- Cross-point switch installed, it allows to organize data in a right order for ROI selection

THANK YOU