Status of FELIX Belle II DAQ Upgrade Option

Vladimir Savinov (University of Pittsburgh) on behalf of KEK & Pitt

Figure 2: Left: TTD mezzanine for Belle II timing interface. Right: BNL-712 FELIX I/O card with timing mezzanine mounted on the top left corner.
The Original Proposal from BNL

Belle II DAQ upgrade

D. Asner\textsuperscript{1}, H. Chen\textsuperscript{2}, D. Jaffe\textsuperscript{3}, B. Pal\textsuperscript{4}  

\textit{Brookhaven National Laboratory, Upton, NY-11973, USA}

June 11, 2018  
Version-1.0

\textbf{Abstract}

We present a proposal for the upgrade of Belle II data acquisition system based on a new detector independent readout architecture FELIX, Front-End LInk eXchange, developed by Brookhaven National Laboratory.

\textsuperscript{1}\texttt{dasner@bnl.gov}  
\textsuperscript{2}\texttt{chc@bnl.gov}  
\textsuperscript{3}\texttt{djaffe@bnl.gov}  
\textsuperscript{4}\texttt{bpal@bnl.gov}

(implicit) expectations: there will be a source of money to pay for this option (this includes manpower)
# The US-Japan Proposal: the Team

## U.S. Collaboration Members

<table>
<thead>
<tr>
<th>No.</th>
<th>Name</th>
<th>Affiliation</th>
<th>Position</th>
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<tbody>
<tr>
<td>1</td>
<td>Hucheng Chen</td>
<td>BNL</td>
<td>Physicist (PI)</td>
</tr>
<tr>
<td>2</td>
<td>David Jaffe</td>
<td>BNL</td>
<td>Senior Physicist (Co-I)</td>
</tr>
<tr>
<td>3</td>
<td>Shaochun Tang</td>
<td>BNL</td>
<td>Physics Associate II (Co-I)</td>
</tr>
<tr>
<td>4</td>
<td>Vladimir Savinov</td>
<td>University of Pittsburgh</td>
<td>Professor (Co-I)</td>
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## Japanese Collaboration Members

<table>
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<tr>
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<th>Position</th>
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<tbody>
<tr>
<td>1</td>
<td>Satoru Yamada</td>
<td>KEK</td>
<td>Associate Lecturer (PI)</td>
</tr>
<tr>
<td>2</td>
<td>Ryosuke Itoh</td>
<td>KEK</td>
<td>Professor (Co-I)</td>
</tr>
<tr>
<td>3</td>
<td>Mikihiko Nakao</td>
<td>KEK</td>
<td>Professor (Co-I)</td>
</tr>
<tr>
<td>4</td>
<td>Soh Suzuki</td>
<td>KEK</td>
<td>Associate Professor (Co-I)</td>
</tr>
<tr>
<td>5</td>
<td>Qidong Zhou</td>
<td>KEK</td>
<td>Postdoctoral Researcher (Co-I)</td>
</tr>
</tbody>
</table>
Begin forwarded message:

From: "Denisov, Dmitri" <denisovd@bnl.gov>
Subject: DAQ for Belle II
Date: April 18, 2019 at 4:01:27 PM EDT
To: "Chen, Hucheng" <cht@bnl.gov>
Cc: "Ma, Hong" <hma@bnl.gov>, "Jaffe, David" <djaffe@bnl.gov>

Dear Chen,

on the US-Japan proposal for Belle II DAQ. The final outcome was not to fund the proposal this time. Main concern is that Belle II did not select the final design for new DAQ system (while all referees agreed such upgrade is critical), so the recommendation is for the proponents to work with Belle II collaboration and when the plans are finalized and there is Belle II support for the proposal US-Japan will be glad to consider future proposals.

You will get formal feedback from DOE soon.

I'll be glad to talk more,
Dmitri.
BNL’s Decision on Their Proposal

To the Belle II DAQ Upgrade Committee:

We regret to inform the DAQ Upgrade Committee and the Belle II Collaboration that we must withdraw the “BNL proposal for the Belle II DAQ upgrade” from consideration. We have not been able to secure a satisfactory commitment from US funding agencies. We have sought and received commitments from other Belle II institutions, but we have not been able to identify sufficient funds to complete the work specified in our Letter of Intent. In addition, we do not have high confidence in our ability to secure funds to carry out the DAQ installation, commissioning and maintenance required by Belle II DAQ Upgrade Committee.

We thank our Pittsburgh and KEK colleagues for the fruitful, informative and enjoyable collaboration on FELIX R&D. We are sorry that we will not be able to continue this collaboration.

Hucheng Chen, David Jaffe
13 May 2019
Where does the “THERE IS NO MONEY FOR YOU” (FELIX) option take us from here?

1) BAD NEWS: There is NO DOE money available even for R&D work

2) More BAD NEWS: BNL can not continue without additional DOE funding

3) Pittsburgh will continue for as long as KEK is able to continue

4) “Resources” in Pittsburgh: students and bottomless reservoirs of enthusiasm

5) Our current plans:

   Start belle2link and b2tt integration with FELIX architecture FW

   Use FELIX architecture FW to implement slow control

NB: there is a world-wide FELIX expertise available and lots of development going on
Pitt setup with a full boardstack of TOP FEE

A working POCKET DAQ with both data and trigger paths for TOP FEE and L1

Another option (not shown) a working dummy FEE setup with custom FW on an HSLB (thanks to Yamada-san!)

DELL Precision 5820
16-core 3.7 GHz CPU Xeon W-2145
Test branch at KEK
Subject: Re: FELIX work in Pittsburgh / a brief description of plans / July 1, 2019

Date: Tue, 2 Jul 2019 11:16:23 +0900
From: zhouqidong <qidong.zhou@kek.jp>
To: Vladimir Savinov <vladimirsavinov@gmail.com>
CC: zhouqidong <qidong.zhou@kek.jp>

Dear Vladimir,

Sorry for the late reply.

1) as you suggested, we will try to integrate your belle2link and b2tt FW with the FELIX architecture FW ASAP - I have the tools and the framework installed already, but learning curve is definitely going to be steep (though also exciting).

Yes, this would be the first priority I think, for the about he b2tt part if you have any question, Nakao-san will provide helps
You can also ask him about how to preform the functionality test.

A particularly important task: resource usage for 24-channel FW with belle2link integration for all channels

A note concerning prior work:

1) In October 2018, Shaochun and Vladimir got b2tt part to work in Pittsburgh and hacked through to get data packets from TOP FEE (by piggy-backing on Pocket DAQ)

2) Qidong got belle2link part work both ways at KEK (reproduced using Qidong’s FW at KEK and Pitt)
2) as soon as we get your FW integrated with FELIX architecture, we should start working on slow control using your development.

Yes, this part would depends on the pcie express part, which is a little bit difficult what I can image now. But we can try to fix it together when we are at this step.

3) Then we would need a software framework to talk to slow control implementation on FELIX. This would also require to understand the architecture better.

This part is some how connect to the firmware implementation. to understand the FELIX software maybe takes time.

4) I would also like to see how the board and the chip perform with 12 instances of belle2link which are all programmed to push a lot of data through to some other ultrascale board (I have such with multiple transceivers, so this could be done).

Before to perform this test, I think it is better to add the event building (which now is taken care by Yamada-san), we need to add this part. Then maybe better to test with your TOP setup.

5) Wolfgang suggested to investigate latency associated with using FW on FELIX to read computer’s RAM to see if there could be a bottleneck there.

Yes, this is somehow important, since there is no memory on FELIX.

By the time of June 2019 B2GM we had already performed a detailed investigation of how to use the transceivers on the chip used on FLX-712 board - all this experience is very useful in general (even if not for Belle II DAQ upgrade)
Actual summer work: primarily by Xiao Han (was at KEK until Aug. 20)

Learning for VHDL and Testing for b2link in FELIX

Xiao HAN
Beihang University (x.han@buaa.edu.cn)

July 11, 2019, KEK, Japan

I’m from Beihang University, Beijing, China, and come here to learn / work on DAQ firmware upgrade especially for FELIX proposal. Because I am in the beginner level for both FPGA and VHDL, my mainly plan for this few month is about reading and learning.

Todo list for me during I staying at KEK, presented by Yamada-san.

1. Learn VHDL
   ✓ Try to understand HSLB module.
   ✓ Compile by ISE
   ✓ Modify codes and play with COPPER + FTSW

2. B2link in FELIX board
   ✓ Compile b2link on FELIX
     * read the code of b2link part in FELIX
     * Test it at B2 test bench

3. B2link part in the full FELIX firmware
   3.1 Compile the full FELIX firmware
   3.2 Implement the above b2link to FELIX
   3.3 Check signal with chipscope
Actual summer work at Pitt: primarily by Emil Allegria (and Vladimir)

Have to use VIVADO 2018.1 (to avoid regenerating of locked cores)

Generated the project for FULLMODE ("raw" data) / 24 channels version

Spent some time learning about FW structure and organization

/opt/Xilinx/Vivado/2018.1/bin/vivado

./firmware/scripts/FELIX_fullmode_top # to build VIVADO project do:
vivado -mode batch -source FLX712_FULLMODE_import_vivado.tcl

Focusing on two wrappers:

FELIX_FM_gbt_wrapper: the interface to transceivers / cores
TTC_FMC_wrapper: the interface to b2tt / TTC / FTSW

Vladimir promised (on July 11) to set up an SVN server with relevant parts of FELIX FW / architecture: WAS NOT DONE (my most sincere apologies). Main reason: realized that this was not a good idea. A git mirror would be a much better option - learned how to do this, will do (hopefully this week)
Actual summer work at Pitt: primarily by Emil Allegria (and Vladimir)

FLX card firmware: FromHost Data path

Host → Wupper → CR → GBT wrap. → fiber → GBT wrap. → CR → Wupper → Host

1. register_map_control.GBT_UPLNK_FQ_SEL(GBT_NUM-1 downto 0) = 0x0000000
2. register_map_control.GBT_DOWNLINK_FQ_SEL(GBT_NUM-1 downto 0) = 0x0000000

Relevant wrappers in FELIX FW
1) As before, there is NO DOE money available even for R&D work

2) As before, BNL can not continue without additional DOE funding

3) Pittsburgh will continue for as long as KEK is able to continue, but we have no MOU

4) “Resources” in Pittsburgh: students and bottomless reservoirs of enthusiasm

5) Our current plans remain the same:
   - Continue to work toward belle2link and b2tt integration with FELIX architecture FW
   - Use FELIX architecture FW to implement slow control

6) set up a git mirror for BELLE II FELIX developers (in case all this magically happens)