Status of IHEP Project for Belle II DAQ Upgrade

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2019 Belle II Trigger and DAQ workshop
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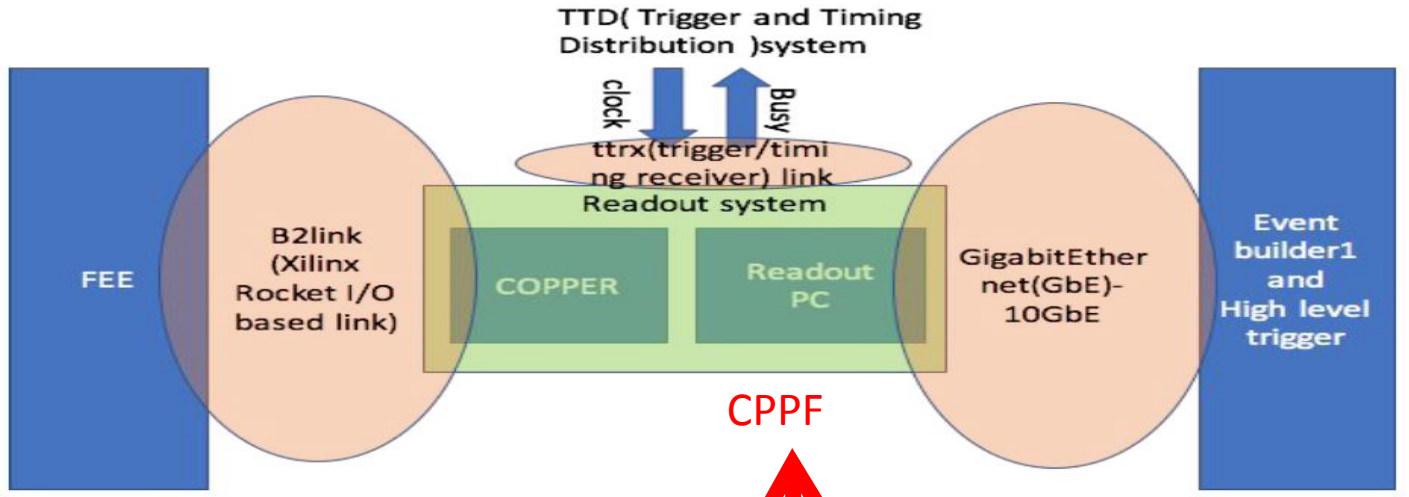
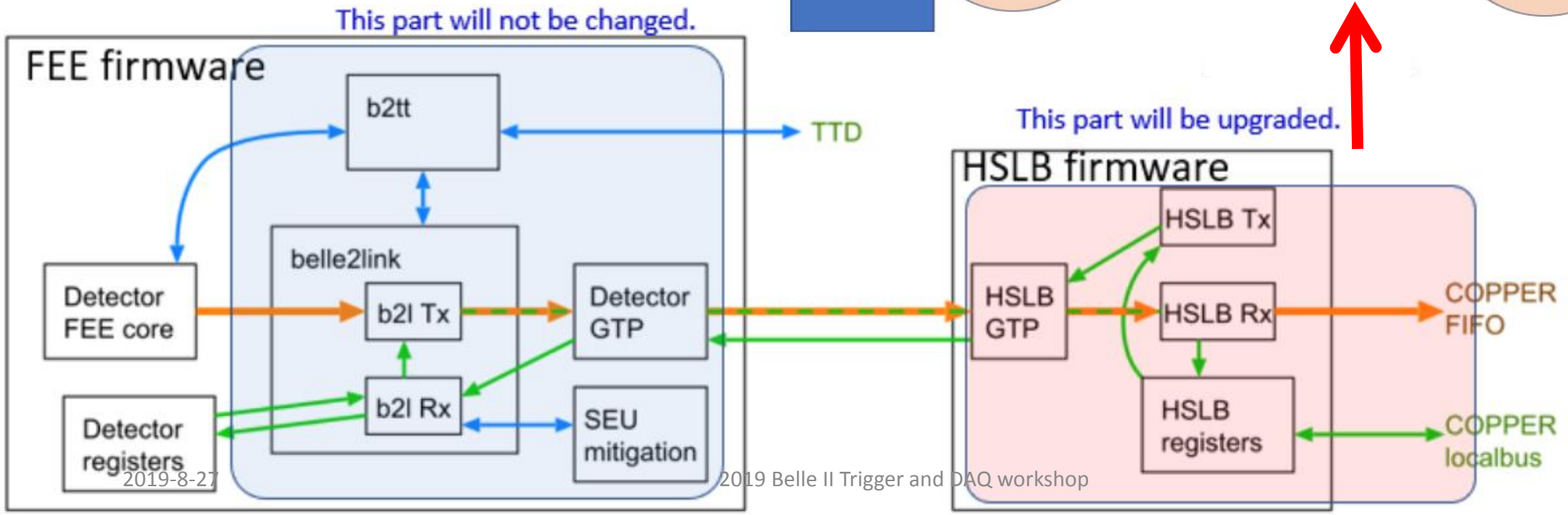
Outline

- IHEP Solution for Belle II DAQ upgrade
- CPPF introduce and upgrade
- Demo system at IHEP
- Progress/Status
- Summary

IHEP Solution for Belle II DAQ upgrade

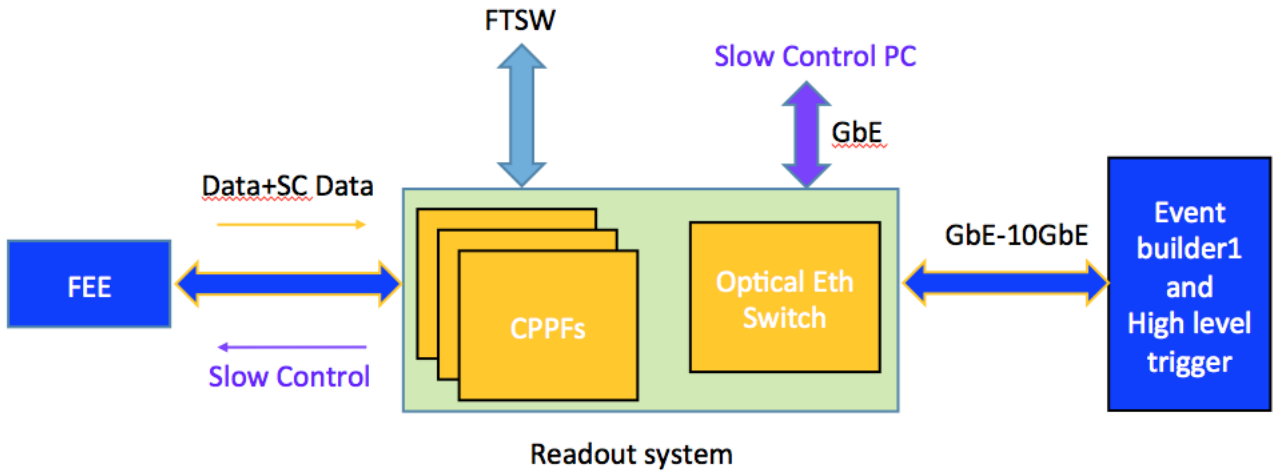
- Upgrading is straight forward:
  - Replacing HSLB/COPPER with CMS/CPPF designed by IHEP
  - Network link: GbE/10GbE

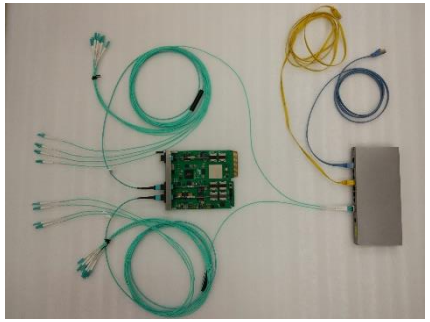




More on IHEP Solution for Belle II DAQ upgrade

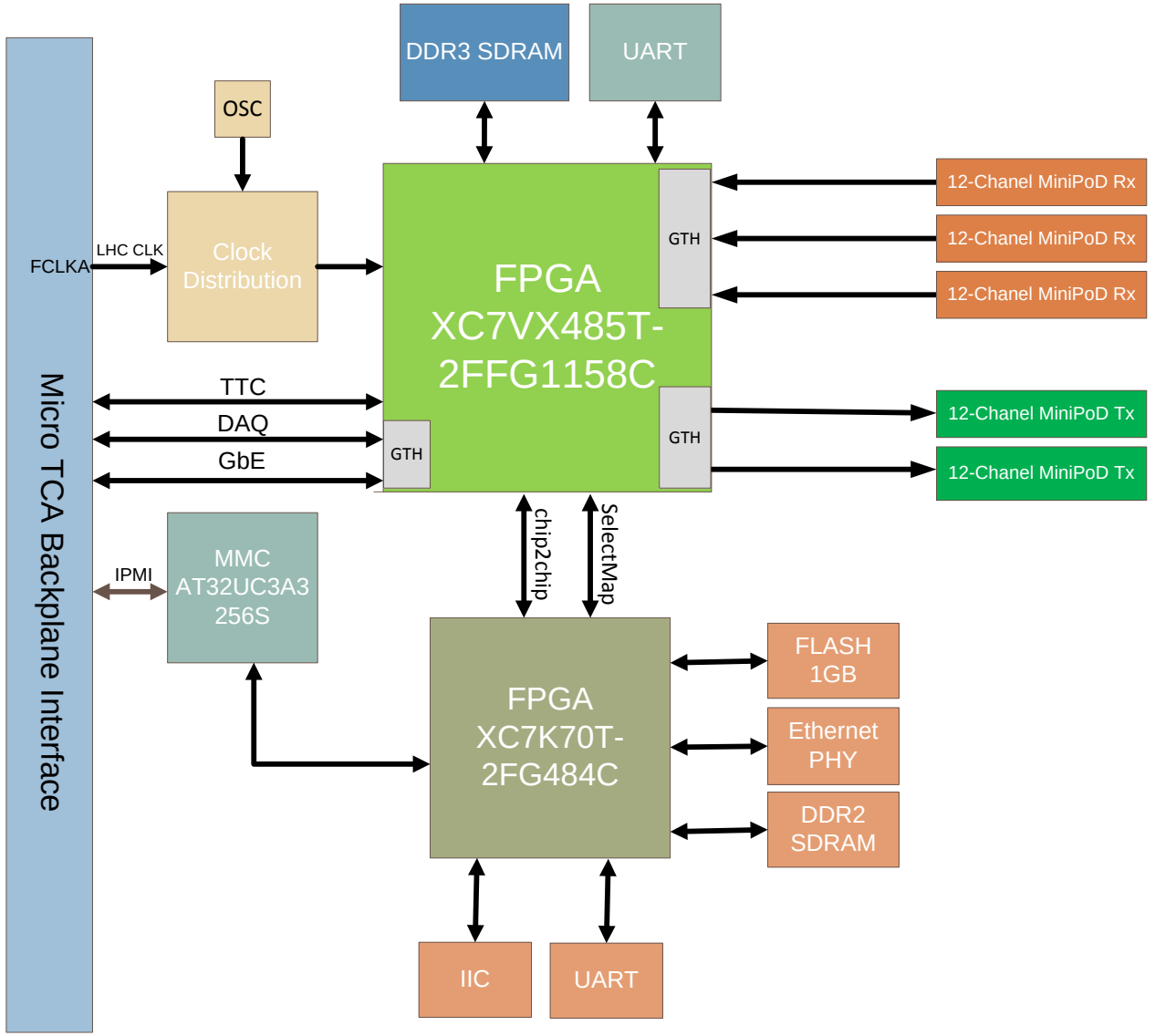
- Replacing HSLB/COPPER board with CPPF/CMS board/uTCA crate
- Merging/Concentration is based on 4 ports
- One CPPF board replaces 4-6 COPPERs(with HSLBs),24 input links (depends on system bandwidth)
- One CPPF outputs one or more 1/10GbE to Event builder
- One CPPF with 1/2 TTD interface
- One CPPF with one Slow Control network
- No change to other DAQ parts





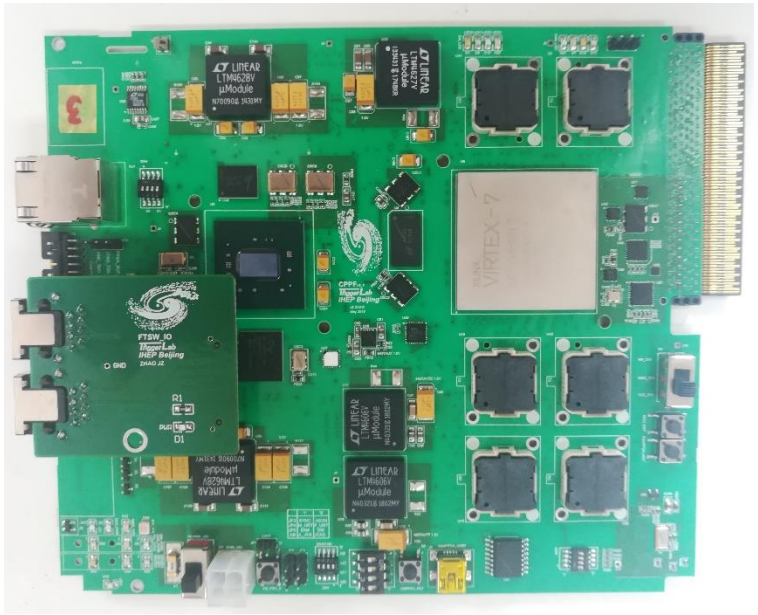
CPPF Introduction

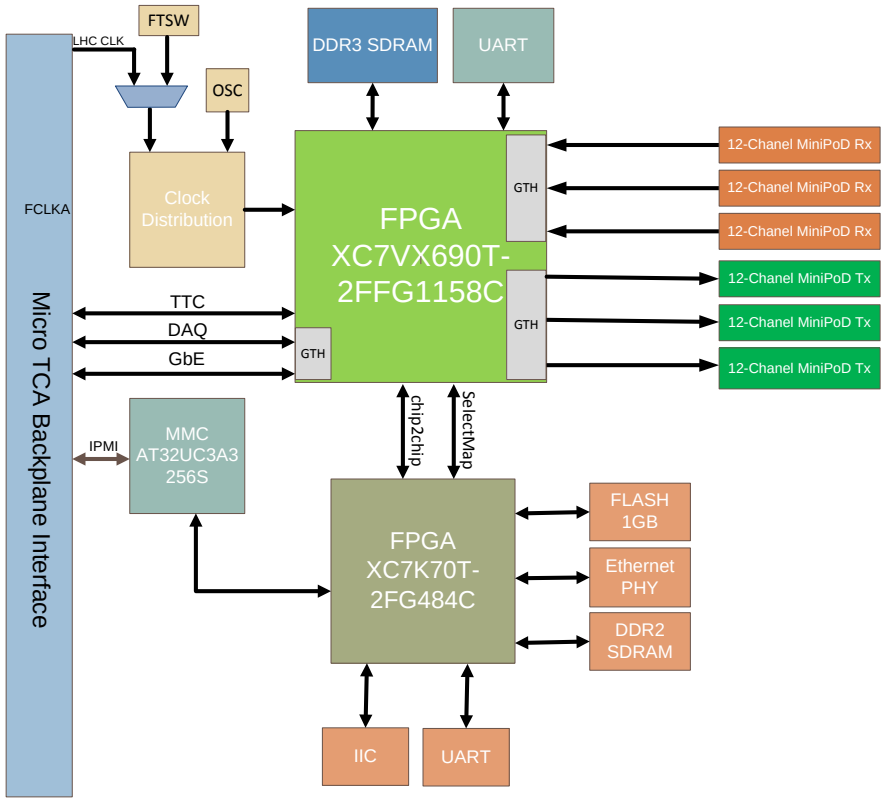
- Data throughput
  - 3 MiniPoD, support 360Gb/s INPUT,
  - 2 MiniPoD, support 240Gb/s OUTPUT
- XC7VX415T-2 (Virtex-7)
  - Core FPGA for data processing,
  - Pin compatible with XC7VX690T,
  - 48 channel GTH Transceivers，
  - Support up to 13.1Gbps per channel。
- DDR3 2Gb(pin compatible with 4Gb)
- XC7K70T-2 (Kintex-7)
  - Control FPGA,
  - Configure and Control CPPF.
- Flash 1GB
  - Configuration file store
- AT32UC3A1512 (Atmel)
  - MMC, Module Management Controller.



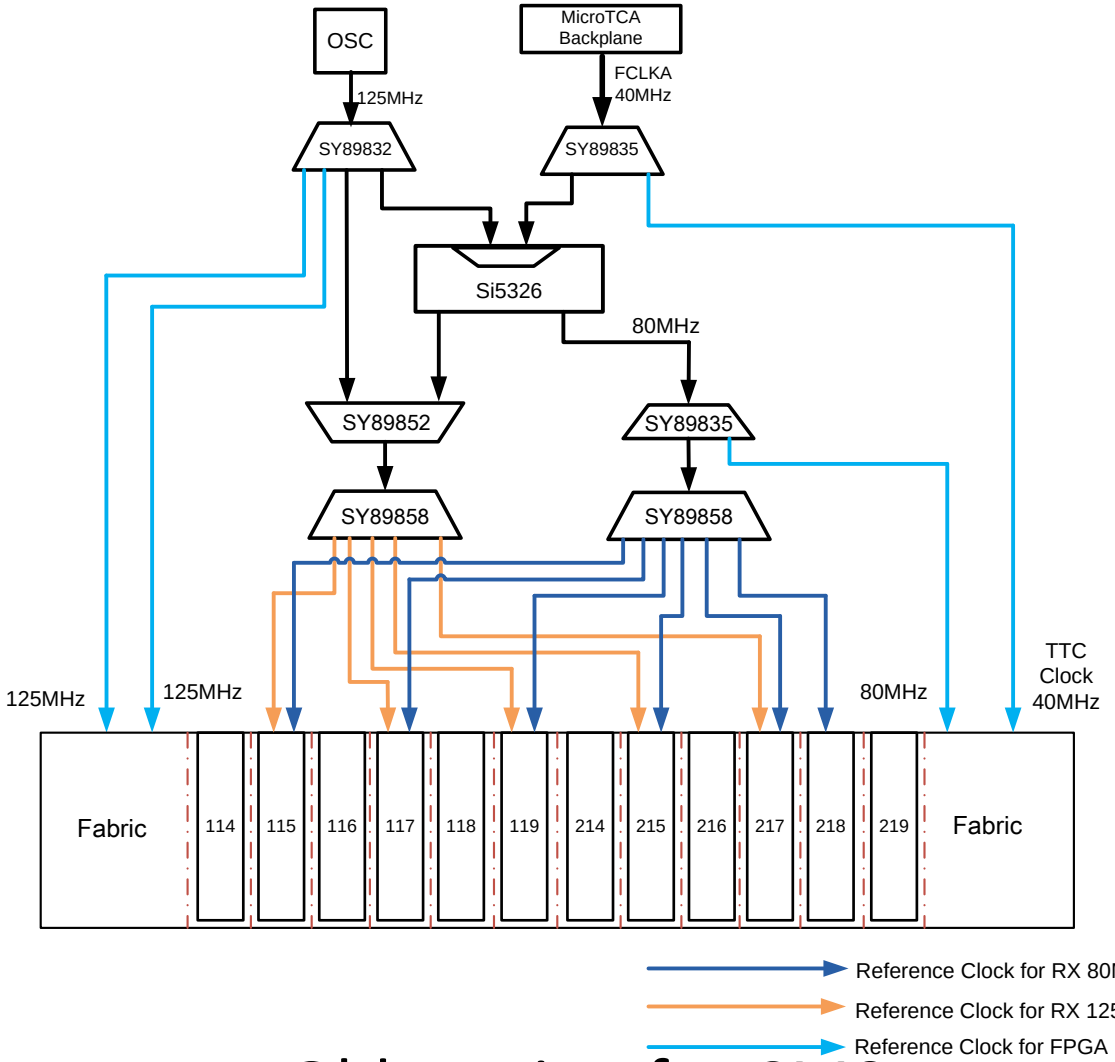
CPPF upgrade for BelleII

- XC7VX415T upgrade to XC7V690T
- Added one TX MiniPoD(12 TX channel),
- Total: 36 channel input, 36 channel output,
- Added 156.25MHz OSC for 10GbE,
- Added TWO FTSW RJ45 Ports,
- CPPF_V3_4 is ready and under testing.

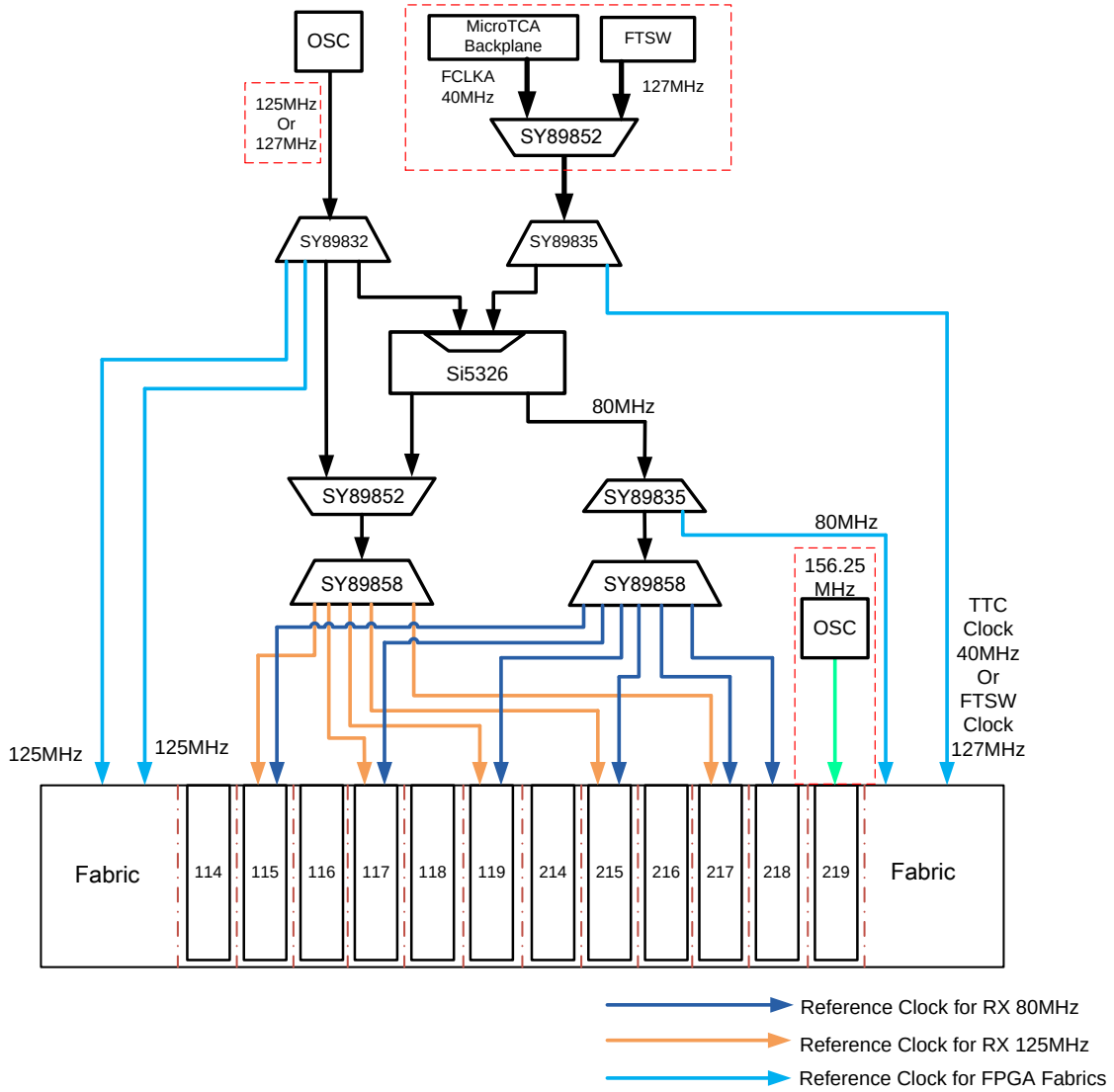




CPPF Clock Distribution



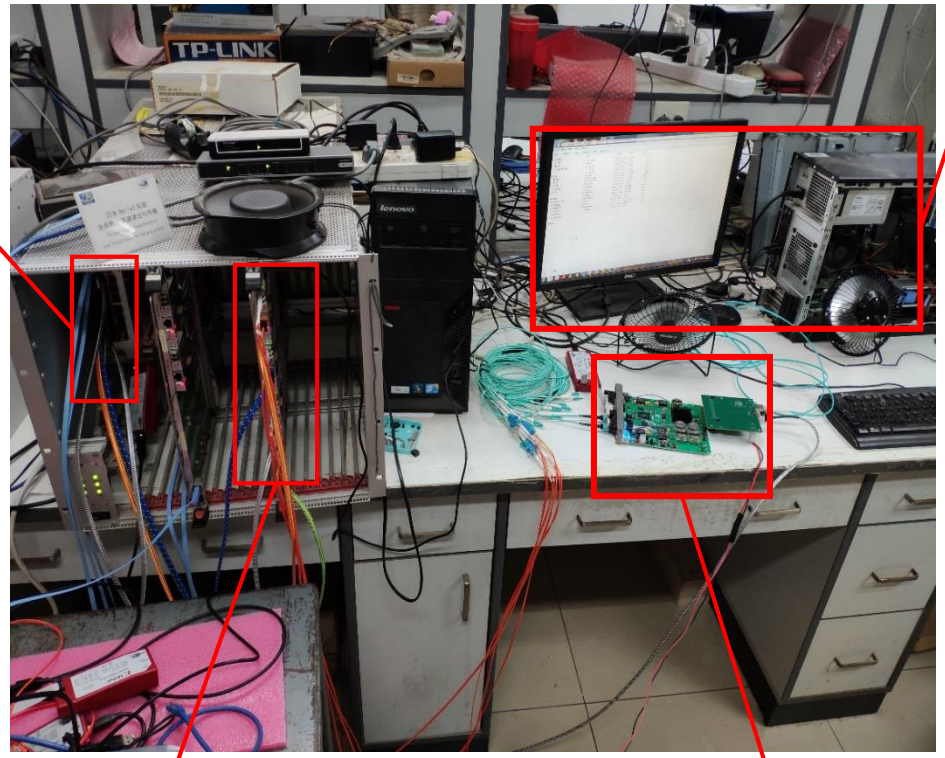
Old version for CMS

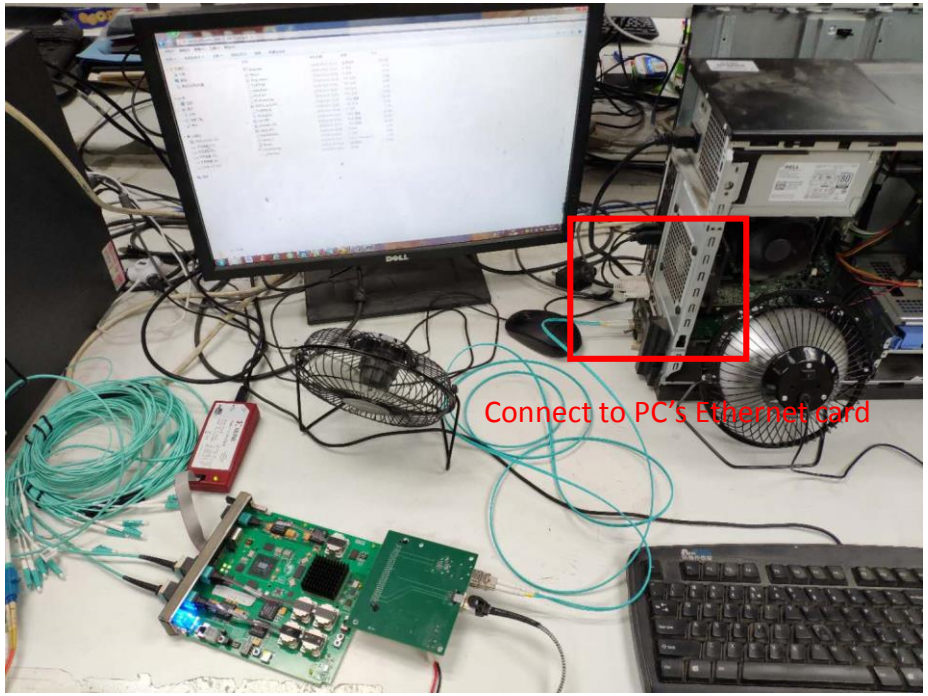


New version for Belle II

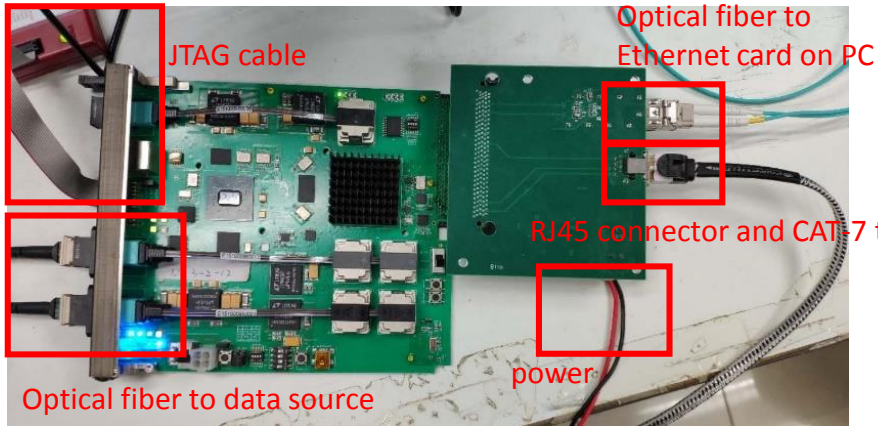
Demo system Setup at IHEP

- Photo of Full Demo System





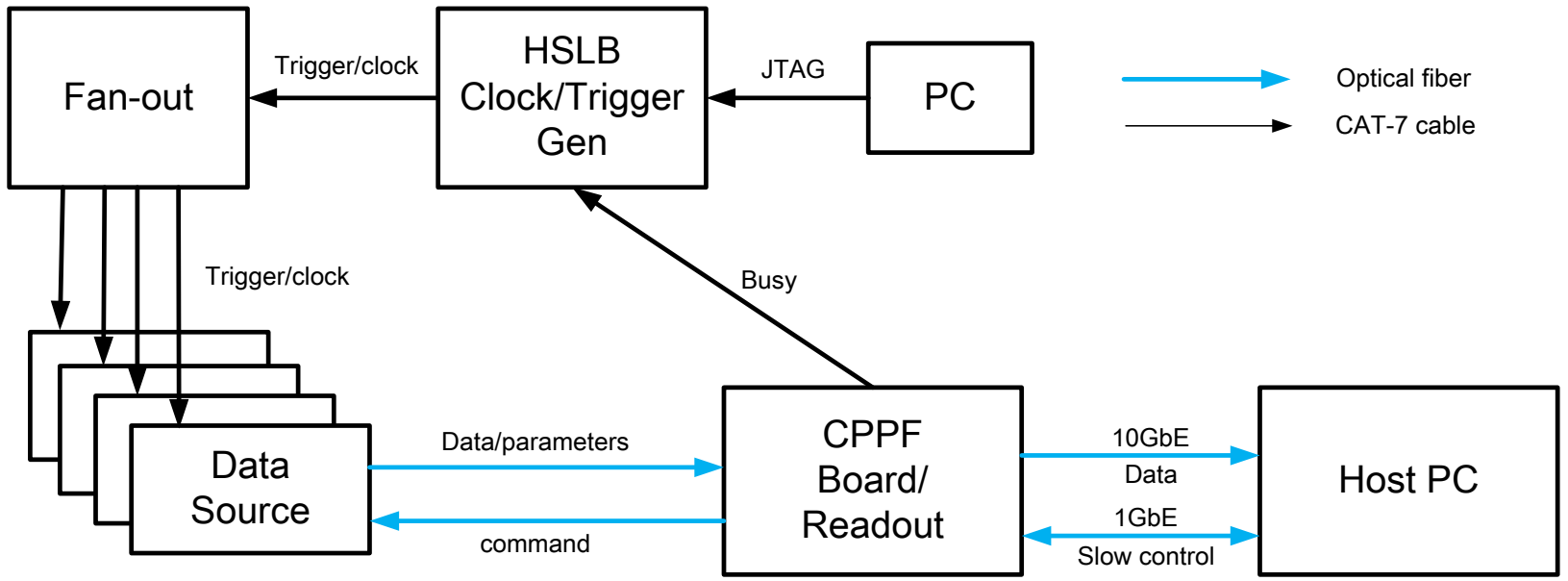
CPPF and PC in working



CPPF and Interface to FSTW/PC

Demo system Based on 10GbE

- HSLB Clock/Trigger Gen
  - --Generate 125MHz clock
  - --Generate trigger signal
  - Trigger rate is controlled by PC;
  - Trigger signal can be masked by feedback BUSY signal;
  - --send clock and trigger to fan-out board
- Fan-out board
  - Fan out 125MHz clock and trigger signal to Data source boards,
- Data source board
  - --use hslb as data *source (belle2link-0.19)*
  - --generate dummy data and provide some register for slow control test
- Readout board
  - use CPPF as readout board
  - implement belle2link(data merge and slow control) and some COPPER and ROPC function on it
  - output data to PC and receive command from PC via Ethernet.



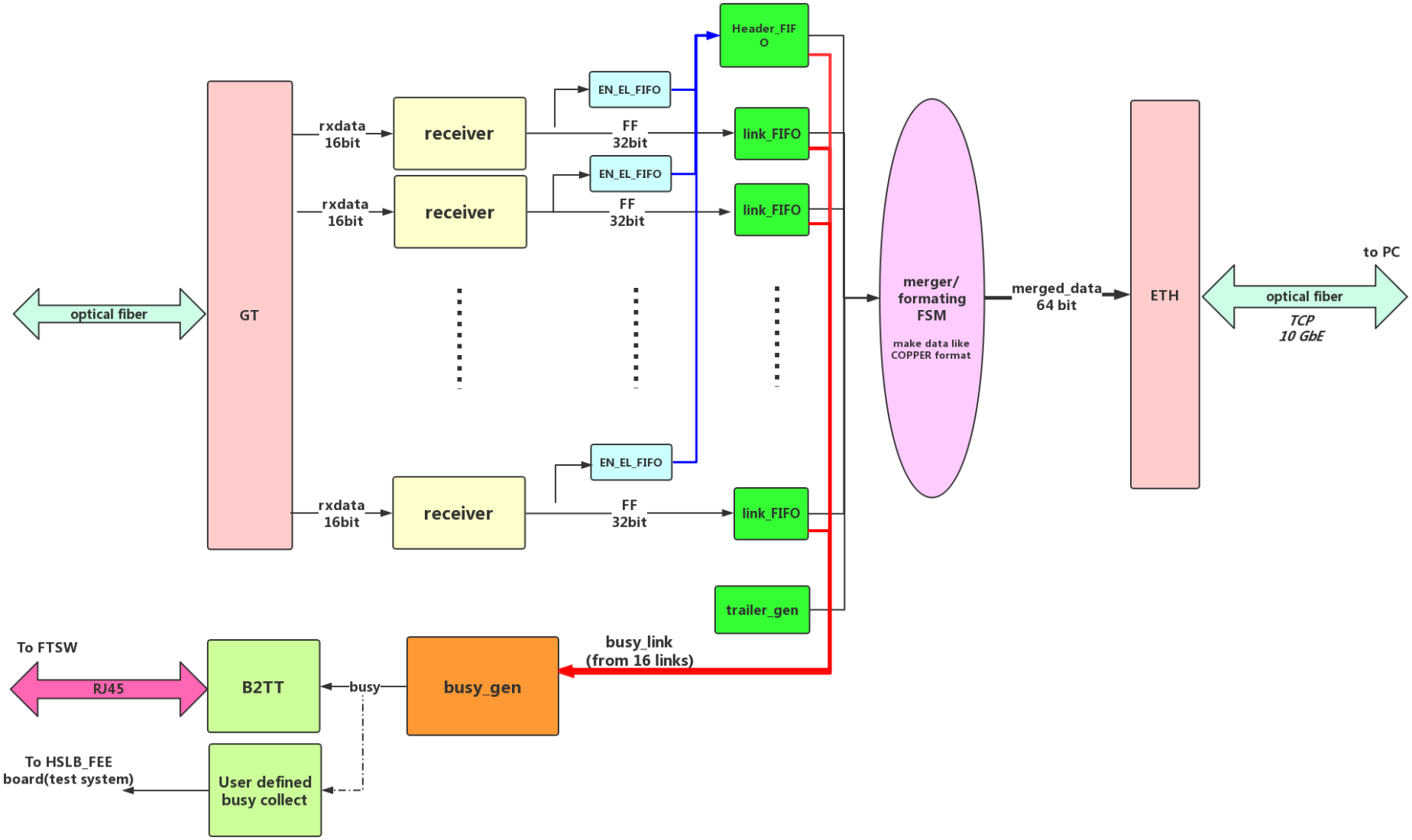
- host pc

  --receive data from CPPF through 10G Ethernet

  --send slow control command to CPPF via SiTCP

- Use an short-time(10min) evaluation version 10GbE IP core(from a company), implemented on CPPF

Firmware structure Data merger based on 10GbE

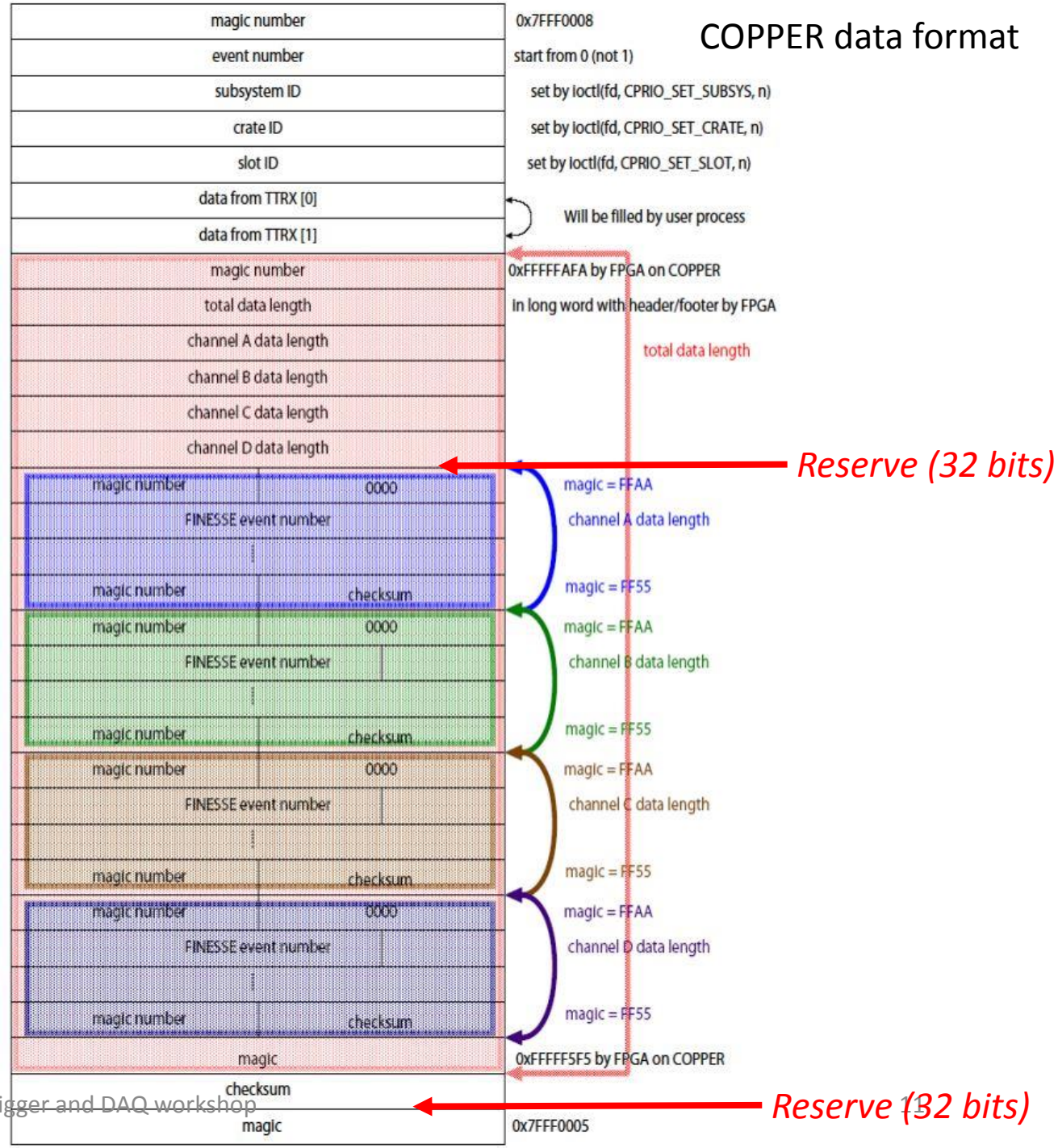


COPPER Data format based on 10 GbE(4 links)

- 10GbE IP core data width 64 bits;
- Old COPPER data format header:
  - 13*32bits

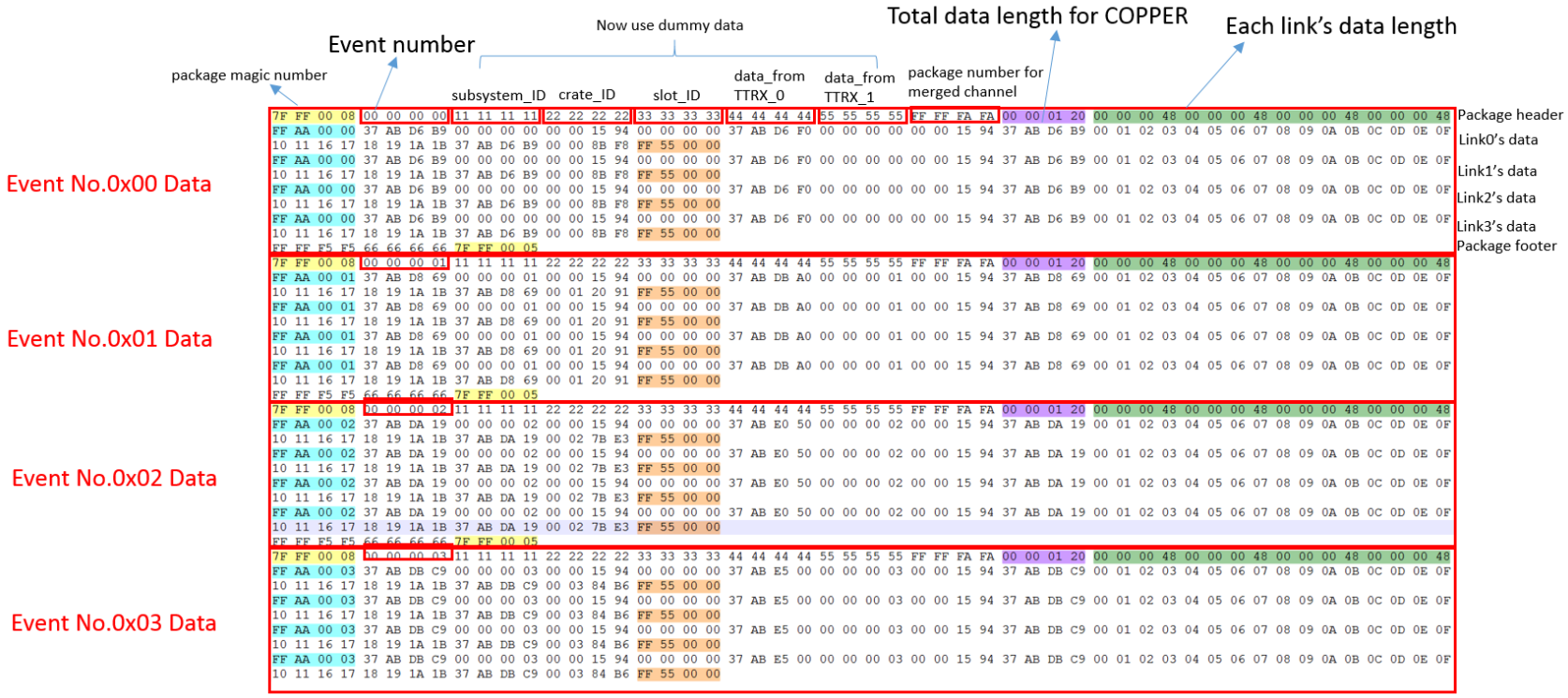
Modification on COPPER Data format:

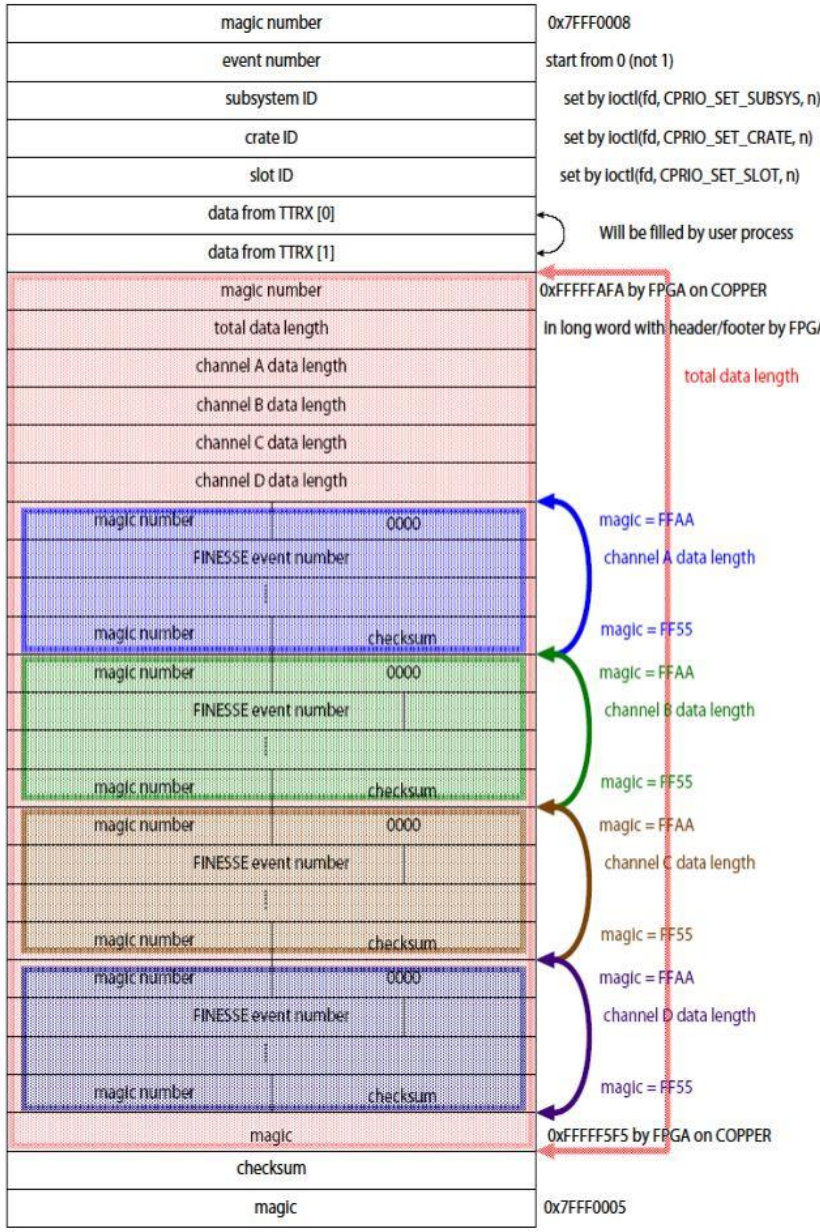
- Inserting a 32bit word called *Reserve* after *channel D data length,*
- make the header into 14*32bit,
- Inserting a 32bit word called *Reserve in trail,*
- *Make the trail into 4*32bit*



Merged data format(4 links)

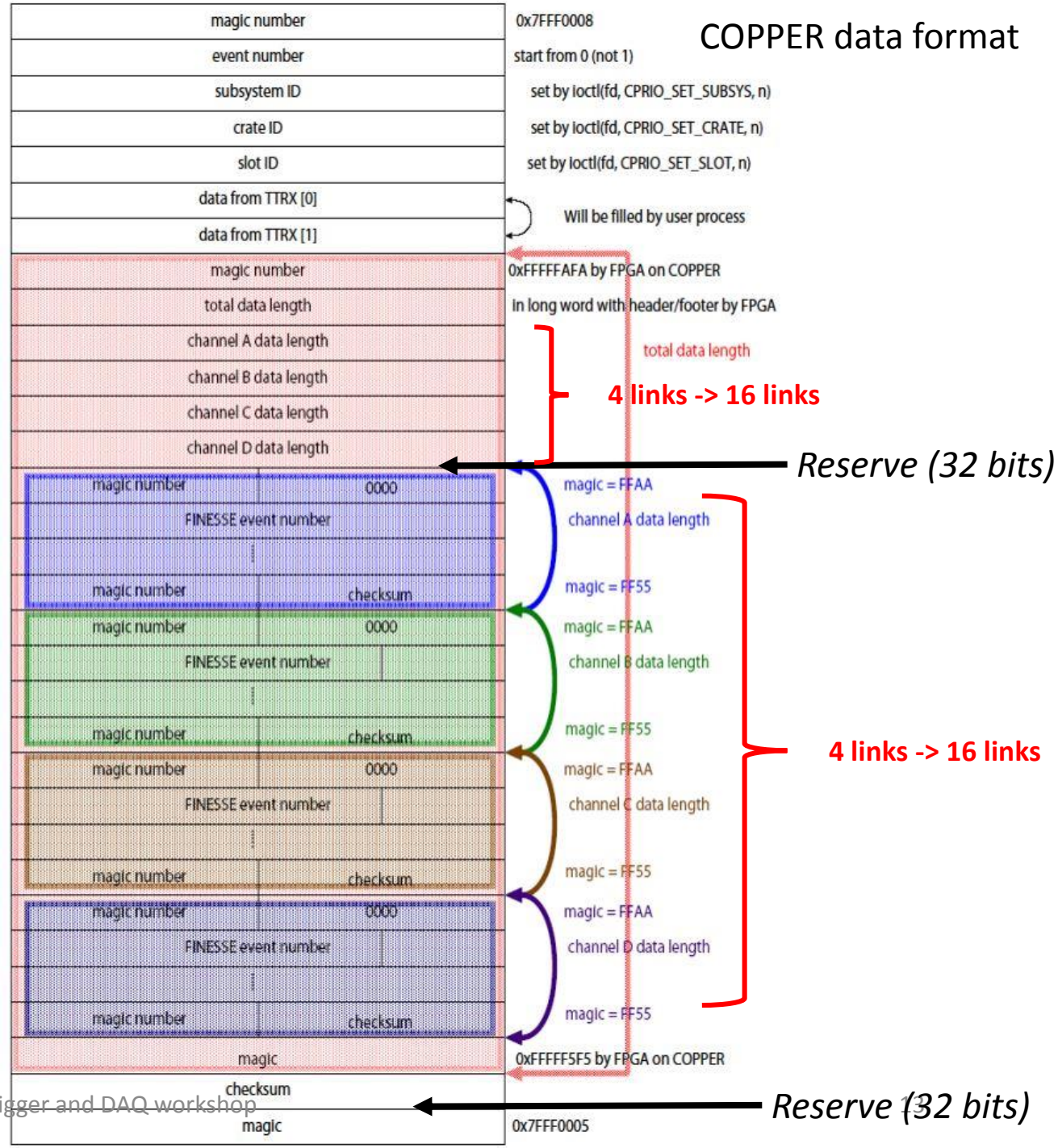
First 4 events shows below follows COPPER format, event number is incremented





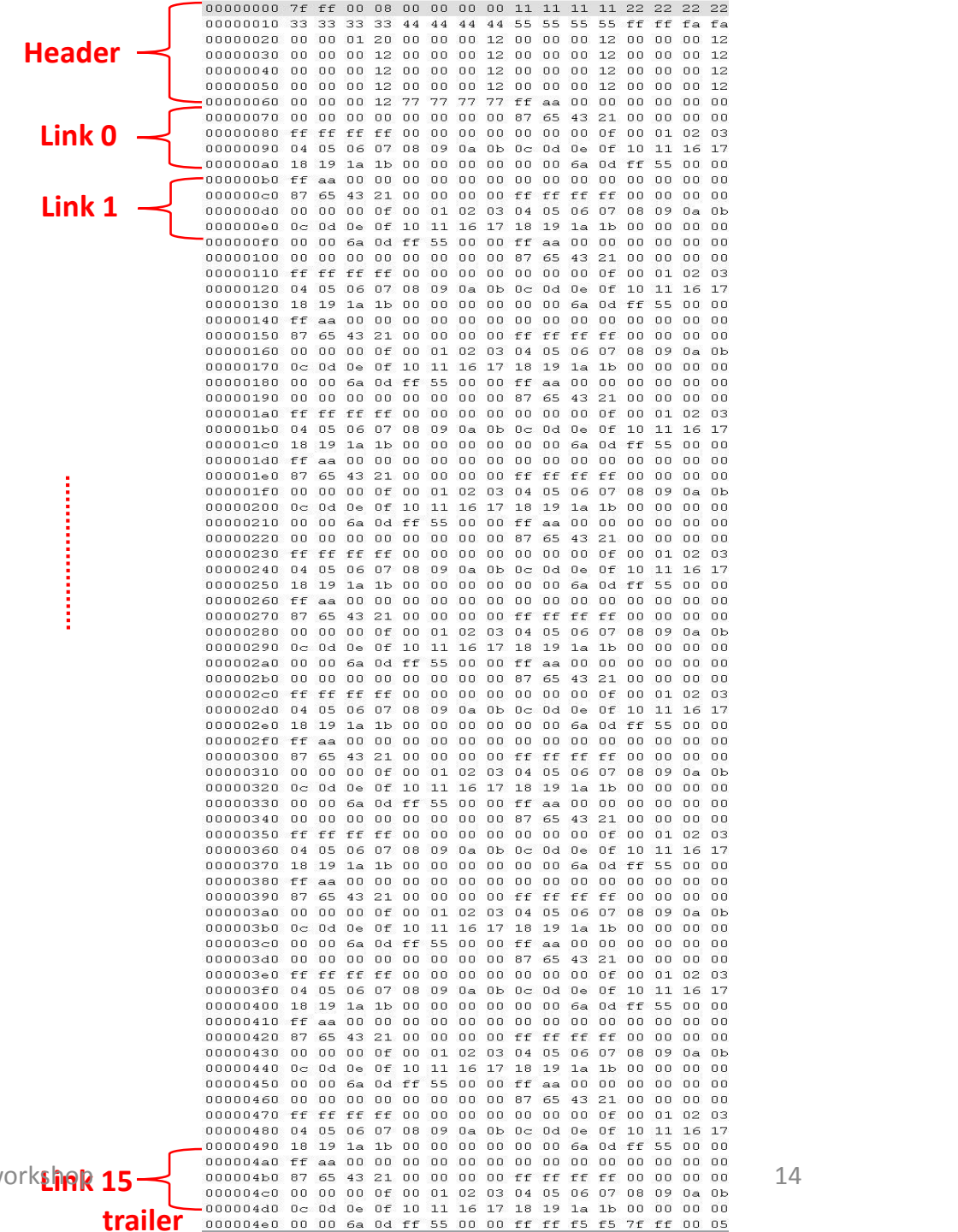
COPPER-like Data format based on 10 GbE(16 links)

- For 16 links
  - Similar to 4 link COPPER data format
  - Header add 12 more 32bit word to represent the data length of added links and *total data length* is the sum of 16 links' data length
  - 4 links -> 16 links data in one event
- Data format for 16 or 24 links should be further discussed with Yamada-san.

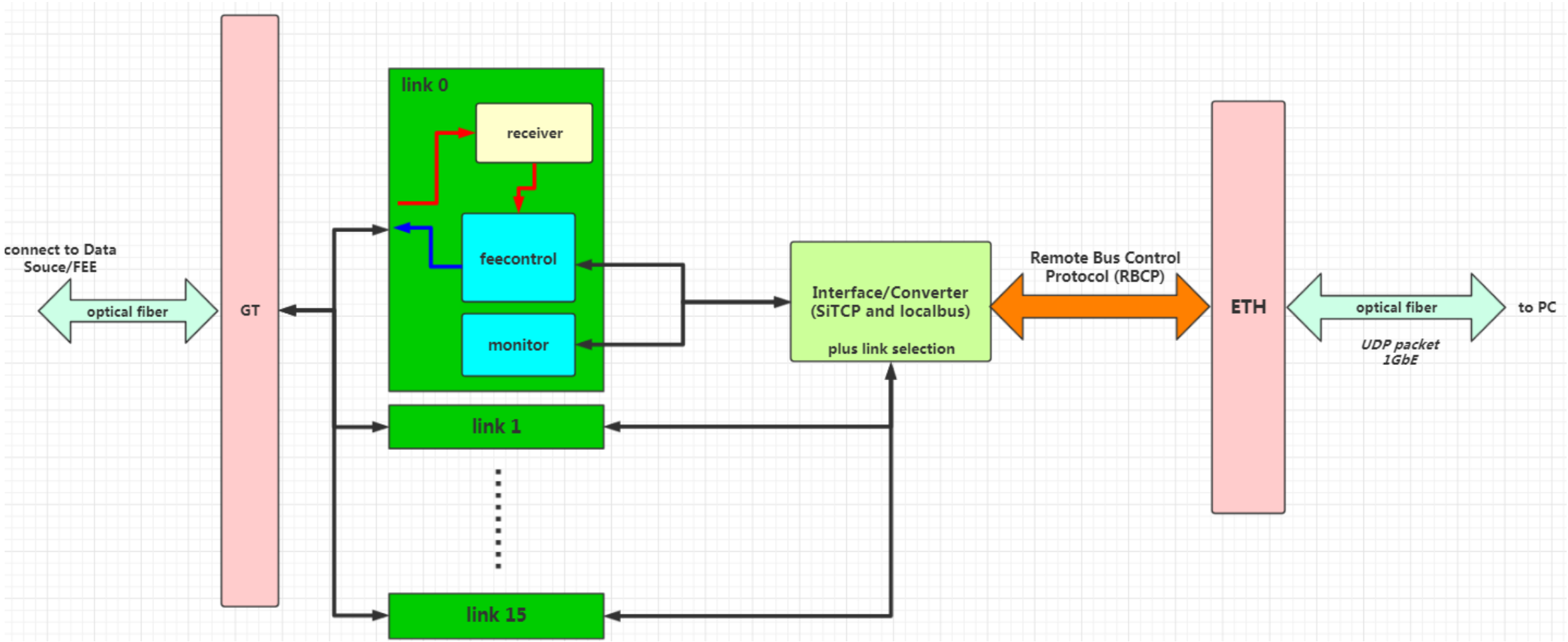


COPPER-like Data format based on 10 GbE(16 links)

- PC received data(1st event) is shown as right,
- COPPER event number and link event number are checked.
- Header of COPPER and link header and footer are checked.
- Event number are checked whether they are increased one by one.
- About 100 thousands events are received and checked, and data are correct.



Firmware structure-*Slow control*



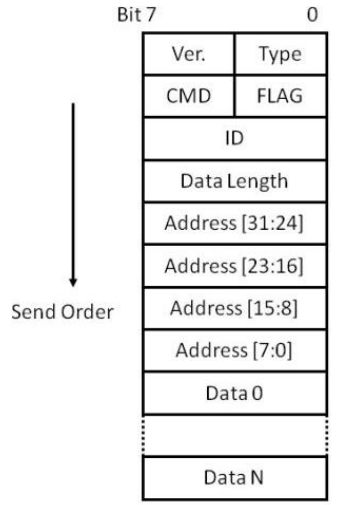
Firmware structure: Slow Control

Interface between *localbus* and *SiTCP*

Signal name	I/O	Description
RBCT_ACT	O	Indicates the bus operating.
RBCT_ADDR[31:0]	O	Address in access
RBCT_WE	O	Write enable
RBCT_WD[7:0]	O	Write data
RBCT_RE	O	Read enable
RBCT_RD[7:0]	I	Read data
RBCT_ACK	I	Access response

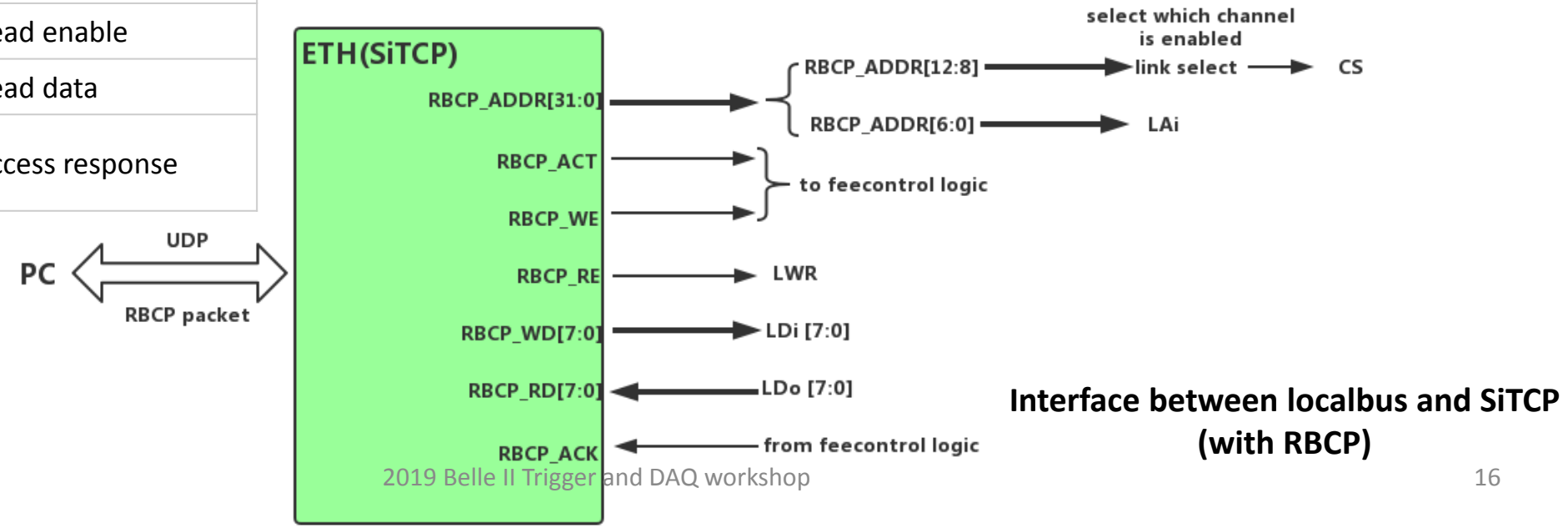
RBCP signal description

UDP RBCP packet format



CMD bit	Name	Description
3	Access	Bus Access
2	R/W	0: Write, 1:Read
1	Reserve	Always 0
0	Reserve	Always 0

FLAG bit	Name	Description
3	REQ/ACK	0: Request, 1: Acknowledge
2	Reserve	Always 0
1	Reserve	Always 0
0	Error	0: Normal, 1: Bus Error



Interface between localbus and SiTCP (with RBCP)

Slow control test result

Slow control

Main functions are realized and verified
--8 bit register read and write—*A7D8*
--32 bit register read and write—*A16D32*
--Stream write –*Stream*

```
SUN@SUN-PC /cygdrive/c/Users/SUN/Desktop/caopc_sitcpudp_new/RBCP_sample
$ ./rbcp.exe 192.168.10.16 4660
$ B2LDo -a -p delay 0x1
B2LDo: delay was set as: 0x01

$ B2LDo -b -p delay 0x2
B2LDo: delay was set as: 0x02

$ B2LDo -c -p delay 0x3
B2LDo: delay was set as: 0x03

$ B2LDo -d -p delay 0x43
B2LDo: delay was set as: 0x43
```

A7D8: Delay parameter was written and read back correctly

```
Administrator@PC-201707170902 /cygdrive/c/User
l_udp_tcp/B2linkTcpUdp
$ ./B2ldoTcpUdp.exe 192.168.10.16 4660

B2LDo$ setreg -c 0x0101 0x03050709

The register value was set as: 0x03050709
```

A16D32 example

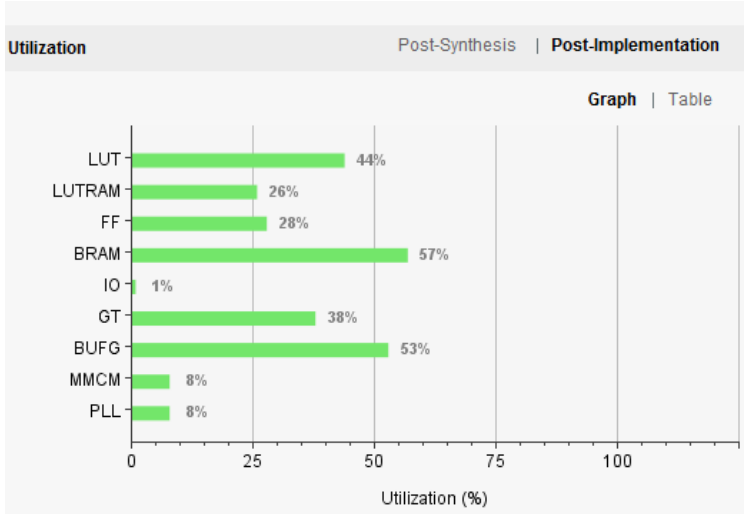
```
/cygdrive/c/Users/Administrator/Desktop/B2linkTcpUdp
Administrator@PC-201707170902 /cygdrive/c/Users/Administrator/Desktop/B2linkTcpU
dp
$ ./B2ldoTcpUdp.exe 192.168.10.16 4660

B2LDo$ testa7d8 -a 1000

The error count is 0

B2LDo$ testa16d32 -a 0x0101 1000

The error count is 0

B2LDo$ testa7d8 -a 10000

The error count is 0

B2LDo$ testa16d32 -a 0x0101 10000

The error count is 0

B2LDo$ testa7d8 -b 100

The error count is 0

B2LDo$ testa7d8 -c 100

The error count is 0

B2LDo$ testa7d8 -d 100

The error count is 0

B2LDo$ testa16d32 -a 0x0101 100

The error count is 0

B2LDo$ testa16d32 -b 0x0101 100

The error count is 0

B2LDo$ testa16d32 -c 0x0101 100

The error count is 0

B2LDo$ testa16d32 -d 0x0101 100

The error count is 0

B2LDo$
```

Test slow control, A7D8 and A16D32,
up to 10000 times w/r, without error

Resource utilization in CPPF

- 16 links version resource utilization in CPPF.
- BRAM is used 57% in old version of CPPF.
- And BRAM 34 % used in new version of CPPF.
- New version of CPPF based on xc7vx690t can provide enough BRAM for Data buffering.

Old CPPF
Device: Xc7vx415tffg1158-2

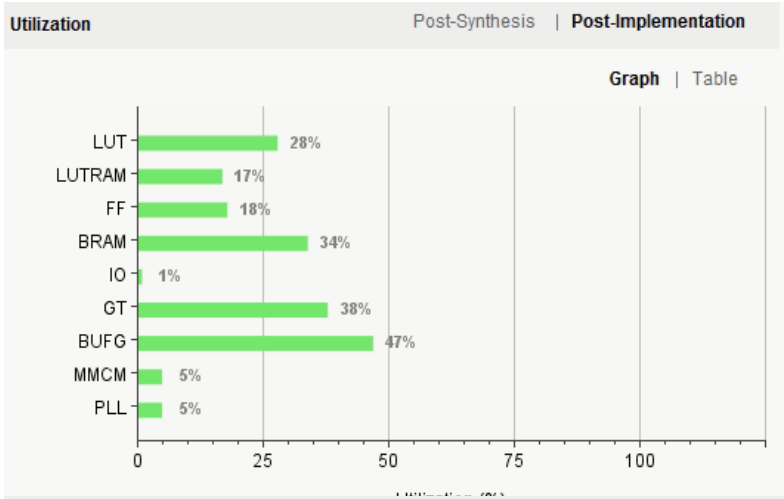


Utilization — Post-Synthesis | **Post-Implementation**

Graph | **Table**

Resource	Utilization	Available	Utilization %
LUT	112438	257600	43.65
LUTRAM	26936	104400	25.80
FF	143170	515200	27.79
BRAM	500.50	880	56.88
IO	5	350	1.43
GT	18	48	37.50
BUFG	17	32	53.13
MMCM	1	12	8.33
PLL	1	12	8.33

New CPPF for Belle II
Device: Xc7vx690tffg1158-2



Utilization — Post-Synthesis | **Post-Implementation**

Graph | **Table**

Resource	Utilization	Available	Utilization %
LUT	119362	433200	27.55
LUTRAM	29827	174200	17.12
FF	151970	866400	17.54
BRAM	498.50	1470	33.91
IO	4	350	1.14
GT	18	48	37.50
BUFG	15	32	46.88
MMCM	1	20	5.00
PLL	1	20	5.00

Status of the IHEP Demo system

- Based on 10GbE(4 channels)
  - Functions are based 4 inputs implementation of COPPER — Done
  - Data output to Event builder/readout PC via Optical Switch — Done
  - Four Slow control links in one CPPF — Done (simple CDC parameters)
  - TTD interface, BUSY handshake with FTSW — **Done** based on SiTCP, For 10 GbE Waiting for new version of CPPF
  - Data check function — Done
    - checking event number
    - CRC and others not yet
- Based on 10GbE(16 channels)
  - Functions are based 4 inputs implementation of COPPER — Done
  - Data output to Event builder/readout PC via Optical Switch — Done
  - 16 Slow control links in one CPPF — Done (simple CDC parameters)
  - TTD interface, BUSY handshake with FTSW — **Done** based on SiTCP, For 10 GbE Waiting for new version of CPPF
  - Data check function — Done
    - checking event number
    - CRC and others not yet

Manpower and tasks

- China side
  - Zhen-An LIU: Overall.
  - Jingzhou ZHAO/Jia TAO: Main person for the implementation.
  - Wenxuan GONG/Na WANG: Hardware modification and production.
  - Hanjun KOU: readout via 1G/10G Ethernet implementation with SITCP, B2TT implementation.
  - Pengcheng CAO: Slow Control and control firmware.
  - Jianing SONG: Hardware testing.
  - Two students from Fudan Uni. are also possible
- KEK side
  - Discussion: Yamada, Itoh,Nakao, Qidong
  - Firmware improvement later

Summary

- CPPF is the main board in IHEP Demo system for DAQ upgrade.
- New version of CPPF for Belle II is ready and under testing.
- Demo system at IHEP achieved success for 16 channels.
  - Based on 10GbE
- IHEP proposal could meet all requirement
  - Open, scalable, upgradable, re-configurable hardware platform
  - Suitable for future FEE and DAQ networking upgrade also
- Join test in KEK could start to plan.