- Belle II DAQ Upgrade -
Firmware development at KEK

Qi-Dong Zhou (KEK)
Outline

• Firmware development for DAQ upgrade
• Firmware development status for each functions
  • Belle2link implementation for the new system
  • User logic (event building) implementation
  • Slow control function
• Summary
Overview of Belle II readout system

- Belle2link, FTSW interface, slow control, pre event building
- PCIe / Ethernet …
## Functions require firmware development

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<th>Belle2link (data)</th>
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<th>B2tt (include busy handshake)</th>
<th>User logic (event building)</th>
<th>Interface with PCs (PCle/Ethernet)</th>
<th>SLC software</th>
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<td>D) User logic, event-building</td>
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<td>E) Slow control</td>
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Belle2link establishment

HSLB

- `hslb_feecontrol.vhd`
- `txstate = '0000'`
- Send "00bc"
  - 20x65536 times (10ms)
- Send "951c"
- Send "00bc"
- `prog_empty = '1'` and `LEMPTY = '1'`
- Send "95fb"
- Send request

FEE

- `b2l_receiver.vhd`
- `txstate = '0000'`
- `b2llost = '1'`
- Receive 256 x "00bc"
- Receive "95fb"
- `ZERO` (LinkOff)

FEE

- `b2l_transmitter.vhd`
- `txstate = '0000'`
- `txstate = 4`
- `if dataprogbuffull = '1'`
- `else if txstate = 4`
- `txstate` incremented by 1 after 0.5ms, if `b2llost` remains '0'
- Send "00bc"
- Send "95fb"
- `ONE` (LinkOn)

HSLB

- `hslb_receiver.vhd`
- Every state
- `if gtpreset = '1'` or `sig_linkdown(0) = '1'`
- Receive "951c"
- AlignCnt = 15
- 15 consecutive "00bc" receives make AlignCnt=15
- Send "951c"
- AlignCnt = 15
- `ONE` (LinkOn)

BUSY <= not linkup

FTSW

b2tt.payload error checks

not sig_b2lreset (linkdown) and sig_initdone (initdone) => b2lready
b2l establishment and data transfer

- Full b2l functions has been implemented.
- Tested performed based on FELIX (Kintex UntraScale) and dummy FEE (HSLB).
- Test was first done at KEK test bench, then confirmed at BNL and Pittsburgh.
User-logic (formatting, event-building)

Basically, the tested part in HSLB is just implemented to PCIe40 FPGA.

S. Yamada

Currently, only one input is connected so again, data stream is duplicated and merged.

Converting 256 to 16 bit is not necessary in future.
Functionality confirmed by Signal Tap

- Currently, data are checked by signal tap.
- More detailed check will be done by read out software.
- Test of 24/48 inputs also should be done for high-rate test.
- This part can be used also by FELIX or CPPF, if needed.

Still needs more detailed check.
SLC interface

- **IP**
- **FIFO**
- Serial data flow
- Parallel data flow

Diagram:
- **FEE**
  - TX
  - RX
  - GT transceiver
- **hslb_slc_wapper**
  - hslb_slc
  - SLC protocol
  - State machine & control
- **RegCmd**
- **ParaIn**
- **DataIn**
- **RegStatus**
- **ParaOut**
- **PCIe**
- **Readout PC**
SLC FIFO data structure

MSB  64bit width

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<tr>
<td>73</td>
<td>0a</td>
<td>08</td>
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<tr>
<td>cmd/file</td>
<td>type</td>
<td>addr</td>
<td>data</td>
<td>end</td>
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<td>04</td>
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<tr>
<td>cmd/file</td>
<td>type</td>
<td>addr</td>
<td>data</td>
<td>data</td>
<td>length</td>
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<td>73</td>
<td>0b</td>
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<td></td>
</tr>
<tr>
<td>cmd/file</td>
<td>type</td>
<td>data</td>
<td>data</td>
<td>x</td>
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<tr>
<td>00</td>
<td>09</td>
<td></td>
<td></td>
<td></td>
<td>08/04</td>
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<tr>
<td>cmd/file</td>
<td>type</td>
<td>data</td>
<td>data</td>
<td>data</td>
<td>data</td>
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16 bit width

<table>
<thead>
<tr>
<th>addr</th>
<th>data</th>
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<tbody>
<tr>
<td>addr</td>
<td>xx</td>
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<tr>
<td>6a</td>
<td>xx</td>
</tr>
<tr>
<td>6b</td>
<td>xx</td>
</tr>
<tr>
<td>6c</td>
<td>xx</td>
</tr>
<tr>
<td>6d</td>
<td>xx</td>
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</tbody>
</table>

(7 downto 0)  (7 downto 0)  (15 downto 8)  (23 downto 16)  (31 downto 24)
Test bench for SLC w/ COPPER

CDC FEE

GT transceiver

RX

TX

hslb

localbus

Address

Data

Control &
state machine

KEK specific

hslb_slc

hslb_slc_wapper

Serial data flow

Parallel data flow

IP

FIFO

SLC protocol

state machine & control

RegCmd

ParaIn

DataIn

RegStatus

ParaOut
Test the functionality based on COPPER
SLC functionality test with PCIe40

Access the register with address 0x0012 of FEE

Return the data of 0x03000843 from register address 0x0012 of FEE
Summary

- Functions of belle2link, FTSW interface, pre event building and slow control need firmware development for Belle II DAQ upgrade.
- Full b2l function was implemented for all three proposals. For the FELIX (GTH, Kintex Ultrascale) b2l was tested at KEK, BNL and Pittsburgh.
- User logic (pre event building) and slow control were ready for all three projects. Currently, they were implemented to PCIe40, and PCIe40 already get full functions could be tested with current Belle II DAQ system.
Backup
Schedule & Prospects

<table>
<thead>
<tr>
<th>Tasks</th>
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<th>2020</th>
<th>2021</th>
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<tr>
<td>Firmware development</td>
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<td>Device driver</td>
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<td>Prototype board*</td>
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<tr>
<td>Firmware implementation</td>
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<tr>
<td>Test w/ prototype board</td>
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<tr>
<td>Readout test with FEE</td>
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<td>Mass Production*</td>
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<td>Installation &amp; commissioning</td>
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*: Depending on the budget

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<tbody>
<tr>
<td>Slow control (implement, software)</td>
<td>20-30</td>
<td>1-15</td>
<td>16-31</td>
<td>1-15</td>
<td>16-30</td>
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<tr>
<td>User logic (implement)</td>
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<td>Long-term stability test</td>
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<td>B4 TOP test bench</td>
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Readout test with HSLB

HSLB(dummy data source) -> HSLB(duplicate event -> merged) -> COPPER

Red: header of readout board (RawCOPPER header)
BLUE: header of each link
GREEN: padding for converting to 256bits-width

Read data: 480 : LEF_FF = 1

 Todo
- Implement to New ROB firmware. (Currently, try to implement it in PCIe40)
- Functionality of data-checking
- Belle2link event-data from FEE has the minimum unit of 32bits = 1 word.
- The output width should be larger for high throughput.

**Example:** if 14 word/event for link #0 and 12 word for link #1.

**Data FIFO For #0**

```
1  2  3  4  5  6  7  8
9 10 11 12 13 14  P  P
```

256bits = 8 words

**Data FIFO For #1**

```
1  2  3  4  5  6  7  8
9 10 11 12  P  P  P  P
```

**Output data (not considering data-reduction/hdr/trl here)**

```
1  2  3  4  5  6  7  8
9 10 11 12 13 14 1  2
3  4  5  6  7  8  9 10
11 12  P  P  P  P  P  P
```

This part needs to be removed downstream. (driver, software or?)
### TX FIFO data structure

<table>
<thead>
<tr>
<th></th>
<th>MSB</th>
<th>64bit width</th>
</tr>
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<tbody>
<tr>
<td></td>
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<td></td>
</tr>
<tr>
<td>TX FIFO</td>
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</tbody>
</table>

#### A7D8 write
- **cmd/file**: 73
- **type**: 07
- **addr**: 08
- **data**: end

#### A7D8 read
- **cmd/file**: 73
- **type**: 0a
- **addr**: 08
- **x**: end

#### A16D32 write
- **cmd/file**: 73
- **type**: 0b
- **addr**: addr
- **data**: data
- **length**: continue
- **end**: x

#### A16D32 read
- **cmd/file**: 73
- **type**: 0c
- **addr**: addr
- **data**: data
- **length**: continue
- **end**: x

#### Serial stream (files)
- **cmd/file**: 00
- **type**: 09
- **data**: data
- **length**: end/continue
- **08/04**: