- Belle II DAQ Upgrade -
Firmware development at KEK

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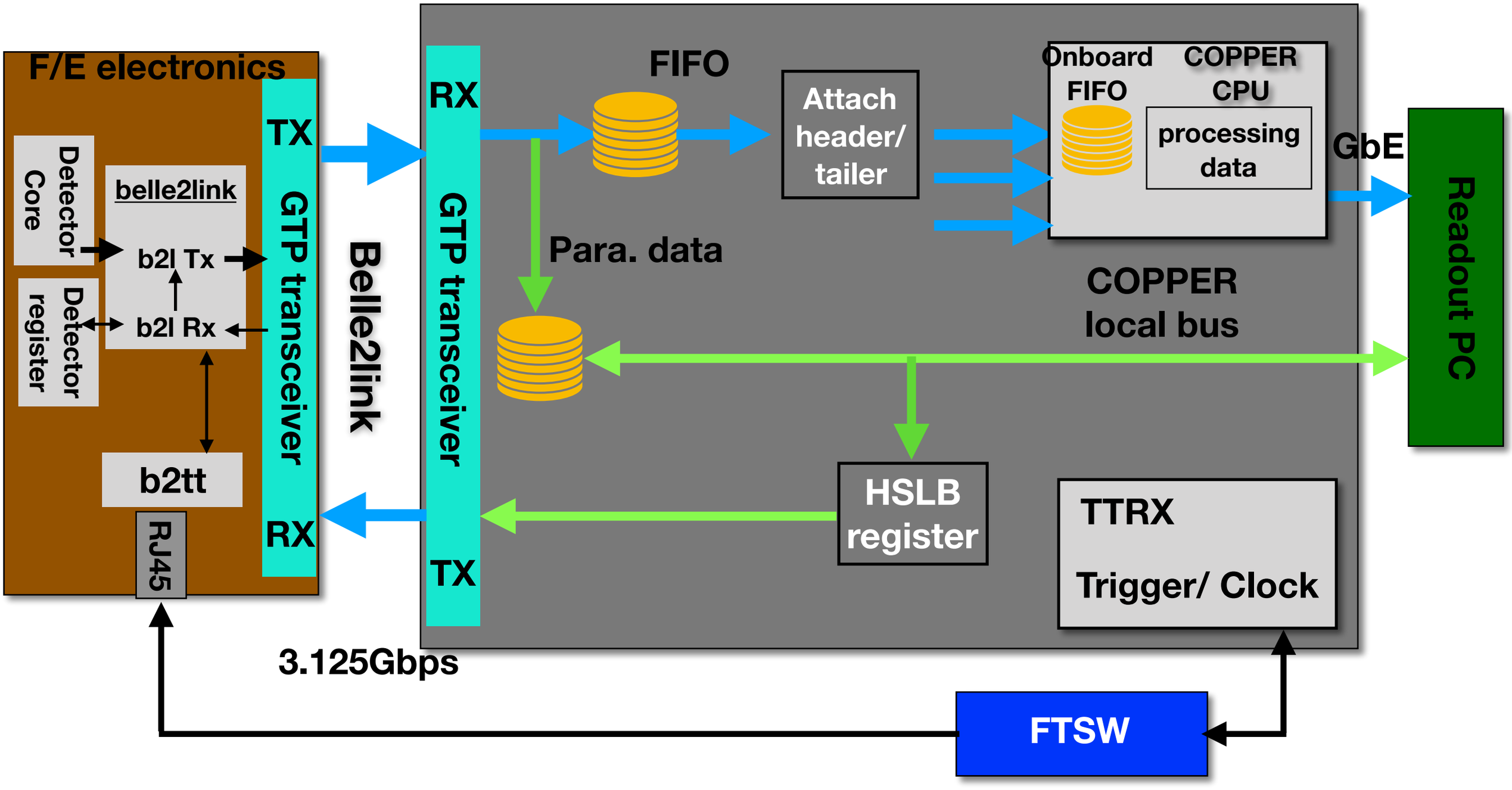
DAQ UPGRADE SESSION
TRG/DAQ Workshop 2019, Yonsei University, 26-29 Aug. 2019

Outline

- Firmware development for DAQ upgrade
- Firmware development status for each functions
  - Belle2link implementation for the new system
  - User logic (event building) implementation
  - Slow control function
- Summary

Overview of Belle II readout system

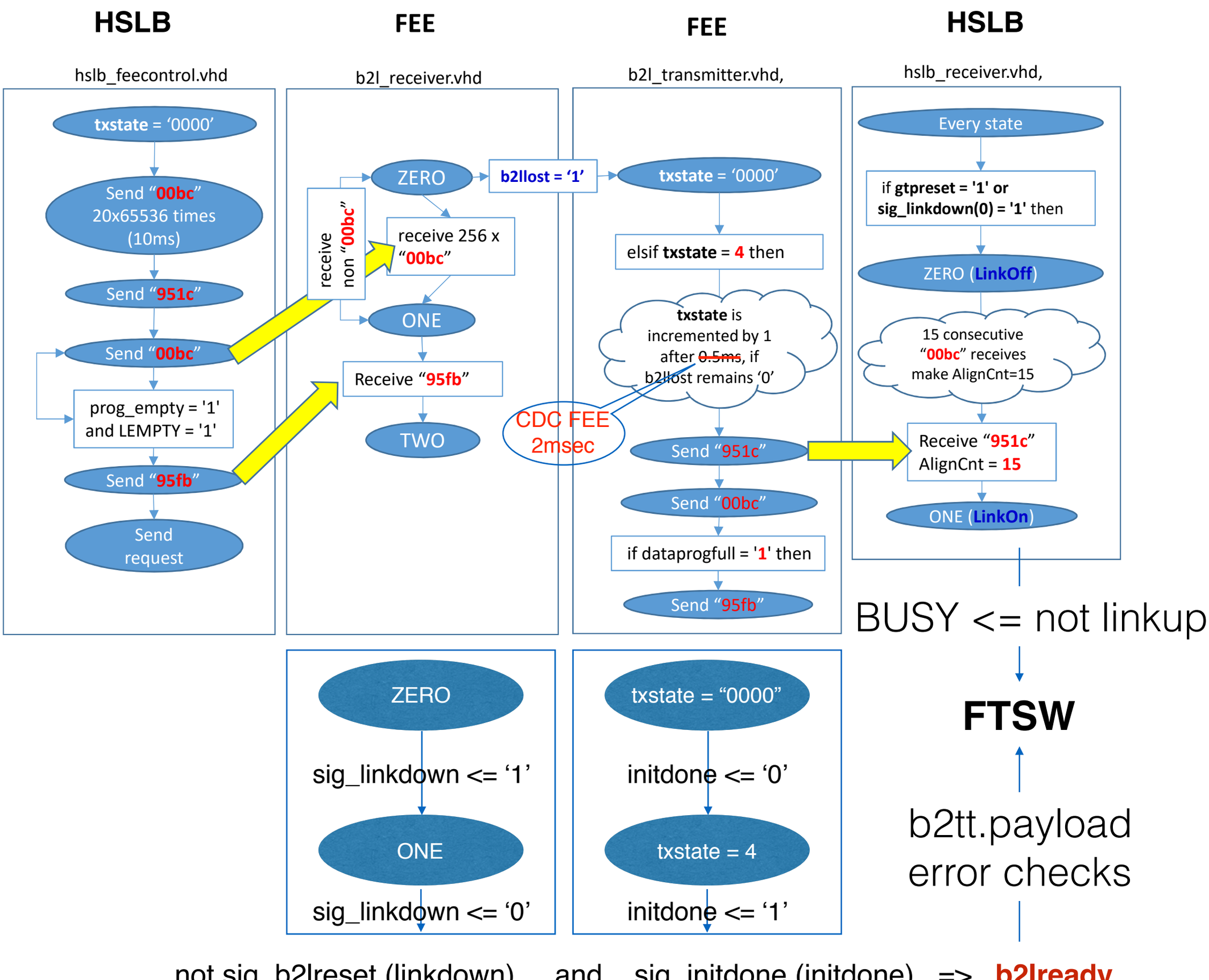


- Belle2link, FTSW interface, slow control, pre event building
- PCIe / Ethernet …

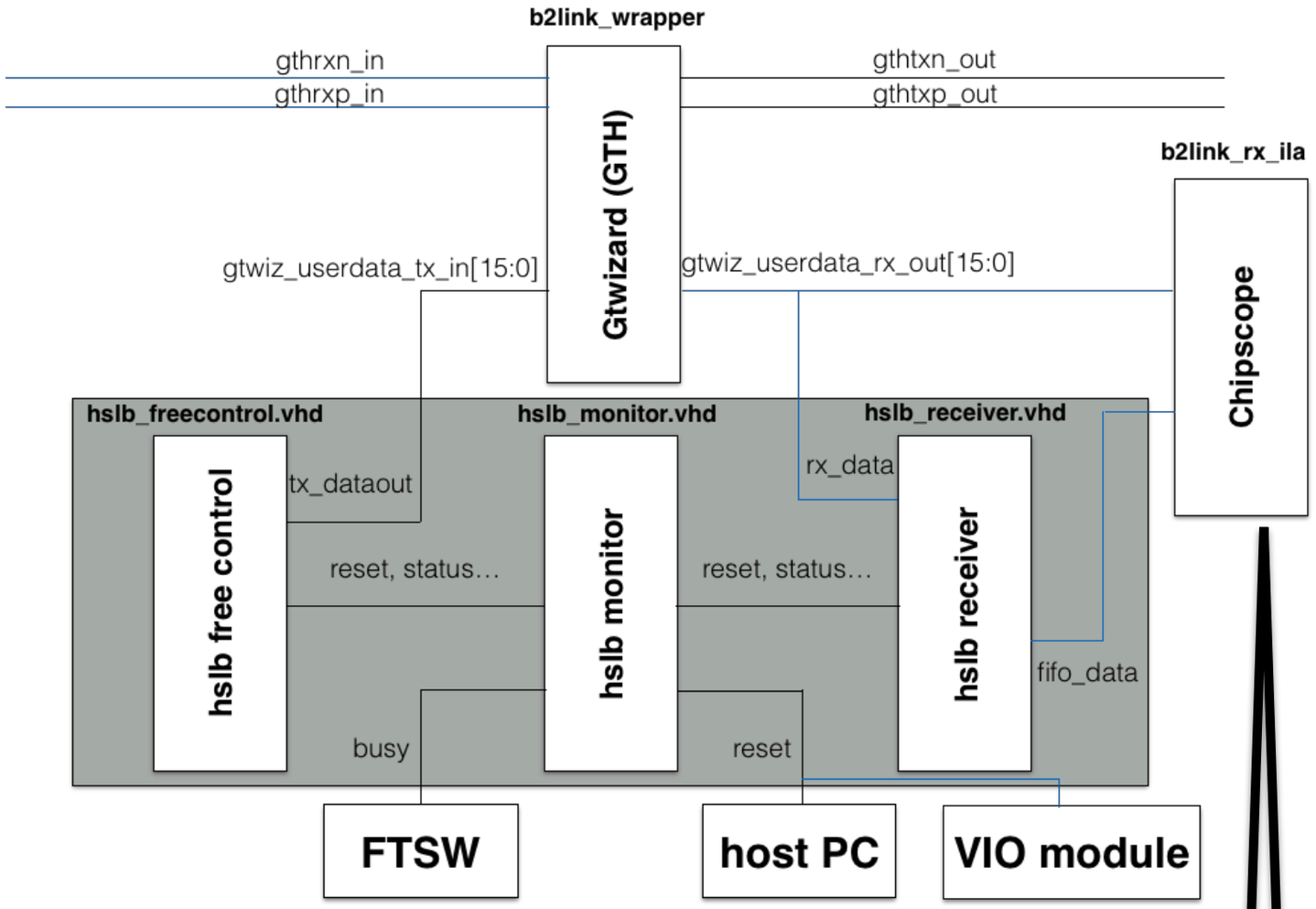
Functions require firmware development

	Belle2link (data)	Belle2link (SLC)	B2tt (include busy handshake)	User logic (event building)	Interface with PCs (PCIe/ Ethernet)	SLC software
A)b2link data-transfer	○	-	-	-	-	-
B) b2link readout by PC	○	-	-	-	○	-
C) FTSW interface	○	-	○	-	-	-
D) User logic, event-building	○	-	-	○	○	-
E) Slow control	○	○	-	-	○	○

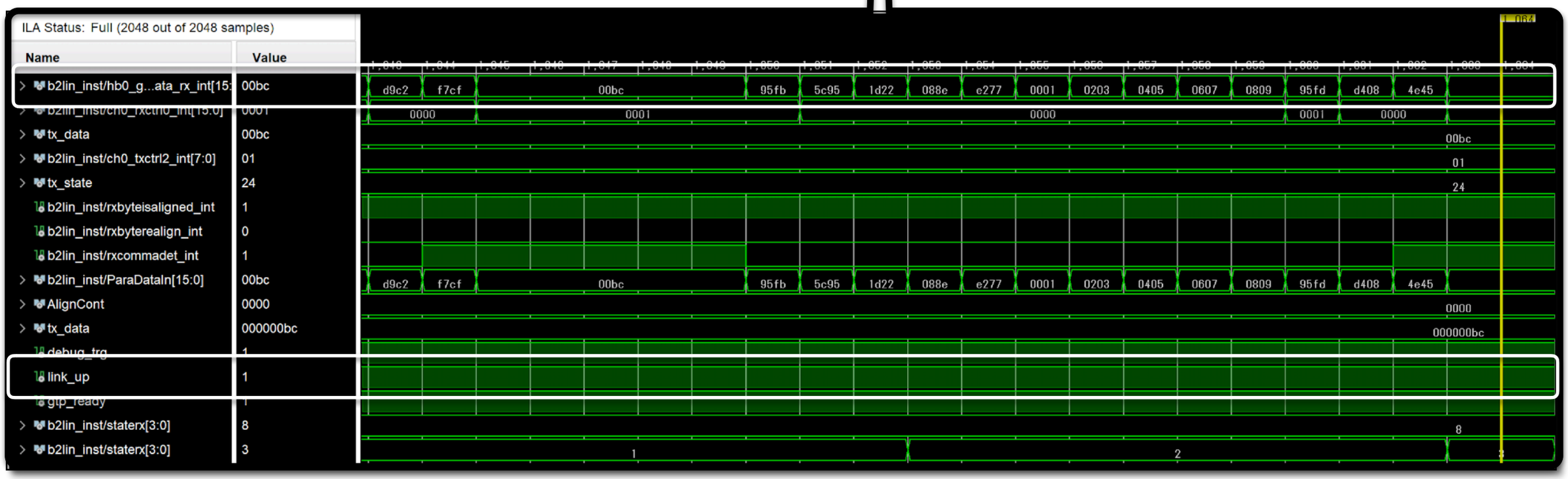
Belle2link establishment



b2l establishment and data transfer



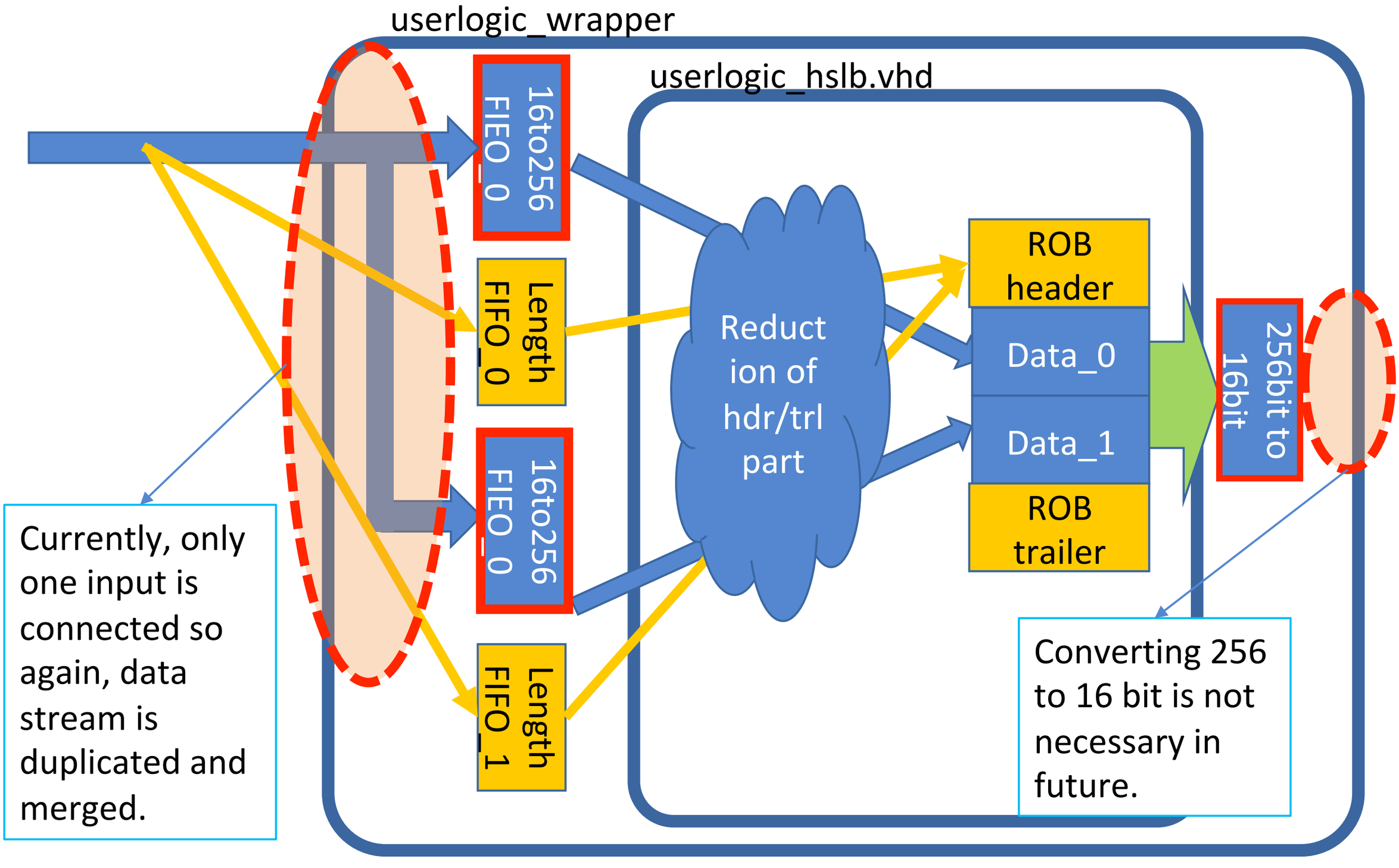
- Full b2l functions has been implemented.
- Tested performed based on FELIX (Kintex UntraScale) and dummy FEE (HSLB).
- Test was first done at KEK test bench, then confirmed at BNL and Pittsburgh



User-logic (formatting, event-building)

Basically, the tested part in HSLB is just implemented to PCIe40 FPGA.

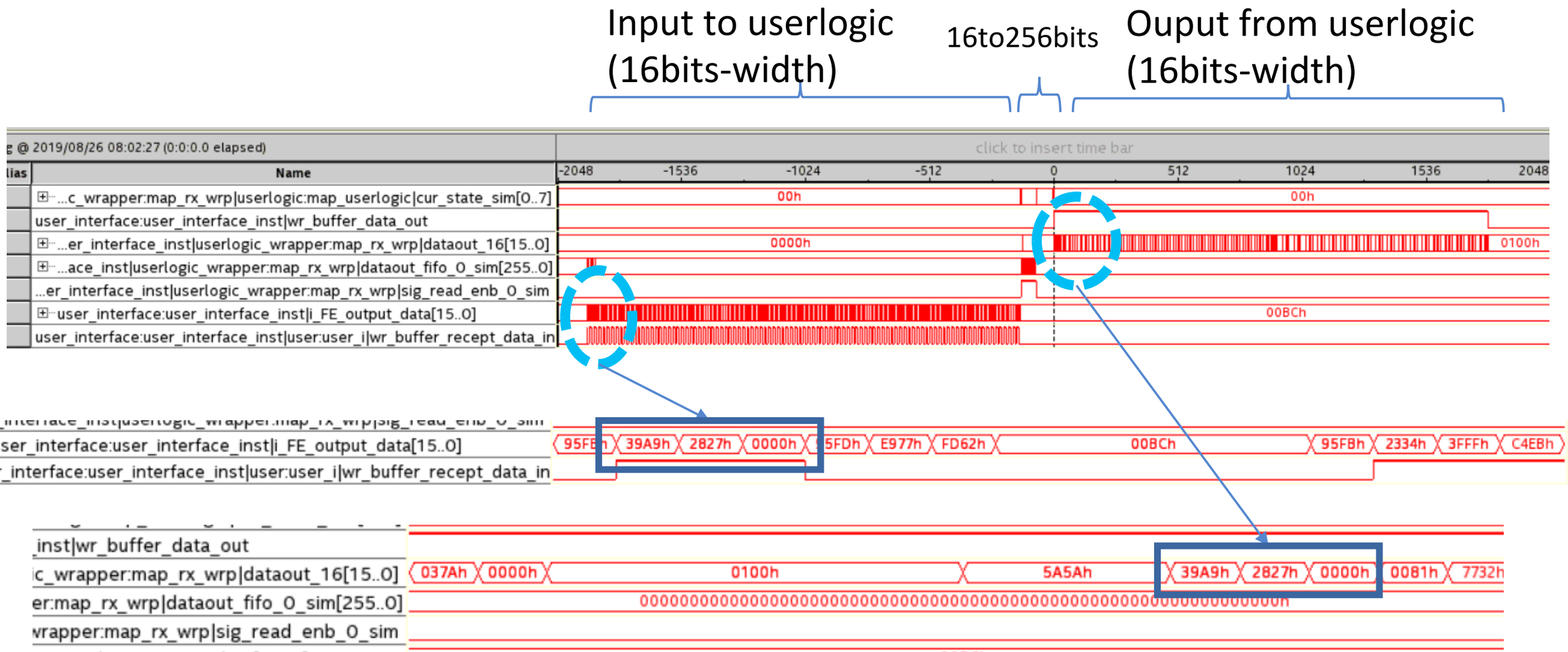
S. Yamada



Functionality confirmed by Signal Tap

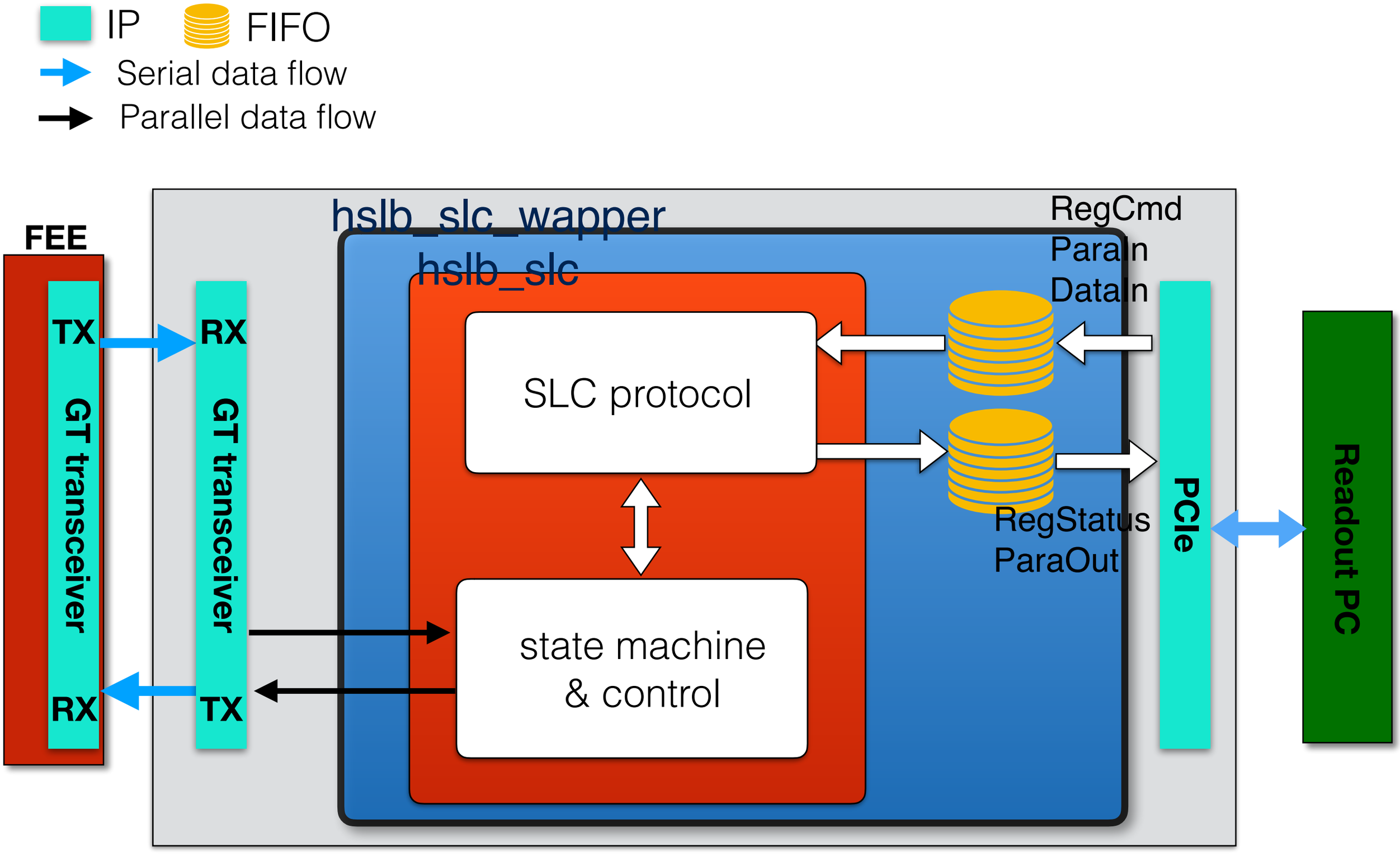
S. Yamada

- Currently, data are checked by signal tap.
  - More detailed check will be done by read out software.
- Test of 24/48 inputs also should be done for high-rate test.
- This part can be used also by FELIX or CPPF, if needed.

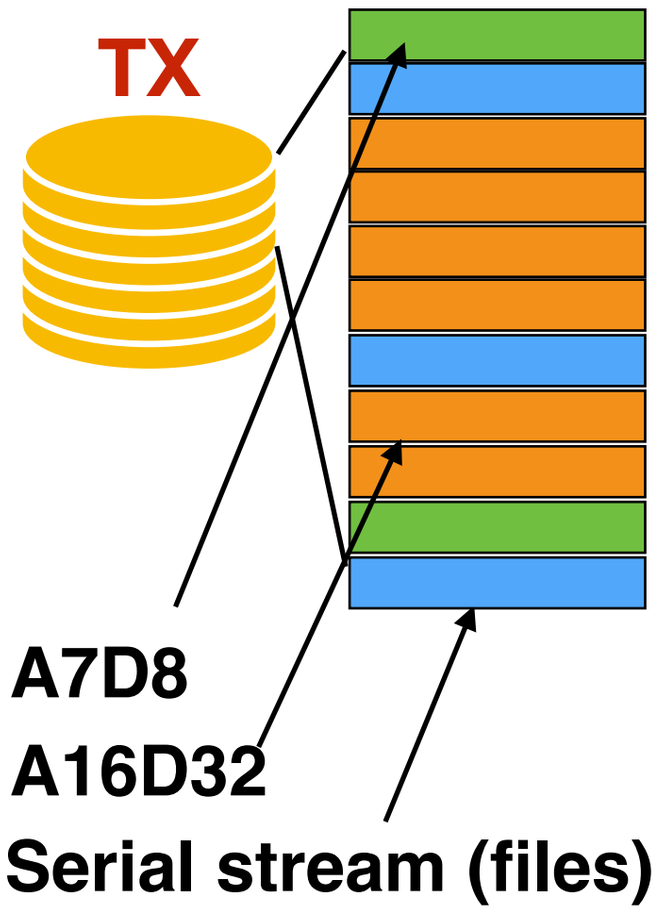


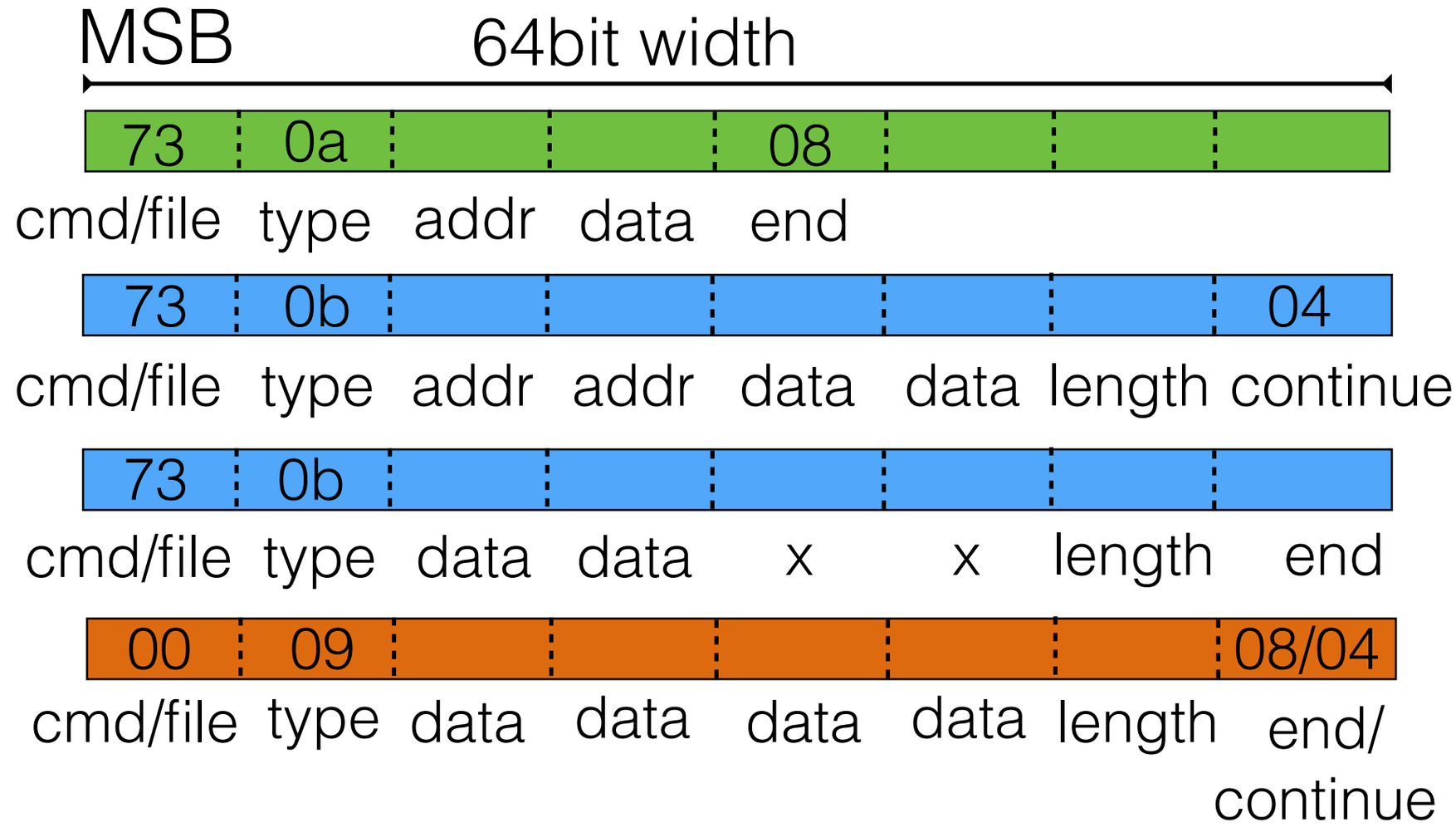
Still needs more detailed check.

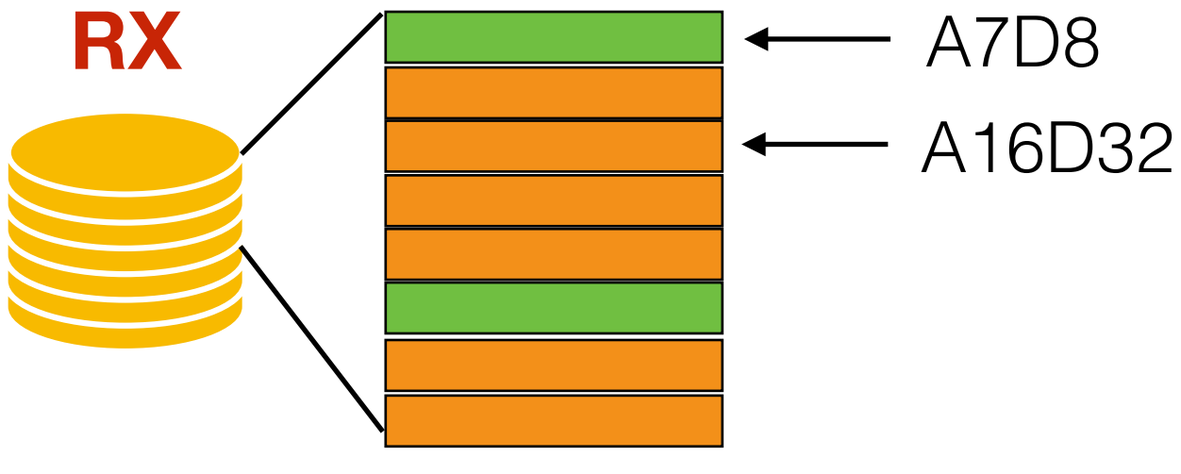
SLC interface

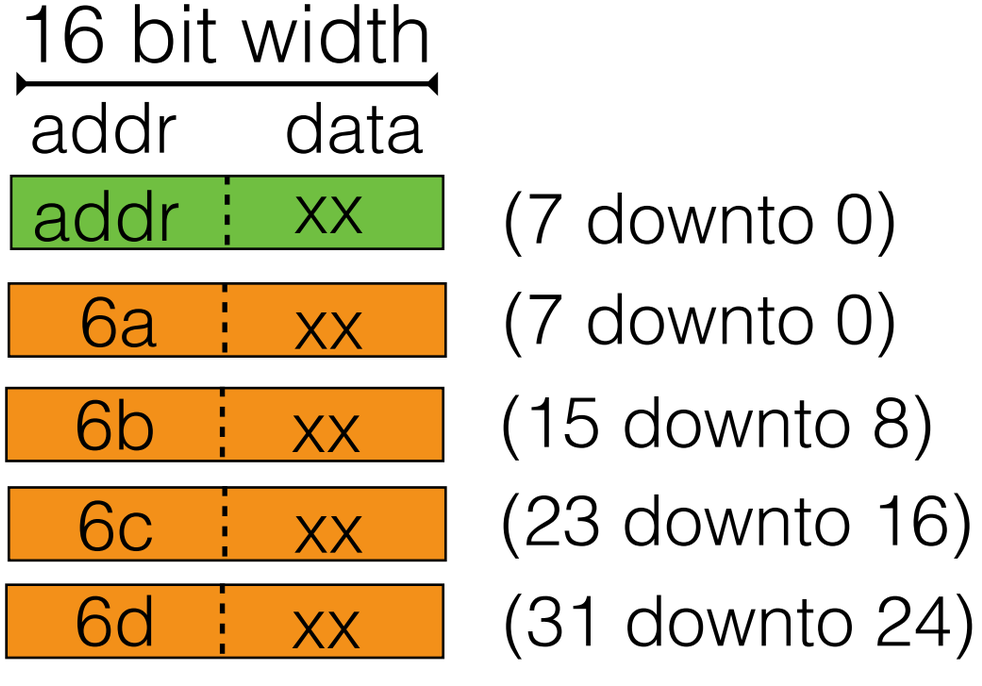


SLC FIFO data structure

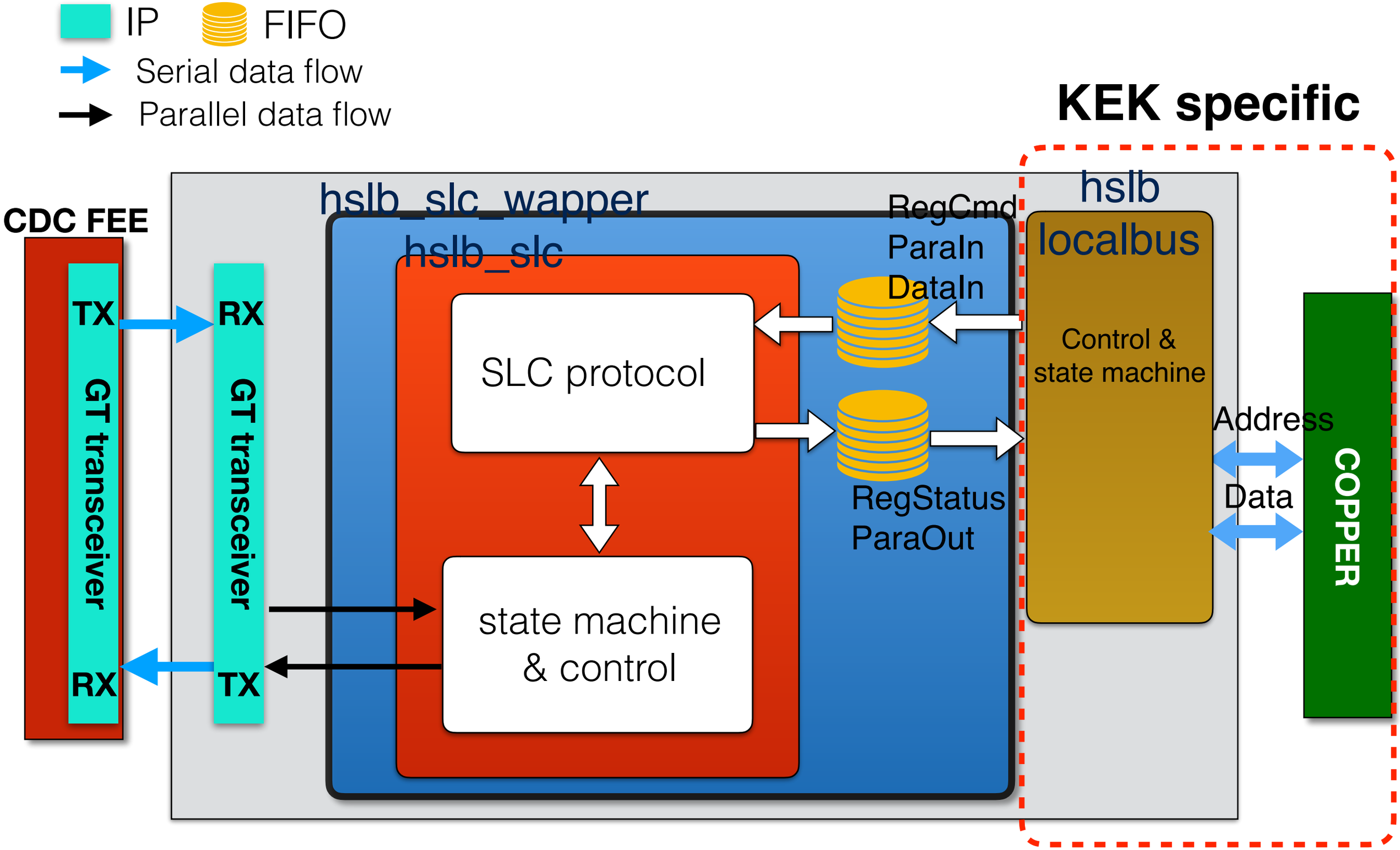




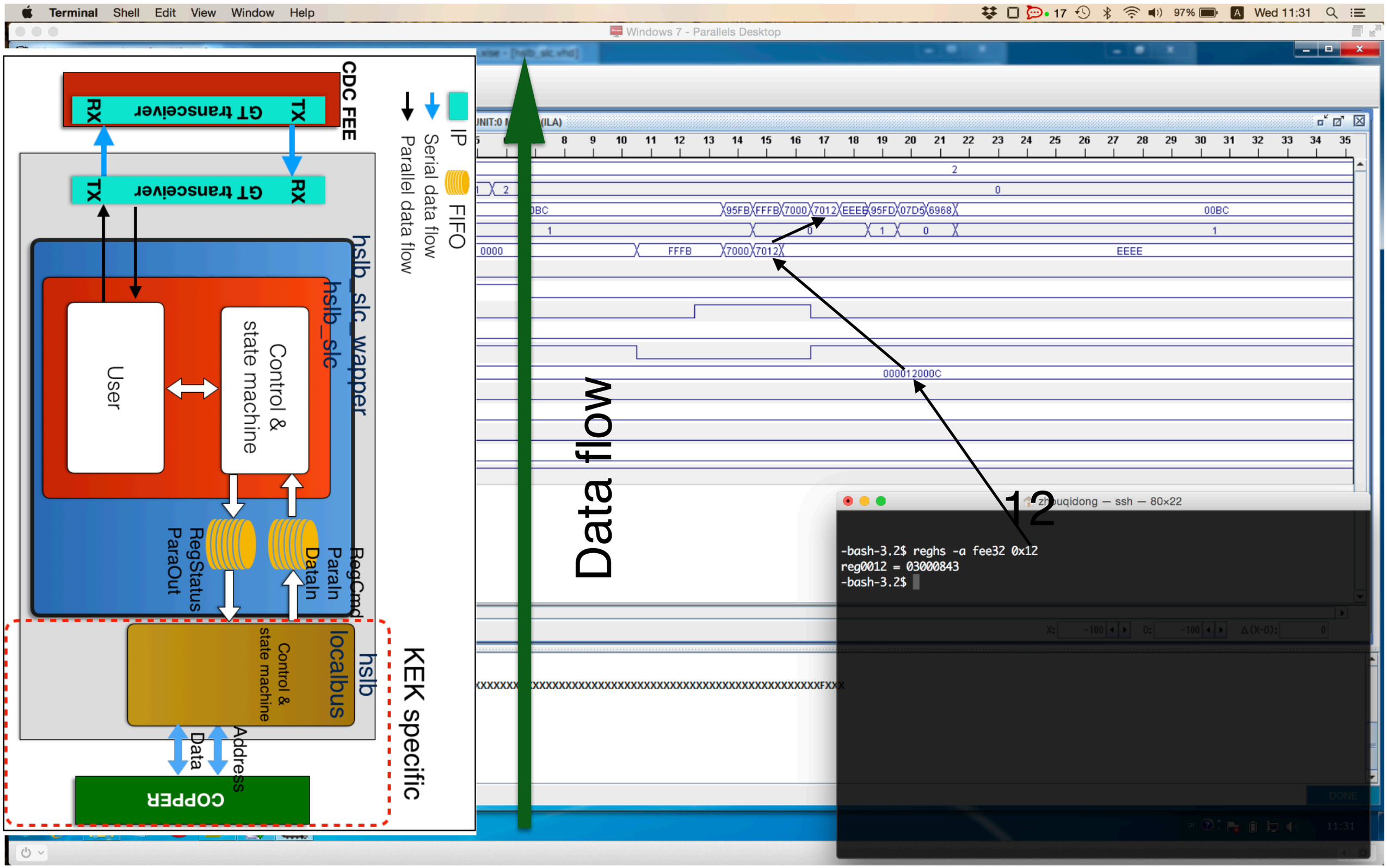




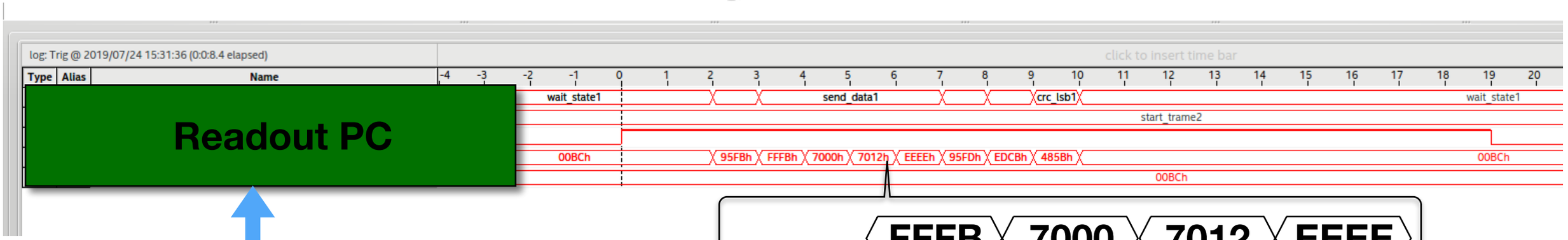
Test bench for SLC w/ COPPER

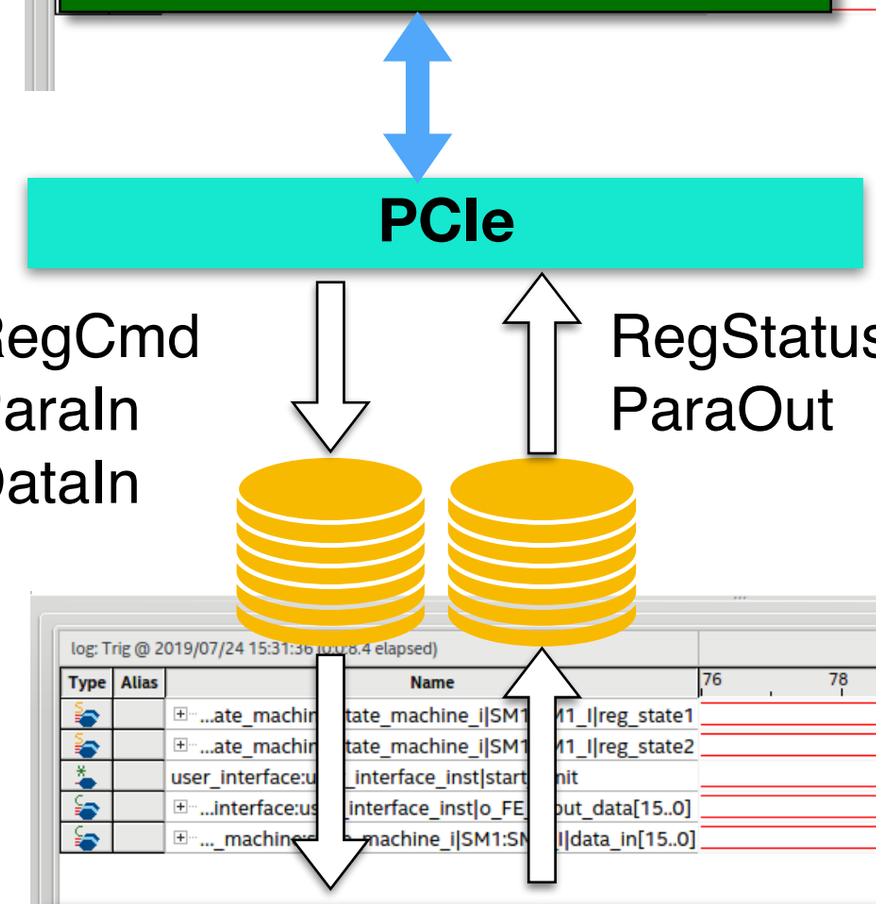


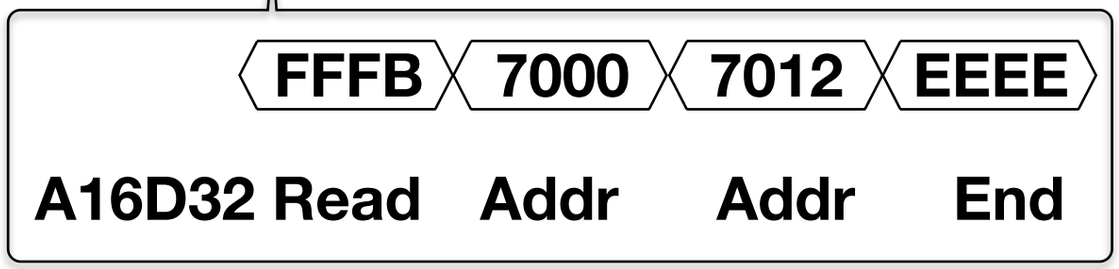
Test the functionality based on COPPER



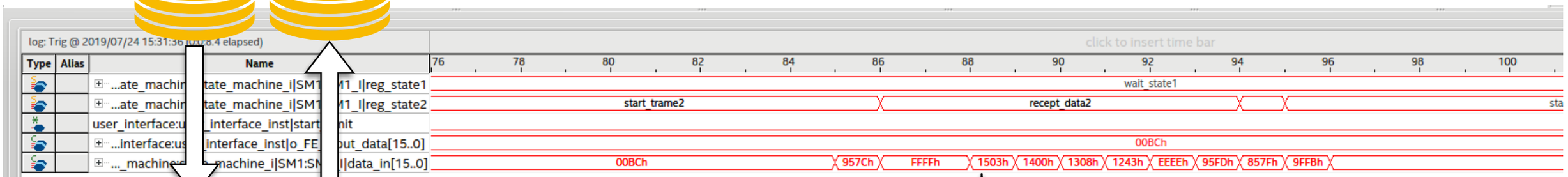
SLC functionality test with PCIe40

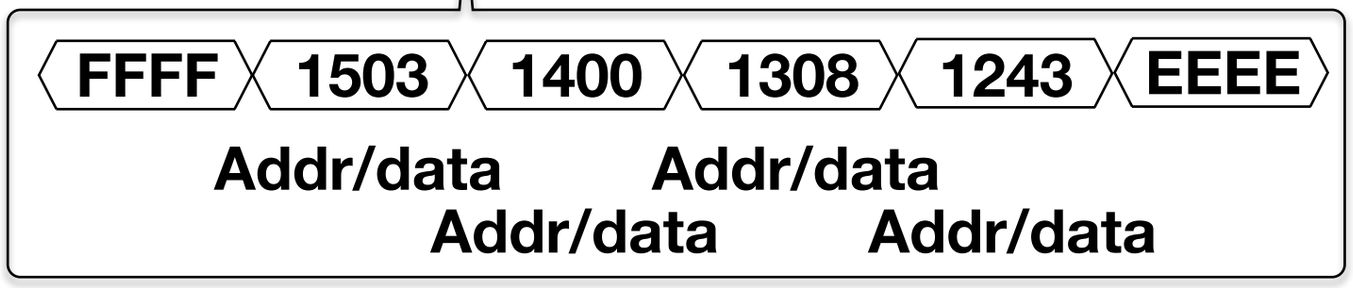






Access the register with address 0x0012 of FEE





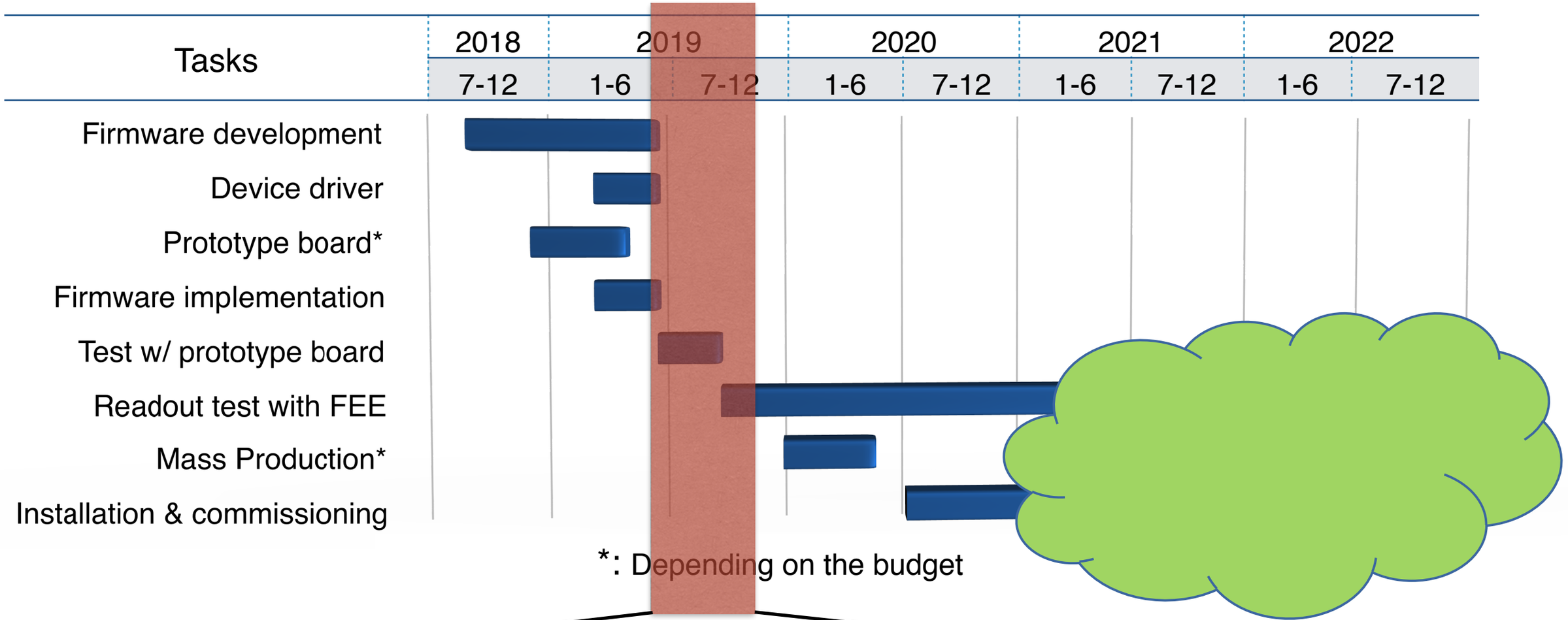
Return the data of 0x03000843 from register address 0x0012 of FEE

Summary

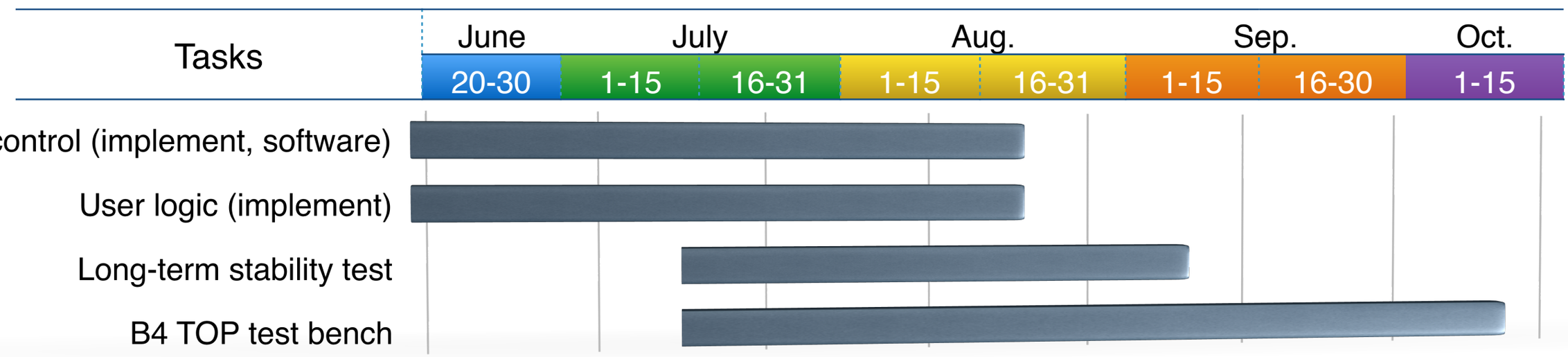
- Functions of belle2link, FTSW interface, pre event building and slow control need firmware development for Belle II DAQ upgrade.
- Full b2l function was implemented for all three proposals. For the FELIX (GTH, Kintex Ultrascale) b2l was tested at KEK, BNL and Pittsburgh.
- User logic (pre event building) and slow control were ready for all three projects. Currently, they were implemented to PCIe40, and PCIe40 already get full functions could be tested with current Belle II DAQ system.

Backup

Schedule & Prospects



*: Depending on the budget



Readout test with HSLB

HSLB(dummy data source) -> HSLB(duplicate event -> merged) -> COPPER

Red: header of readout board (RawCOPPER header)
BLUE: header of each link
GREEN : padding for converting to 256bits-width

Read data: 480 : LEF_FF = 1

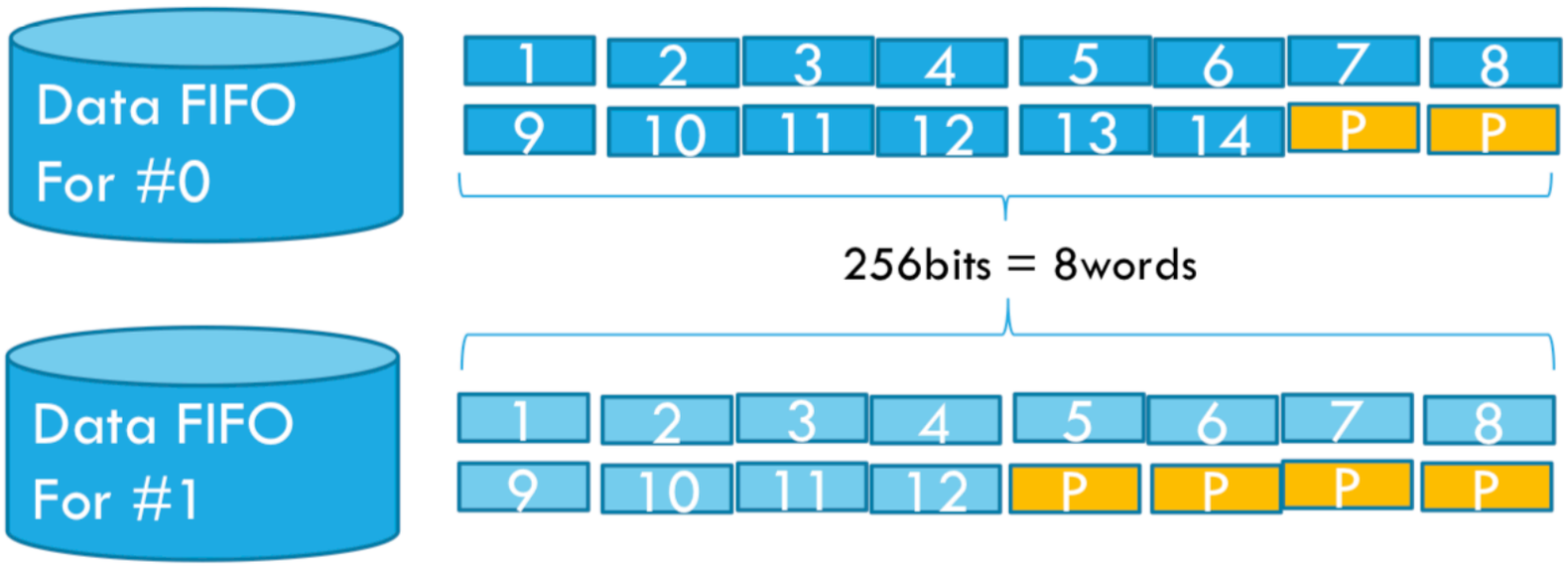
00000000 7fff0008 00000002 00000000 00000000 00000000 00000000 00000000 ffffafa 0000006f 00000068
00000010 00000000 00000000 00000000 00000064 7f7f0001 00009900 00000002 20676f37 5d065822 1a160050
00000020 1a170050 00000032 ffaa0002 20676f70 00000002 5d065822 20676f37 00010203 04050607 08090a0b
00000030 0c0d0e0f 10111213 14151617 18191a1b 1c1d1e1f 20212223 24252627 28292a2b 2c2d2e2f 30313233
00000040 34353637 38393a3b 3c3d3e3f 40414243 44454647 48494a4b 4c4d4e4f 50515253 54555657 58595a5b
00000050 5c5d5e5f 60616263 64656667 68696a6b 6c6d6e6f 70717273 74757677 78797a7b 7c7d7e7f 80818283
00000060 84858687 88898a8b 8c8d8e8f 90959697 98999a00 20676f37 00028317 ff550032 00000032 ffaa0002
00000070 20676f70 00000002 5d065822 20676f37 00010203 04050607 08090a0b 0c0d0e0f 10111213 14151617
00000080 18191a1b 1c1d1e1f 20212223 24252627 28292a2b 2c2d2e2f 30313233 34353637 38393a3b 3c3d3e3f
00000090 40414243 44454647 48494a4b 4c4d4e4f 50515253 54555657 58595a5b 5c5d5e5f 60616263 64656667
00000100 68696a6b 6c6d6e6f 70717273 74757677 78797a7b 7c7d7e7f 80818283 84858687 88898a8b 8c8d8e8f
00000110 90959697 98999a00 20676f37 00028317 ff550032 18181818 18181818 fffff5f5 7de0a170 7fff0009

- Todo
  - Implement to New ROB firmware. (Currently, try to implement it in PCIe40)
  - Functionality of data-checking

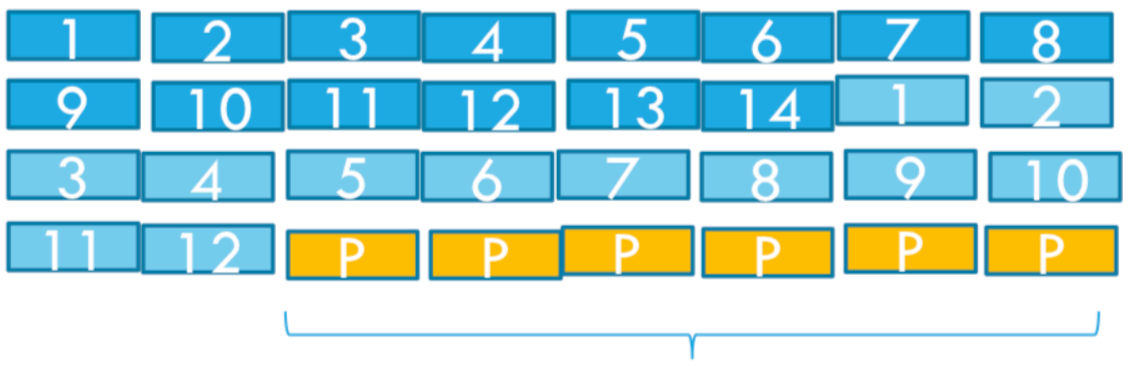
PADDING

- Belle2link event-data from FEE has the minimum unit of 32bits = 1word
- The output width should be larger for high throughput.

e.g. if 14word/event for link #0 and 12 word for link #1



Output data(not considering data-reduction/hdr/trl here)



This part needs to be removed downstream. (driver, software or?)

TX FIFO data structure

MSB — 64bit width

A7D8 write	73	07			08			
	cmd/file	type	addr	data	end			
A7D8 read	73	0a			08			
	cmd/file	type	addr	x	end			
A16D32 write	73	0b						04
	cmd/file	type	addr	addr	data	data	length	continue
	73	0b						08
	cmd/file	type	data	data	x	x	length	end
A16D32 read	73	0c						04
	cmd/file	type	addr	addr	data	data	length	continue
	73	0c						08
	cmd/file	type	data	data	x	x	length	end
Serial stream (files)	00	09						08/04
	cmd/file	type	data	data	data	data	length	end/ continue