DAQ Upgrade Committee Report at the 2019 Trg-DAQ WS

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- W. Kuehn (Giessen)
- Z. Liu (IHEP)
- G. Varner, K. Nishimura (Hawaii)
- S. Yamada (KEK)
- R. Itoh (Ex-officio : Belle II DAQ group leader)
- P. Krizan (Ex-officio : Belle II Technical coordinator)

Gary Varner [Chair] for the Committee August 28, 2019

## Streamlined Synopsis

- Since many of the updates already presented supersede information in my slides, they and history are relegated to back-up
- Brief update on the end-game

### At last B2GM

- 1. Unfortunately the KEK-BNL US-Japan/日米 proposal was not funded. After discussion, an effort will continue, led by U. Pittsburgh on demonstrating FELIX as a viable back-up. (however funding would be needed to follow-through on this option)
- 2. The PCIe40 effort announced that piggy-backing on the CERN production run would benefit from a decision earlier than October. October could work, if MoU process causes no further delays
- 3. IHEP reports CPPF funding for half of the production has been secured, with good prospects for remainder on timeline of decision/MoU

### **Committee Action**

- In response to request relayed by the committee, on behalf of the PCIe40 effort, the EB and senior management agreed to establish an MoU template
- Yamada-san and I drafted such and received significant feedback from the senior management
- The MoU template was released August 1, with a number of important resource items to be confirmed therein
- This MoU is to be acted upon immediately after decision by the Belle II leadership, which follows receipt of the DAQ Upgrade committee report
- We encourage proponents to initiate any negotiations in a timely manner (updates provided) <sup>4</sup>

## MoU: Replacement timescale

• The schedule would ideally align with long summer shut-down (PXD L2, TOP MCP-PMT replacement)

Year	2018	2018	2018- 2020	2020	2020	2021	2021	2022	2022	2023
Month	Jul.16	Oct.31	Apr/18 Mar/20	Apr.	July- Sep.	Jan.	July- Sep.	Jan.	July- Sep.	Jan.
	Proposal deadline	Decision	<b>→</b>							
Proto typing					Could be on budge	shorten tary situ	ed depend ation and	ling		
Mass Produc-					Integratio	n resullt	S			
tion										
COPPER- replacem					repl. 1	spare	repl. 2	spare	repl. 3	spare
ent										
Comment		Multipe candi- dates may be chosen?	test with pocket DAQ	-	COPPER summer s Short win work.	s are rep shutdowr ter shutc	placed det n period in lown migh	ector by 2020, 2 t be utili	detector o 2021, and 2 ized for add	luring 2022. ditional
				•	Implies	s requir	ement fo	or conc	urrent op	eratior

### Summary

- There are 3 compelling options for a DAQ Upgrade, though the FELIX is now firmly a back-up
  - 1. CPPF [IHEP]
  - 2. FELIX [BNL]
  - 3. PCIe40 [LAL]
  - In October, the committee stands ready to provide technical assessment of the final results, as well as comments on whether levels of sustained support and spares in the Production MoUs are reasonable
- In order to avoid production delays, a draft MoU template has been made available and hopefully completed in advance of a final technical assessment

### Backup



# Expressions of Intent

Group	Heritage	FPGA Basis	Experiments	Status	Comment
BNL	FELIX	Ultrascale (Xilinx)	ATLAS, etc.	Prototype+	Large ANL/BNL FW
IHEP	xFP/CPPF	Virtex/Kintex (Xilinx)	Belle II/CMS	prototype	Belle2link experience
KEK	Aurora2PCIe	Ultrascale (Xilinx)	DEPFET (not PXD)	concept	Same company UT- 4
LAL	PCIe40	Intel Arria 10 (Altera)	LHCb	Prototype+	Large LAL/CPPM FW
TUM	PXD		Belle II		Withdrawn

- To first order all HW solutions look to be in the few 10's M円, 100's k\$/Euro
- FW development effort largest differentiator/uncertainty
- Clearly none of proposals will have full vetting by October 2018
- Prototype tests on CDC proto, TOP Module01

# Brief reminder: DAQ Upgrade history

- Adiabatic transition of COPPER-based backend roughly a decade old → needs replacement
- **Reminder:** originally to provide a recommendation to the Belle II Management by October, 2018
- Initial interest by a number of groups, committee formed and given charge to review proposals
- In order to provide meaningful comparison of the proposals
  - Posted System Specifications
  - Call for proposals that should address these requirements
  - Comparison to be based upon these criteria, including the development time, manpower, distributed effort (in particular for Firmware)

## Requirements

- After multiple iterations within the committee, decided to release along with a Call for Proposal
- Anticipated there may be poorly specified items → get questions/feedback during the proposal period

$\leftarrow$ $\rightarrow$ C $\triangleq$ Secure   https://confluence.d	lesy.de/display/BI/Requirements+Document+for+DAQ+upgrade
≡ XConfluence Spaces - Peo	ple Create ···· Q · 🕰 🔍 ·
Emergency shutdown of DAC	Pages / / Upgrade of the Belle II Readout Subsystem 🔒 🕘 🥒 🖉 Edit 😤 Save <u>f</u> or later 🐵 Watch 🖆 Share 🚥
Pre DAQ-expert shift	Requirements Document for DAO upgrade
Readout PCs	Satoru Yamada posted on 07. Feb. 2018 03:39h - last edited by Satoru Yamada on 12. May. 2018 06:59h
Recovery of DAQ in E-hut fro	
✓ Upgrade of the Belle II Reado	Requirements Matrix Document     The latest version
<ul> <li>Requirements Document</li> </ul>	Older versions
> Detector BelleIISchedule	Overview of the current Belle II readout system     Event size estimation from each sub-detector
> Detector BelleIIWeeklyReport	Belle2link
> Detector Material	Overview     Eirmware code
Detector Radiation	
> ECL WebHome	
IR WebHome	Requirements Matrix Document
KLM WebHome	·
> LABM WebHome	The latest version
> MDI WebHome	• v0.9 (2018.5.12) : Add new sections about firmware development and event-size, remove logistics and quality tables.
> PXD WebHome	
> Slow Control	Older versions
> SVD WebHome	• v0.1 (2018.3.14)
> TOP WebHome	<ul> <li>v0.2 (2018.3.15) : Add block diagrams of COPPER and readout PC in Appendix A-C.</li> <li>v0.3 (2018.3.26) : Add description of TTD interface (Appendix, D)</li> </ul>
٠	• v0.4 (2018.4.12) : Add description of slow control interface (Appendix. E)
🔅 Space tools 🗸 🛛 «	<ul> <li>v0.5 (2018.4.24): Add comments about number of input channels from the viewpoint of the implementation of the TTD interface.</li> <li>v0.6 (2018.5.03): Add a matrix about resources</li> </ul>

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# Key Functionality



• Naturally focus is on item 1, but a long-term successful system should spread the development, integration and maintenance broadly across the collaboration

### Replacement timescale

• In the course of discussion and evaluation it became vital to clarify the timescale that is being considered

Year	2018	2018	2018- 2020	2020	2020	2021	2021	2022	2022	2023
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	Proposal deadline	Decision								
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tion										
COPPER- replacem					repl. 1	spare	repl. 2	spare	repl. 3	spare
ent										
Comment		Multipe candi- dates may be chosen?	test with pocket DAQ		COPPER summer s Short win work.	s are rep shutdown ter shutc	placed det n period in down migh	ector by 2020, 2 t be util	detector d 2021, and 2 ized for add	luring 2022. ditional
				•	Implies	s requir	ement fo	or conc	urrent op	eratior

## Subsequent DAQ Upgrade process

- As a reminder: agreement was reached to proceed in 2 phases (post initial proposals)
- **R&D LoIs:** were provided, and concisely summarized in spreadsheet form after the Feb B2GM
  - Provided in the backup slides
  - Committee reviewed and iterated to ensure uniformity
- **Production MoU: provide a final recommendation to the Belle II Management by October 2019 B2GM**
- Since full proposals had already been received, and were considered of sufficiently high technical merit, point of this R&D LoI was to clarify what will be demonstrated by October

### **R&D** Coordination Phase

- 3 proposals advanced to the R&D Phase
  - 1. CPPF [IHEP]
  - 2. FELIX [BNL]
  - 3. PCIe40 [LAL]
- All 3 have significant heritage in current LHC experiments (and other) DAQ upgrades [backup]
- Since early spring regular DAQ upgrade meetings are being held of the DAQ Upgrade group and details on progress and issues reported
- Progress tracking in Redmine
- Very good preliminary steps toward integrating any of these efforts once a downselect is made

# DAQ Upgrade Group



# DAQ Upgrade Activities

- Bi-weekly meeting
  - BNL/Pittsburgh: JST 8:00, EST 18:00 (Thursday)
  - LAL/IHEP : JST 17:00, CET 9:00 (Thursday)
- Redmine: management of schedule, tasks and milestones <u>https://b3ropc01.kek.jp/redmine/projects/belle-ii-daq-upgrade/issues/gantt</u>
- Rocket Chat to proceed the test.



### Milestones by Oct. 2019 B2GM

- A) Test of B2link operation and data transfer with FEE (or HSLB)
- B) Test of b2link data-readout by PC Server (via PCIe or Ethernet)
- C) Test of FTSW interface ( including BUSY handshake )
- **D)** Test of readout with user logic and event-building
- **E) Test of Slow control with FEE**
- F) Performance benchmarking (stress-test links) and longterm stability test
- G) Readout test with full functionality of spare TOP module in Tsukuba B4

These are the technical achievements upon which committee will assess readiness

### TOP B4 Test bench

- Hawaii has hired a dedicated DAQ upgrade postdoc, but awaiting visa, learning curve
- Interim Contact: Martin Bessner



### • PCIe40 production:

- CERN is managing the contract for the current large production of PCIe40 boards (1250 boards in total):
  - This production will be finished by November 2019
  - The CERN contract foresees a last batch of production end of 2019: to be part of this last batch, we must tell CERN in October
  - If we cannot be part of this last batch, we would have to renegociate a contract to produce the board, since we have only 20 boards to produce, the prices for the production will be very high (probably factor 2 higher)
- Production (=board assembly) is not the only step to have the board but we have to produce the PCBs, order and prepare the components, use the test bench at the company, ... All of these have a fixed cost, so it is better to have these steps done together with the current big production for LHCb+ALICE or immediately after. These steps are progressively finished for the big LHCb+ALICE production, so starting from now, the longer we wait, the larger number of steps would have to be redone only for Belle 2. For example, PCB production for LHCb+ALICE is finished. The longer we wait to restart the PCB production for Belle 2, the higher the price. For PCB only, if we wait until October to start reproducing it, the total PCIe40 board price would be 10% higher.

# User-logic (formatting, event-building)



# CMS heritage

### **CPPF** upgrade

- XC7VX415T upgrade to XC7V690T
- Added one TX MiniPoD,
- Total: 36 channel input, 36 channel output,
- Added 156.25MHz OSC for 10GbE,
- Added FTSW RJ45 Port,
- PCB layout is finished, and ready for submitting to PCB factory.







### **Current testing with existing CPPF board**

## CPPF test bench [IHEP]

### Demo system Setup at IHEP

• Photo of Full Demo System





CPPF and PC in working



2019-6-17

33th B2GM

#### CPPF and Interface to FSTW/PC

### **Architectural distinction: 10GbE network collection**

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### **CPPF project status and tentative plan**

	2019-4	2019-5	2019-6	2019-7	2019-8	2019-9	2 <b>019</b> -10	2019-11	20
Development #104: CPPF project						, ,	New 43%		
Support #145: Submit proposal	Completed	100%							
🧓 <del>Test #129</del> : A) Test of B2link establishment and data transfer with FEE (or HSLB)	Completed	100%							
Test #132: B) Test of b2link data-readout(todo : 10GbE)				date	TBD 70%				
🤜 Test #135: D) Test of readout with user logic and event-building						date TBD 3	80%		
Test=#144: C) Test of FTSW interface ( including BUSY handshake )		Completed	100%						
Test #138: E) Test of Slow control with FEE (todo: communicate between FW and PC)						date TBD 3	80%		
🧊 Test #141: F) performance (full input links) and long-term stability test				date TBD 0	%				
Support #160: (IHEP) Provide a CPPF board to KEK ?				New	0%				
Test #161: (KEK) Build a setup and perform a test at KEK						New 0%			
🗾 Test #117: readout test with Tsukuba B4 setup (IHEP)							date TBD 0	%	



Test with B4 TOP test bench

### FELIX



Figure 2: Left: TTD mezzanine for Belle II timing interface. Right: BNL-712 FELIX I/O card with timing mezzanine mounted on the top left corner.

#### **ATLAS Upgrade heritage**

**Custom card to interface to Belle II FTSW system** 

### FELIX Test Bench at KEK









### FELIX project status and tentative plan

	2019-4	2019-5	2019-6	2019-7	20	19-8	2019-9	20	19-10	2019-11	
🐻 Support #126: 19Oct B2GM					Г					lew 0%	
Development #102: FELIX project										Nev	v 52%
🐻 Support #114: BNL visit	Ended 100	%									
🗾 Support #119: Install FELIX board in b3ropc03	Completed	100%									
园 Support #148: (KEK) delivery date of a MPO24 cable for the KEK FELIX test bench	Completed	100%									
Development #152: (BNL+KEK) Provide proper FELIX projects to start with	Completed	100%									
Bevelopment #158: (KEK) implement TX part(hslb_feecontro.vhd etc) of belleZlink in FELIX	Completed	100%									
Development #153: (KEK+BNL) Implement the skelton user-logic in FELIX firmware	New 0%										
Development #163: A') B2link establishment and data transfer (GTH wizard)	Compl	eted 100%									
😹 Test #149: (BNL+KEK) Belle2link establishment betwen FELIX and HSLB at KEK and BNL	Completed	100%									
🐻 Test #127: A) Test of B2link (todo : implementation in FELIX firmware)				In Pr	ogres	s 80%					
🐻 Test #133: D) Test of readout with user logic and event-building					dat	e TBD 0	%				
Test #136: E) Test of Slow control with FEE				$\rightarrow$		date	TBD 0%				
Test #142: C) Test of FTSW interface ( including BUSY handshake )							date	тв	0%		
🗾 Test #130: B) Test of b2link data-readout by PC Server (via PCIe or Ethernet)							date	тв	0%		
😡 Test #115: readout test with Tsukuba B4 setup (BNL)								da	te TBD 0	%	
😡 Test #139: F) performance (full input links) and long-term stability test										dat	e TBD



Test with B4 TOP test bench

#### Initially great progress, somewhat slowed

### PCIe40 [LHCb and ALICE]



### **Core FPGA is Altera (Belle II is otherwise mostly Xilinx)**

### PCIe40 Test Bench at KEK



### PCIe40 project status and tentative plan

	2019-4	2019-5	2019-6	2019-7	2019-8	2019-9	2019-10	2019-11	20
🔜 Development #103: PCIe40 project							, Ne	ew 81%	
Support #121: Run Quartus at KEK	Completed	100%							
Support #111: Quartus, PCIe40 installation at B3	Completed	100%							
🧓 Development #155: (LAL) b2link establishment beteen PCIe40 and CDC FEE at LAL	Completed	100%							
🐻 Fost #156: (KEK) belle2link establishment between CDC FEE and PCIe40 at Tsukuba B3	Completed	100%							
😡 Development #157: (LAL+KEK) Discuss and provide PCIe interface in FPGA	Completed	100%							
🧾 Development #159: (KEK) implement a missing part(hslb_feecontro.vhd ? hslb_monitor.vhd ? e	Terminate	d 0%							
🐻 Test #128: A) Test of B2link establishment and data transfer with FEE (or HSLB)	Completed	100%							
Development #158: (KEK+LAL) Implement the skelton user-logic in PCIe40 firmware	Completed	100%							
Test #131: B) Test of b2link data-readout by PC Server (todo: DMA readout)				In Progres	s 90 %				$\square$
🗾 Test #134: D) Test of readout with user logic and event-building				In Progres	s 80 %				
🥃 Test #143: C) Test of FTSW interface ( todo : BUSY connection with userlogic FIFO )				In	Progress 90%				
Test #137: E) Test of Slow control with FEE				date TBD	0%				
📰 Test #116: readout test with Tsukuba B4 setup (LAL)					date TBD (	%			
🛃 Test #140: F) performance (full input links) and long-term stability test							N	ew 0%	



Milestones

Test with B4 TOP test bench

### One version of the Schedule



### Committee response

- October B2GM was announced as the deadline for demonstrating capabilities for technical assessment
  - 1. Key functionalities, including slow control
  - 2. Benchmark performance
  - **3.** Stable operation in high-rate and long-term test
  - 4. Operation and successful data taking with a real detector module (TOP Module 01)
- None has yet fulfilled these requirements
- It is reasonable to expect it can happen for multiple solutions, but not there yet
- An early decision would have to be made on nontechnical grounds (by management)

### • MOU:

- Would have to be signed by all parties before starting the production, given the October strong constraint, it is necessary to draft it now.
- The content from the PCIe40 proposing group side would be similar to the LOI: LAL/IN2P3 provides PCIe40 for the experiment (18 + 2 spares + 3 margin + 3 current boards), assuming the corresponding servers are paid by KEK, fibers, cables, personpower for the firmware and software development and for the installation/commissioning, and support for the operation of the board over the entire time they will be used for Belle 2 DAQ.

#### Summary :

If the decision is taken in October B2GM, and PCIe40 board is selected, it is technically possible to proceed, but MoU shouldn't create a delay that could derail the timeline.

If an earlier (June) decision was made, it would ease considerably the process, reduce prices, and may open the door for a full funding already in 2019 (not 2020).

Delay in providing the MOU for October will cause a large cost increase and delays that should be covered by Belle II.

### Committee response

- We agree negotiation of the MoU should proceed right away, to avoid any unnecessary delays
- The DAQ Upgrade Committee provides technical comments, such as whether scheduling, personnel support, or spares seems adequate, however doesn't negotiate the MoU
- A draft template was provided previously, though should be verified by the management (via the EB?)
- We seek EB guidance on how to proceed

#### Overall, what do you plan to demonstrate by the October deadline? [specific test hardware and functionality]

ltem	Estimate	Basis of Estimate/supporting comments
BNL	FELIX functionality with CDC, ECL and KLM	Established contact with maintainers/owners of CDC (R.Itoh,S.Yamada), ECL (V.Zhulanov), TRG(T.Koga) and KLM (K.Nishimura, G.Varner) test stands. Participation in the R&D phase is predicated on individuals and institutions successfully completing their obligations for Phase 3 running.
LAL	<ul> <li>* Readout of FEE via Belle2links</li> <li>* Transfer of data to PC</li> <li>* Connection to FTSW (busy signal)</li> <li>* Configuration of FEE (Slow control)</li> </ul>	Hardware has been tested, only firmware development needed. First prototypes of Belle2links and FTSW links exist. Development of data transfer to PC (via DMA) started.
IHEP	Full Readout based on CMS CPPF, replacing present HSLB+COPPER, with interfacing to FTWS and readout PC after original COPPER/VME crate. Simple CDC slow control implemetation as example, fit also to other systems.	Good under standing and experience of the system. Good R&D progress achieved already as scheduled in the beginning with a full function of a COPPER/HSLBs, including the basical SC and BUSY part.

### What manpower is available and what fraction of their time? [specific names/skill sets most useful]

ltem	Estimate	Basis of Estimate/supporting comments
3NL	BNL FELIX engineers Shaochun Tang and Kai Chen (total fraction 0.75). V.Savinov [DAQ/COPPER/FELIX experience with TOP] at Pittsburgh with grad students T.Pang (25%) and A. Malespina (50%) plus an engineer (100%) if US/Japan proposal funded. Grad students needing training: Xiao Han, Yubo Li, Guangyuan Yuan. Wayne State technician Alfredo Gutierrez with DAQ testing and installation experience, fraction up to 0.25. Postdocs needing training: Rama Adak, BNL postdoc.	Engineers from BNL and Pittsburgh full availability and fraction requires success of US/Japan proposal. Student's and postdoc committment and fraction based on thesis advisor and supervisor statements. Management/senior/PoC personnel omitted from 'Estimate' column are Vladimir Zhulanov, Alex Kuzmin, Xiaolong Wang, Satoru Yamada, Ryosuke Itoh, Qidong Zhou, Todd Pedlar, Kurtis Nishimura, Gary Varner, Taichiro Koga.
_AL	<ul> <li>* Daniel CHARLET, LAL, electronics, 50% firmware dev.</li> <li>* Eric PLAIGE, LAL, electronics, 90%, firmware belle2link dev.</li> <li>* Piotr KAPUSTA, INP Krakow, electronics, firmware dev.</li> <li>* Monique TAURIGNA, LAL, 50%, computing, driver dev.</li> <li>* Eric JULES, LAL, 50%, computing, software dev.</li> <li>* Patrick ROBBE, LAL, physicist, 20%, integration</li> </ul>	* Working already now on the project
HEP	Jia TAO(100%): Main person for the implementation. Hanjun KOU(60%): readout via 1G/10G Ethernet implementation with SITCP, B2TT implementation. Pengcheng CAO(30%): Slow Control and control firmware. Jingzhou ZHAO(40%): hardware and firmware. Na WANG(30%): Hardware modification. Wenxuan GONG(30%):testing. Zhen-An LIU(40%): Overall. Two students from Fudan Uni. are also possible(50%).	IHEP/Trigger team has full experties on hardware, firmware,software and system.

Verification with a minimum of one 'at home' test system is required, with rudimentary functionality. Does your group have any 'stretch goals'?

Item	Estimate	Basis of Estimate/supporting comments
BNL	Demonstrated test system at Pittsburgh. We are working on a test system at BNL.	Details of the demonstration at Pittsburgh were provided in the FELIX presentation at the Oct 2018 B2GM. Additional details are being provided in the FELIX presentation at this (Feb 2019) B2GM.
LAL	<ul> <li>* One complete test bench available at LAL.</li> <li>* Visits to other test benches can be organized to demonstrate the system capabilities</li> </ul>	* At LAL: 1 CDC FEB, 1 ARICH merger board, 1 PC server with several PCIe slots and 10 GB ethernet connection, 1 FTSW module
IHEP	Dummy data source have been made for for links so basically a COPPER functionalities will be implememted, more is possible as require later in the discussion. Aiming a Transparent system for easy upgrade. No change requirement to other existing DAQ/FEE parts.	One 'at home' test system is running with all required parts. Present test results meet most of the requirements already if not all of them.

To better facilitate a comparison on a common, working detector system, the proposal is to use TOP Module01 in Tsukuba Hall. Core and TOP DAQ experts will be available to support these efforts, though not available full-time until the summer shut-down. When might your system be ready for such an integration/benchmark test?

ltem	Estimate	Basis of Estimate/supporting comments
BNL	The FELIX system can be ready for integration and benchmark tests with TOP module01 in Tsukuba Hall if analogous hardware to that already used at the TOP test stand in Pittsburgh is available.	Demonstration with the TOP test stand at Pittsburgh.
LAL	* Test bench at KEK with PCIe40 ready in June 2019	<ul> <li>* 1 PCIe40 board installed end of January 2019 at KEK, with prototype versions of belle2link and TTD.</li> <li>* Development of the firmwares will continue in collaboration with KEK team until June 2019.</li> </ul>
IHEP	As required in October or as early as May if requested.	Good progress already and no problem foreseen. Supporting needed at KEK verification: Materials:FTSW and cables. Data source from FEE with fibers. Ethernet cable to readout PC and control PC. LV power supply. Experties supports: FEE(TOP?),FTSW(Nakao-san),DAQ who understand data checking at later stage.

Are any resources, in particular financial, being requested from Belle II during this R&D or later phases? [Assume that Core DAQ and subdetector experts will handle identified DAQ or subdetector interfaces/provide needed documentation]

ltem	Estimate	Basis of Estimate/supporting comments
BNL	We expect that maintenance and operation after upgrade installation will be the responsibility of KEK.	Funds have been requested as part of US Belle II Operations to facilitate installation in 2020-21.
LAL	<ul> <li>* No financial resource requested from Belle II.</li> <li>* 1 PCIe40 board lent to KEK group end of January 2019</li> <li>* ALTERA licences available for developments in 2019</li> </ul>	<ul> <li>* IN2P3 allocated budget of 80 kEuros for R&amp;D and 30 kEuros for travels in 2019 for R&amp;D phase.</li> <li>* LAL management committed that the team will work on the project in 2019.</li> </ul>
IHEP	We have full resources for the R&D including development plus manpower at present, but not for the production yet. If more tests systems are requested, supporting from the collaboration is welcome. Travel support for the KEK evaluatuion would be appreciated but not a must.	We got support from IHEP resource for the R&D, and we made applications with JSPS/Sakura/IHEP funds in 2018 with success in Chinese side but without KEK/Japan side support we failed finally. We will keep applying in 2019.

Estimates for commissioning/integration resources? revised since the proposal was submitted. [specific names/skill sets most useful]

#### Could be

Item	Estimate	Basis of Estimate/supporting comments
BNL	Some or all of the students and postdocs participating in the R&D (listed above) will be available for commissioning/installation. Appropriate BNL FELIX engineering will be available for commissioning and integration.	Expertise and names above in row 5.
LAL	<ul> <li>* Team will provide support for commissioning and integration</li> <li>* Remote support and travel to KEK</li> <li>* Longer stays at KEK (Daniel CHARLET/Patrick ROBBE)</li> </ul>	* Similar experience in the past with development of hardware for LHCb slow control (Daniel CHARLET/Monique TAURIGNA/Patrick ROBBE)
IHEP	Jia TAO for full time if proposal accepted, Jingzhou and Zhen-An as partial time.	Since Belle2link Working Group formed Jingzhou and Zhen- An have been always in supporting with success

#### Estimates for resources long-term commitment? [specific names/skill sets most useful]

Item	Estimate	Basis of Estimate/supporting comments
BNL	A small fraction of BNL FELIX engineer's time may be available after installation to aid operations.	Need for FELIX engineers during operations depends on success of training new experts on the DAQ team. Funds from US Belle II Operations will need to be requested to support FELIX engineers for operations.
LAL	* Same team available for long-term support	<ul> <li>* Members of team have permanent positions</li> <li>* A group from Marseille (where board was built) will apply to Belle II in October</li> </ul>
IHEP	Jingzhou(hardware/firmware)/Xiaolong. Zhen-An partially.	Xiaolong showed his interest. Training is possible for his team. Anyway IHEP trigger team will stay in Belle II.

### KLM Test bench in Hawaii

### • Interim Contact: Richard Peschke





1 Full scint. Module (150 channels) with pre-amps and MPPCs

