READOUT (STATUS AND UPGRADE)

S. Yamada (KEK)

READOUT STATUS

PXD

(I. Koronov, B. Spruck)

PXD Status – Short Overview

- Only ½ of PXD (20/40) modules installed
  - Two broken, damages on others
  - Only half of readout used (only ½ DHH and ½ of ONSEN powered off)
- Mostly stable data taking
  - 5kHz real data, 10kHz DAQ test, 35kHz with dedicated tests
  - Event selection on HLT (and ONSEN!) turned on now (event reduction to ~10%)
  - ROI selection tested in few runs (for half the modules → DHE order)
- Overlapping trigger firmware deployed during phase 3
- Only Belle 2 trigger veto for continuous injections, no gated mode (yet)

Will be tested in September according to Igor-san's talk

Overview of Main Issues

- Long HLT startup time, long buffering and processing times for some events (up to 2 minutes!), challenge for ONSEN buffering → full → trigger busy at each run start
- HLT does not clear buffers and/or worker nodes crash → for some events we never get triggers → still in memory at run stop
- NSM timeout EB/HLT → PXD seen as excluded (seems to be solved)
- "HLT before DHH" ← no data sent anymore from DHH (in most cases)
  - Firmware and/or ASIC issue
- Not all problem come from PXD even if PXD notices an error
- DHH firmware was updated/changed several times
  - PXD Busy and data corrupting happen with some versions
  - Different reasons → fixed with latest versions
- Lost 25% of data because of wrong trigger delay setting in early phase 3
- One optical link (of 80) went dead in June

SVD

(Katsuro)

- **However, we found a couple of problems**
  1. L6.14.2 sensor current increase
  2. SVD COPPER stuck due to large SVD data
  3. FTSW APV trigger veto problem at high trigger rate

2. ->

- Data size limitation in FEE -> to be tested after IBBelle recovery
- HSLB firmware modification should be done for safe .

3. -> The cause was found. Considering a way to keep both data quality and high-rate processing.

We found the problem is related to a latency setting in APV25.

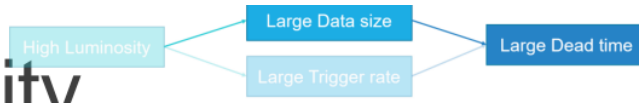
- Thanks for the great efforts of Takuto and Hikaru!
- **By the beg of 2019 spring run:** the latency setting was 4.967usec. (lat=158)
- **During 2019 spring run:** the latency was changed to 4.998usec. (lat=159)
- With lat=158 the error never happens, while with lat=159 the error appears.
  - lat=159 is cutting edge of the APV25 operational range.
  - No degradation seen in the SVD performance unde a few kHz trigger rate

Reminder for possible larger event size

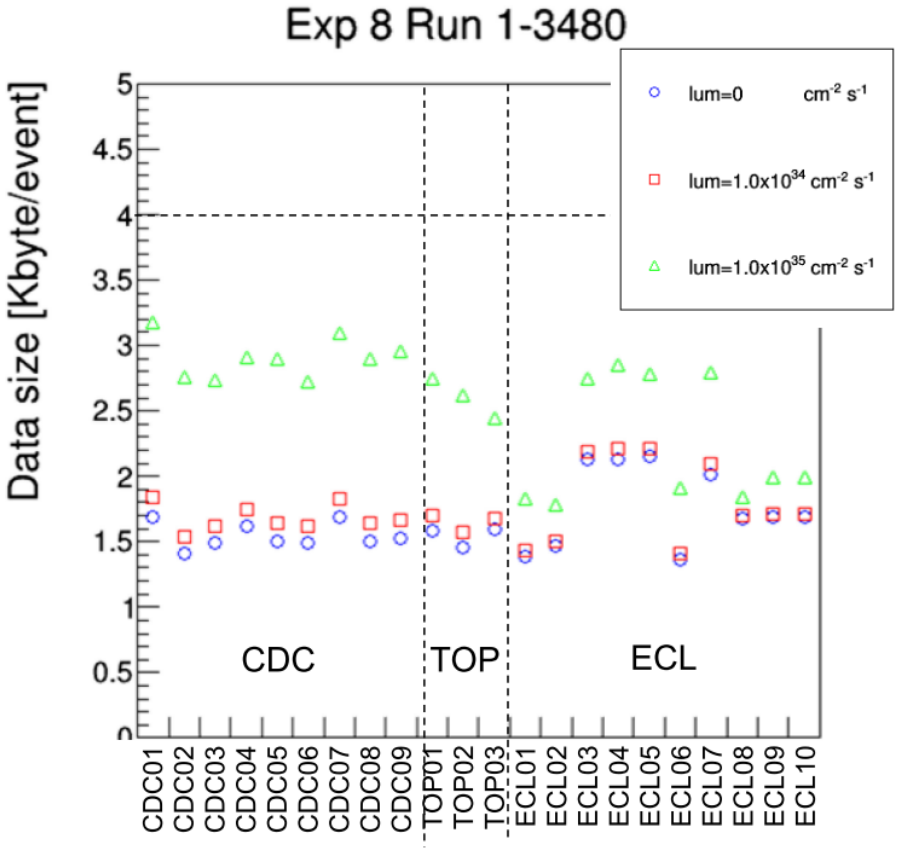
	SVD data size [kB/event]	SVD data rate @ 15kHz [MB/s]	SVD data rate @ 30kHz [MB/s]
COPPER	max. ~ 2.3	max. ~ 35	max. ~ 70
ROPC	max. ~ 11	max. ~ 170	max. ~ 350
EB1	~ 84	~ 1200	~ 2500
		HLT rate ~2.5kHz	HLT rate ~5.0kHz
HLT/ Storage	~ 84	~ 210	~ 420

2019

(Sugiura-san)



Extrapolation to high luminosity



- Data size was extrapolated to 10^{34} cm^{-2}s^{-1} and 10^{35} cm^{-2}s^{-1}
- Bottleneck due to 1GBit ethernet cable is 125MB/s
- Under high trigger rate =30kHz, bottleneck corresponds to about 4kB/event for each readout pc.
- When current data is extrapolated to luminosity= 10^{35} cm^{-2}s^{-1}, data size would be below 4kB/event.
  - If extrapolated to 8×10^{35} cm^{-2}s^{-1}, data size>4kB/event
- Luminosity is not high in experiment 8
  ⇒ Is extrapolation valid for high luminosity?

CDC

(T.Nanae)

➢ B2link error

- 7 FEs are masked during phase-3 physics run
  - #247,204,218 (b2llost) : fixed once ~2 years ago, but appear again
  - #37,193 (b2llost) : new
  - #97, 115 (ttlost/crc error/b2link error) : new. it was occurred when we had resumed operation with Belle solenoid turned ON

-> Zhou-san and Nanae-san investigated link status with IBERT.

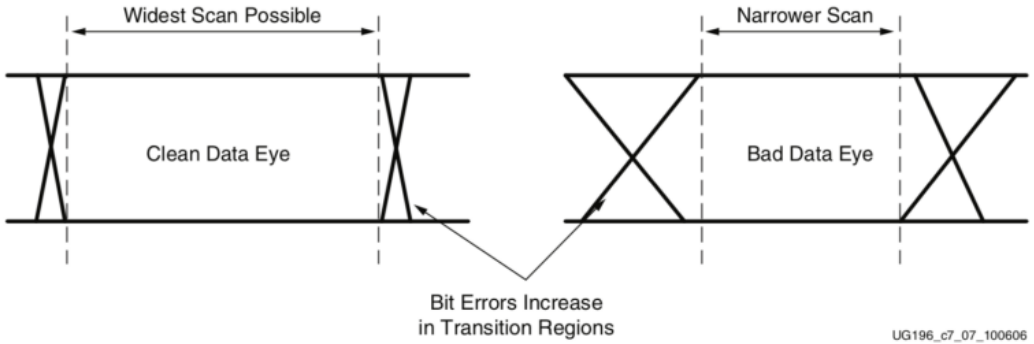
➢ Error signal from FEE

- operation with included in GLOBAL (Apr. 1 - June 30)
- Errors
  - rerr x13
  - fifoerr x9
  - semmbe(multi bit error) x1 (20190503, ~14:00), FE#20

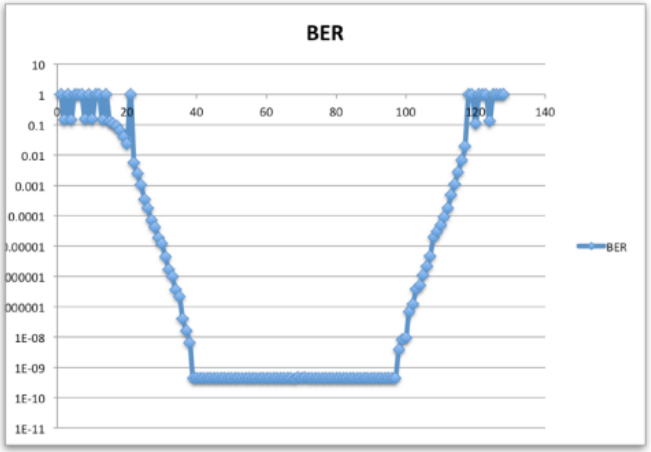
- mostly occurred inner part ?
- study for relation with radiation is ongoing
  - background level measured by diamond sensor and neutron detectors

(Q.Zhou)

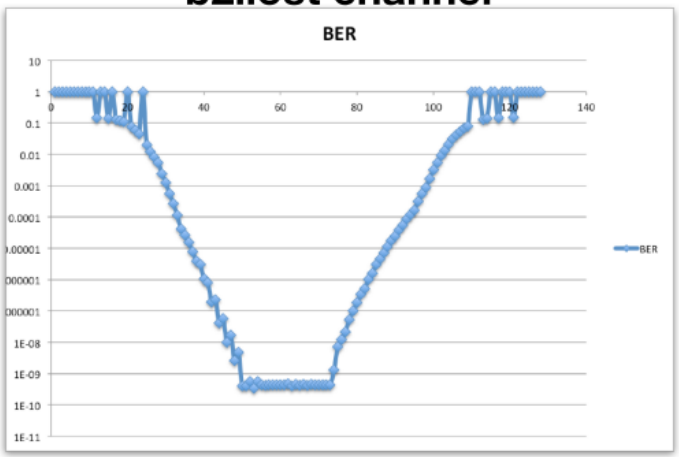
Swing test result



Reference channel



b2llost channel

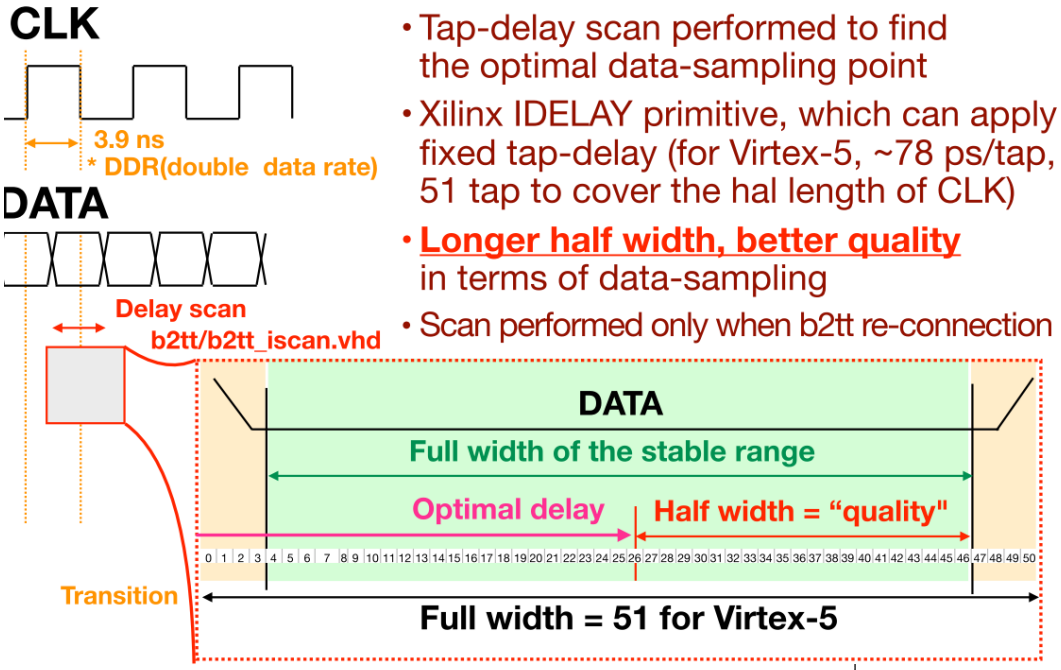


- **The b2llost links show bad eye diagram, while the b2lerror links show normal eye diagram.**
- **By swapping the fiber on HSLB side, RX of fiber data transmission on the HSLB is working well.**

FEE -> HSLB direction. -> Clearly worse than the normal link.

(T. Kunigo

Schematic: data-sampling scan



- Tap-delay scan performed to find the optimal data-sampling point
- Xilinx IDELAY primitive, which can apply fixed tap-delay (for Virtex-5, ~78 ps/tap, 51 tap to cover the hal length of CLK)
- **Longer half width, better quality** in terms of data-sampling
- Scan performed only when b2tt re-connection

Establish a way to check link condition, by measuring stable range in delay-scanning.

FTSW#235 - FTSW#047

* Read only once

TX port number (#235, ft3r) \ RX port number (#047)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1	18	16	15	18	19	16	19	20	18	16	19	19	20	13	20	16
3	18	11	12	14	11	11	11	10	9	9	17	18	19	12	19	10
5	18	10	11	10	9	9	9	9	8	8	19	18	19	10	19	8
7	17	10	9	9	6	11	10	10	9	8	17	17	17	8	13	10
9	17	10	10	10	9	10	9	10	8	8	18	17	18	10	18	8
11	17	18	19	19	18	18	19	19	18	18	17	17	17	18	18	18

FTSW#240 - FTSW#047

RX port number (#047)

TX port number (#240, ft3o)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
3	19	14	20	14	19	12	19	11	18	12	19	19	19	14	19	12
5	18	19	10	11	14	19	10	19	8	18	18	18	19	11	18	10
7	17	8	9	8	7	17	7	9	6	9	17	16	18	9	17	7
9	17	11	10	11	10	18	9	8	23	17	18	17	12	11	9	9
11	18	19	18	18	14	18	18	18	16	17	17	12	18	18	14	18

(O.Hartbrich)

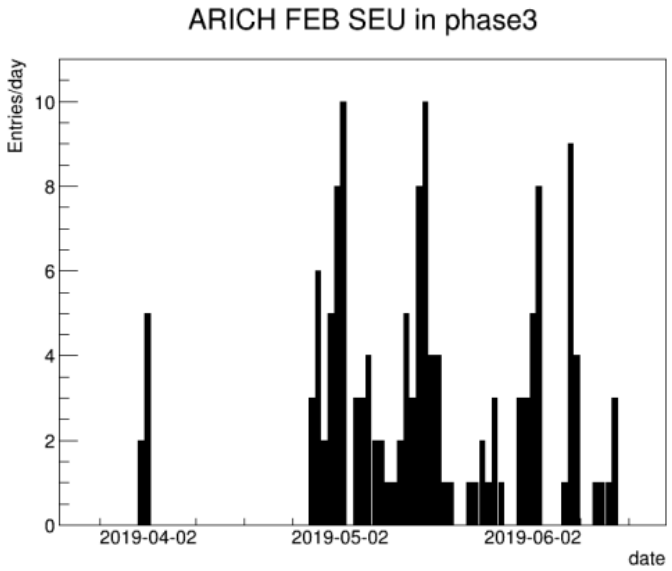
TOP

Readout Status

- SCROD CPU crashes at ~1 BS/day
  - Recover by powercycle of the frontend (~20min)
  - Strong dependence on background conditions: happens more often when background rates are high and “spiky”
  - Don’t the know the exact reason, difficult to debug, cannot reproduce reliably
  - Maybe SEUs? Implementing SEU detection cores and DDR error checking into FW now. (but issue also happens in null runs without beam, though very rarely)
- Some ASICs self-masking in some runs (no response from ASIC within timeout)
  - Negligible hit loss, mostly recovered on run restart/SALS

ARICH

(Y. Lai)



DAQ Problems in phase3: initialization

- In cold-start , we need to booths (re-programming HSLB) after re-configuring Merger.
  - Otherwise, 8-bit data shift problem will happen.
  - As far as I confirmed, only ARICH needs it. (CDCFE is also virtex-5 GTP)

FATAL	ARICH	14/04 11:15:47	ROPC405	cpr4013 : ERROR_EVENT : B2LCRC16 (00ff) differs from one (53a9) calculated by PreRawCOPPERfromat class. Exiting..
DEBUG	ARICH	14/04 11:15:47	ROPC405	cpr4013 : 00ff00ff 00ff00ff 00ff00ff ff550000
DEBUG	ARICH	14/04 11:15:47	ROPC405	cpr4013 : 00ff00ff 00ff00ff 00ff00ff 00ff00ff 00ff00ff 00ff00ff 00ff00ff 00ff00ff 00ff00ff 00ff00ff
DEBUG	ARICH	14/04 11:15:47	ROPC405	cpr4013 : 00ff00ff 00ff00ff 00ff00ff 00ff00ff 00ff00ff 00ff00ff 00ff00ff 00ff00ff 00ff00ff 00ff00ff

- When the data shift happens, FIFO will stop being filled. 00ff is the pattern taken from an empty FIFO inside HSLB.

ECL

(A. Kuzmin)

ttlost problem

ttlost happened for crate #4 just after power cycle or collector firmware reload.

After several ttlosts the connection became stable.

After cable unplug/plug the problem has disappeared.

We continue to monitor the stability

Beam burst problem

-If no ADC data recorded – no problem

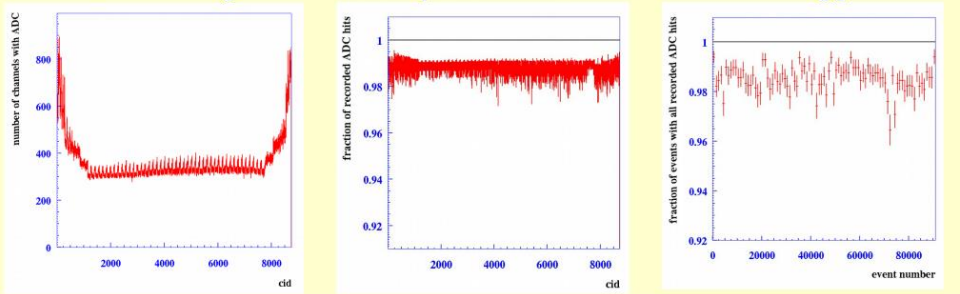
-If steady run with ADC data record – no problem

-In case of bad injection or beam burst +ADC data record – ECL busy

Block ADC data when FIFO is still not almost empty. ->

-Run #1131 with ADC record was taken

-The described algorithm was implemented + scale to 30 kHz trigger



-The lost of the ADC data ~1.2% at 30 kHz

KLM

(C. Ketter)

- RPC readout and (simple) scintillator readout basically running stably

Back-end Issues

- Intermittent BUSY from KLM COPPERs
  - When not recovered by SALS, requires rebooting all HSLBs to restore
  - Observed about once every 2 or 3 weeks
- Intermittent problems with HLT_KLM (e.g. elog/KLM/37)
  - Once at beginning of phase 3, turned out that old node or port numbers were being used
  - Once at end of Spring run, had to restart HLT_KLM
- Intermittent lock-up of COPPERs (e.g. elog/KLM/49)
  - Can't ssh into one or more (usually one) of them
  - Requires restarting of COPPER
  - Observed at least twice in Spring run
- Power cycling COPPER crate does not automatically bring up FINESSE
  - Have to reboot ttrx/HSLBs
  - Observed near end of Spring run

TRG

(T. Koga)

Troubles during phase III

- Bug of event suppression logic for CDCTRG	Fixed
- B2L error of ETF	Masked
- Bit shift of B2L data from GDL	Fixed
- May 2019: VME parameter error	Temporal solution
- May 2019: LVDS connection error btw. GDL and GRL	Fixed
- BUSY from GDL	Reason is unknown
- Ttlost	Reason is unknown
- CDCTRG dataflow is down due to CDCFE or merger	Reason is unknown
- GDL lost signal from ETM.	Reason is unknown

GDL full readout plan in Autumn run

-GDL readout data is time integrated at present.
4bit(127MHz) -> 1bit(32MHz) to reduce data size.

-Full readout will be added in debug mode in Autumn run
- -4 B2L lines from one UT3 board
- -4 more HSLB (cpr15003ab,4ab), 2 or more ropc, and 4 more FTSW are needed
- -firmware is being tested
- -apply scale factor to reduce datasize

(S. Yamada)

Hardware task in COPPER/ROPC : todo before the fall run

Additional nodes
- TRG COPPER : 2 COPPERs(4 links)
  - Installation was done.
- TRG ROPC : Add trg03 (+trg04)
  - Installation of trg03 was done.

-> SLC setup is not yet done.

Network throughput
- SVD : Done before phase 3 (x2GbE)

- ECL : to do before the fall run

Replacement
- Cdc06 : frequent disk? Trouble
  - Replace with a new server

DAQ UPGRADE

(G. Varner)

MoU: Replacement timescale

- **This schedule doesn't reflect long summer shut-down in 2020 (TOP MCP-PMT replacement, other work)**

Year	2018	2018	2018-2020	2020	2020	2021	2021	2022	2022	2023
Month	Jul.16	Oct.31	Apr/18 Mar/20	Apr.	July-Sep.	Jan.	July-Sep.	Jan.	July-Sep.	Jan.
	Proposal deadline	Decision								
Proto typing										
Mass Produc-tion										
COPPER-replacement					repl. 1	spare	repl. 2	spare	repl. 3	spare
Comment		Multipe candi-dates may be chosen?	test with pocket DAQ							

Could be shortened depending on budgetary situation and integration resullts

- COPPERs are replaced detector by detector during summer shutdown period in 2020, 2021, and 2022.
- Short winter shutdown might be utilized for additional work.

- Implies requirement for concurrent operation

SCHEDULE

- It seems that 3months shutdown is not enough for full replacement
    - readout test at test bench for all-subdetector might be also difficult, if delivery of new hardware will be near the summer shutdown in FY2020.
    - So, support for installation/commission length will be extended to JFY2021.
    - But, anyway some sub-systems should be replaced in FY2020 (which subsystem ? TOP(KLM)+SVD+CDC ?)
    -> Discussion : will see the commission status at the test bench to decide
    - Co-exists with the current COPPER system
    - Then, In my idea, the longer shutdown can be used for the replacement of the rest of sub-detectors

Tentative installation plan

- 2020 Summer shutdown (3months)

  - TOP(KLM) : the 1st choice

  plus

  Depending on the commissioning status at test bench.

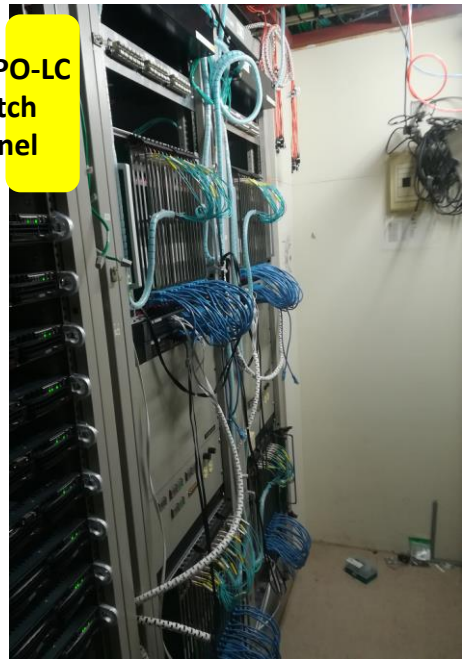
  - SVD, CDC or others ?

  It is better to operate with multiple systems, because it can provide some information when some trouble happen.

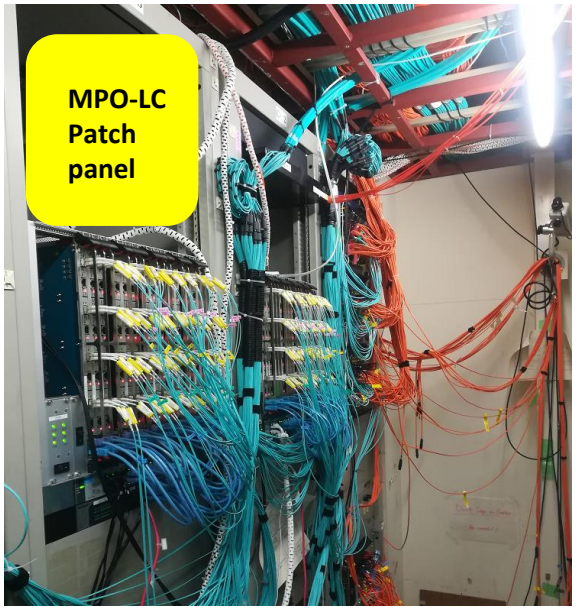
  - Coexists COPPER and new system

- 2021 Possible longer shutdown (6month? From January earliest ?)
  - Still keep COPPER for the moment for roll-back option

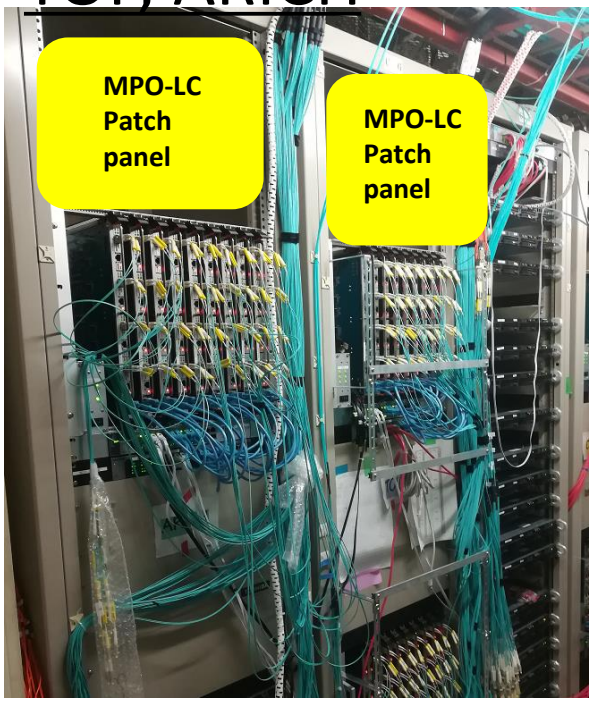
SVD



CDC

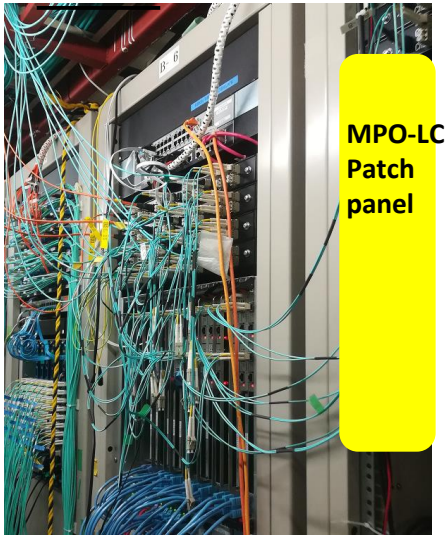


TOP, ARICH

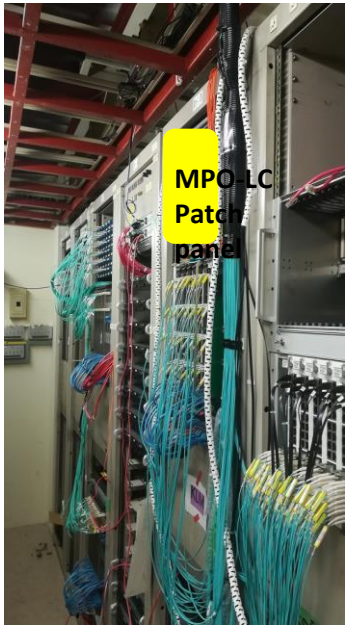


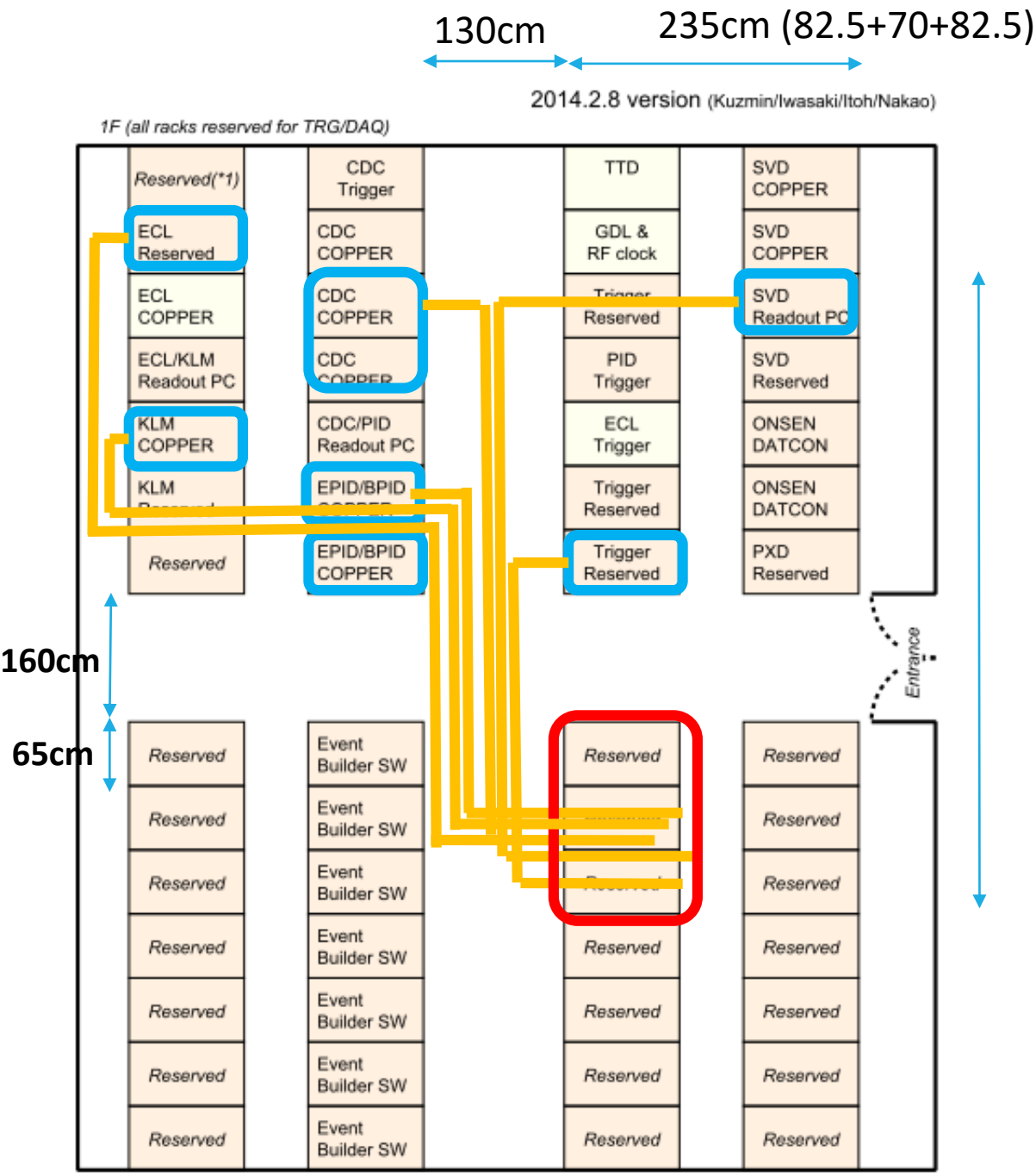
ECL

TRG



KLM




130cm
235cm (82.5+70+82.5)
2014.2.8 version (Kuzmin/Iwasaki/Itoh/Nakao)
1F (all racks reserved for TRG/DAQ)
Reserved(*1)
ECL Reserved
ECL COPPER
ECL/KLM Readout PC
KLM COPPER
KLM
Reserved
CDC Trigger
CDC COPPER
CDC COPPER
CDC
CDC/PID Readout PC
EPID/BPID
EPID/BPID COPPER
TTD
GDL & RF clock
Trigger Reserved
PID Trigger
ECL Trigger
Trigger Reserved
Trigger Reserved
SVD COPPER
SVD COPPER
SVD Readout PC
SVD Reserved
ONSEN DATCON
ONSEN DATCON
PXD Reserved
Entrance
160cm
65cm
Reserved
Event Builder SW

LIAISON WITH DAQ-UPGRADE PROJECT

- The impact of modification is minimize in sub-detector side.
  - use belle2link -> no update for FEE firmware
  - update of SLC software -> previous talk.
- But, as for commission, we need to work together with sub-detector DAQ experts.
  - Building a test bench (KEK or home-institute ?)
  - How to configure FEEs

	Candidates	Test bench
SVD	Katsuro-san ?	Tsukuba B4
CDC	Nanae-san (O.K.)	Tsukuba B4
TOP	Oskar/Martin ?	Tsukuba B4, Hawaii
ARICH	Yun-tsung ?	KEK ? Kitasato ?
ECL	Mikhail (for now)	
KLM	New UH post-doc ?	Hawaii
TRG	Koga-san (O.K.)	
FTSW preparation	Nakao-san/Kunigo-san?	

SUMMARY

- Readout status during the phase III was basically stable.
  - A lot of efforts to investigate the troubles are on-going towards the autumn run
- DAQ Upgrade plan
  - The 1st replacement of COPPER boards will happen in the next summer shutdown.
  - Schedule of each sub-system's replacement will be confirmed as commissioning is on-going. TOP(KLM) could be the 1st choice.
  - Asking to have liaison from each sub-detector group for the upgrade project.