# B2tt-lost study
## ～ quality monitor for b2tt-links ～


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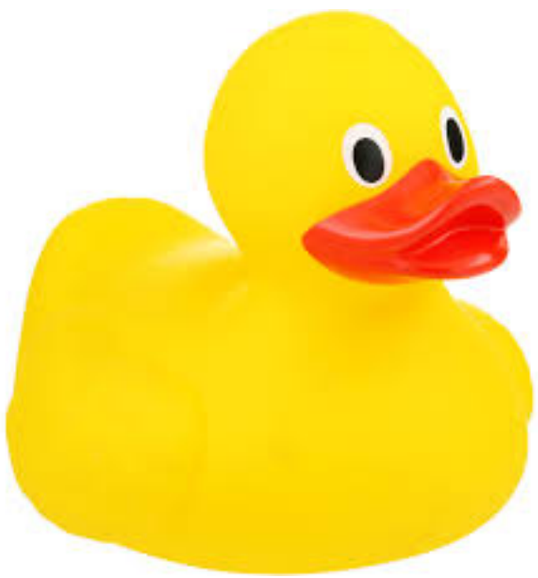

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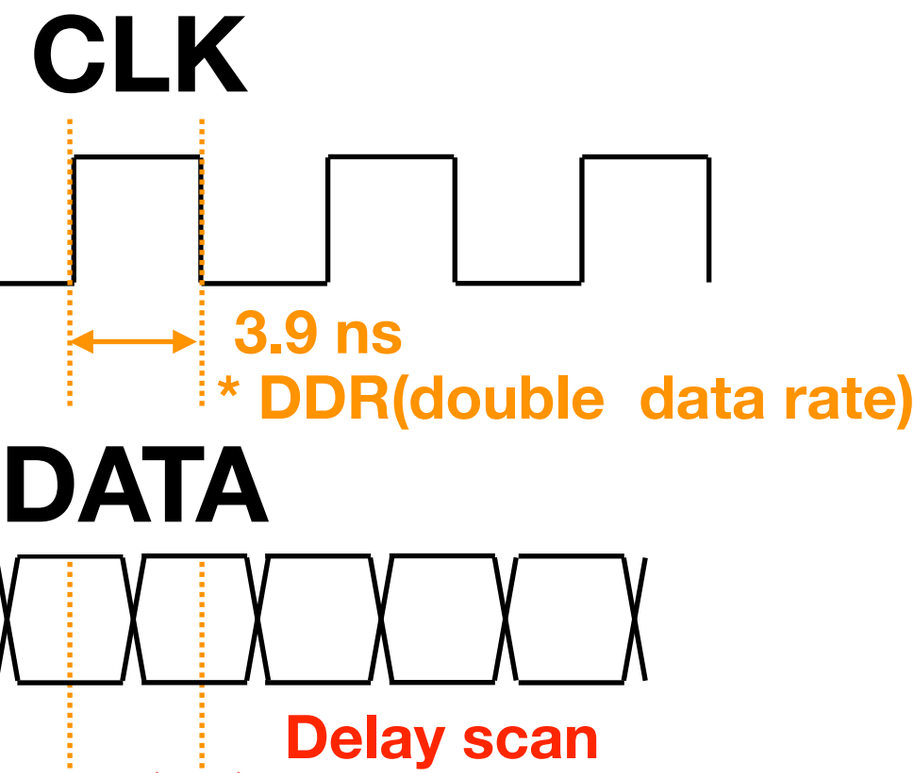
Belle II Trigger&DAQ workshop

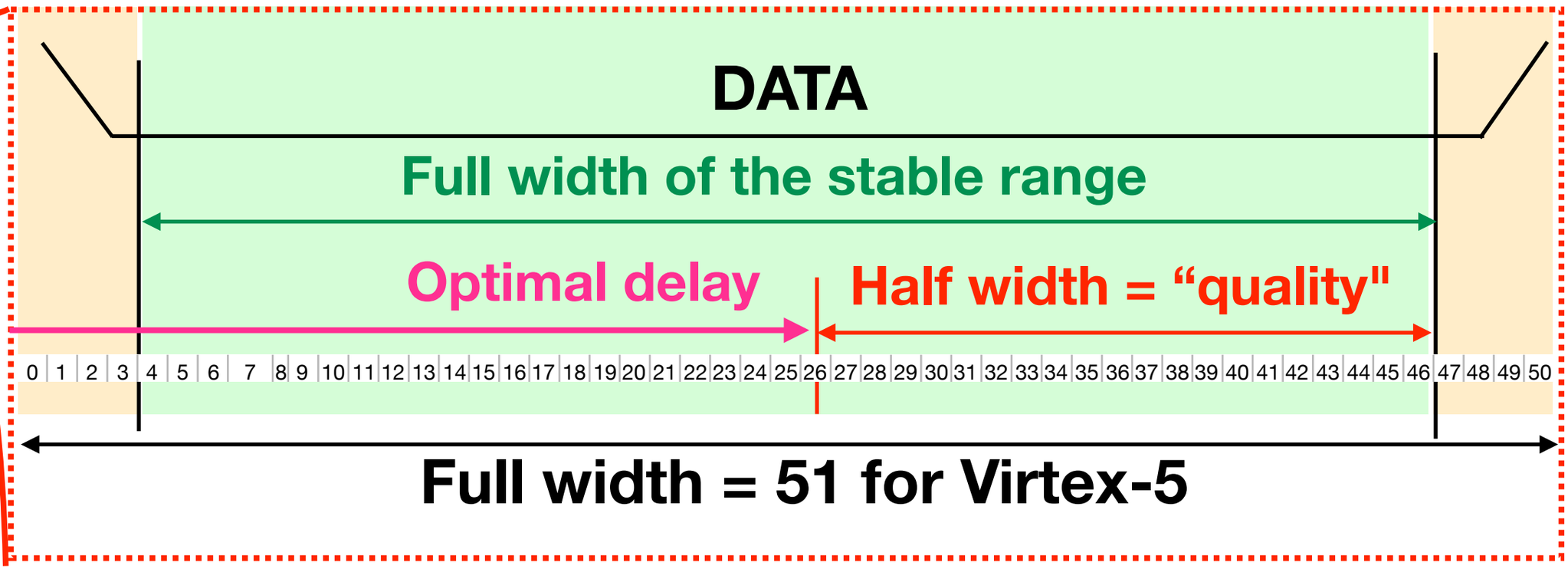
# Introduction

- In order to improve the reliability of the TTD system, it is an urgent task to **improve the b2tt stability**
- Current b2tt protocol checks only whether the link is established
  ➡ No info about the cause(s) of b2tt-lost
- To tackle this issue, we **add "quality" values for b2tt-links**
  ➡ Reject low-quality links
- Several possible qualities to be checked;
  as a first step, we add a quality value for monitoring **data-sampling stability**

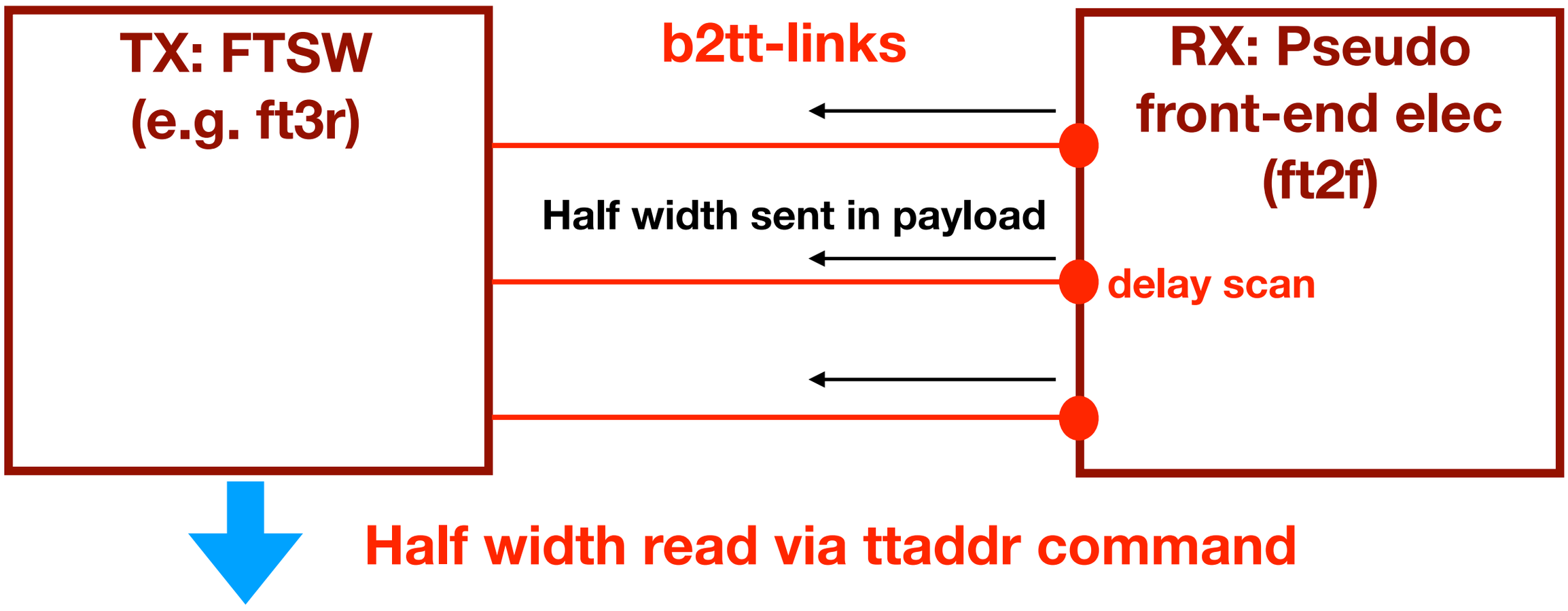
# Schematic: data-sampling scan




- Tap-delay scan performed to find the optimal data-sampling point
- Xilinx IDELAY primitive, which can apply fixed tap-delay (for Virtex-5, ~78 ps/tap, 51 tap to cover the hal length of CLK)
- **Longer half width, better quality** in terms of data-sampling
- Scan performed only when b2tt re-connection



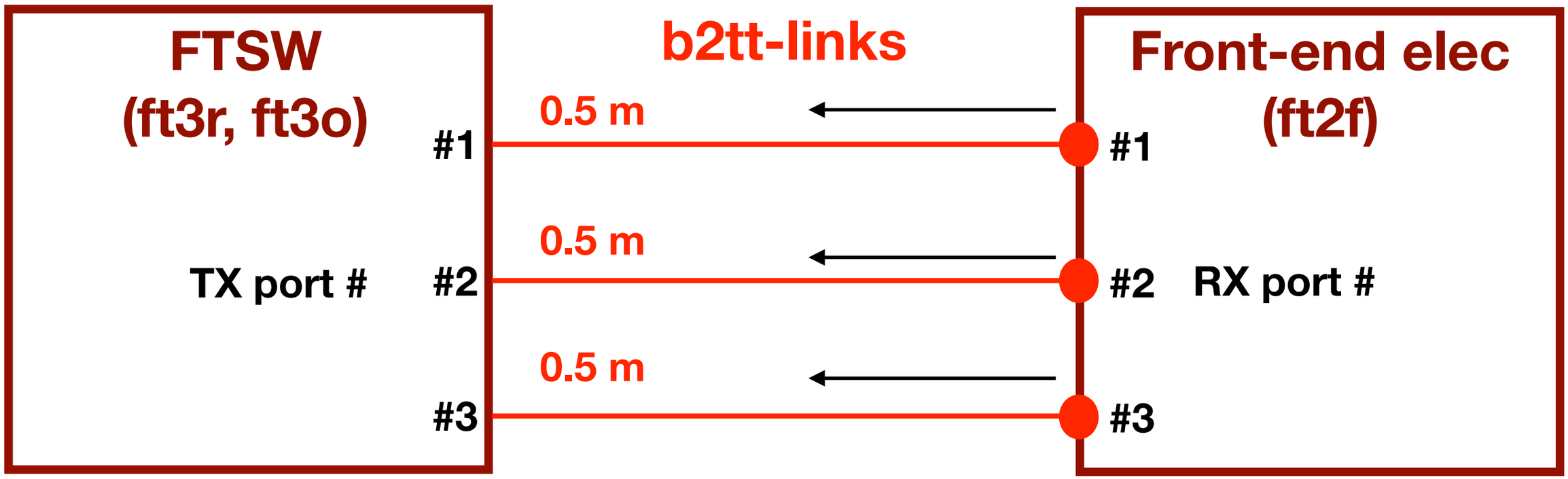
# Test procedure




## Test items

1. Port dependency
2. Cable length dependency
3. Stability test

# Test #1: port dependency




- Half width values checked for all the possible combination among the TX ports and the RX ports
- By re-connecting CAT7 cable, the quality sometimes become good/bad
- 2 different TX setup;
  - FTSW#235 with ft3r firmware
  - FTSW#240 with ft3o firmware

# Test #1: Results

## FTSW#235 – FTSW#047

* Read only once

TX port number (#235, ft3r)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 18 | 16 | 15 | 18 | 19 | 16 | 19 | 20 | 18 | 16 | 19 | 19 | 20 | 13 | 20 | 16 |
| 3 | 18 | 11 | 12 | 14 | 11 | 11 | 11 | 10 | 9 | 9 | 17 | 18 | 19 | 12 | 19 | 10 |
| 5 | 18 | 10 | 11 | 10 | 9 | 9 | 9 | 9 | 8 | 8 | 19 | 18 | 19 | 10 | 19 | 8 |
| 7 | 17 | 10 | 9 | 9 | 6 | 11 | 10 | 10 | 9 | 8 | 17 | 17 | 17 | 8 | 13 | 10 |
| 9 | 17 | 10 | 10 | 10 | 9 | 10 | 9 | 10 | 8 | 8 | 18 | 17 | 18 | 10 | 18 | 8 |
| 11 | 17 | 18 | 19 | 19 | 18 | 18 | 19 | 19 | 18 | 18 | 17 | 17 | 17 | 18 | 18 | 18 |

## FTSW#240 – FTSW#047

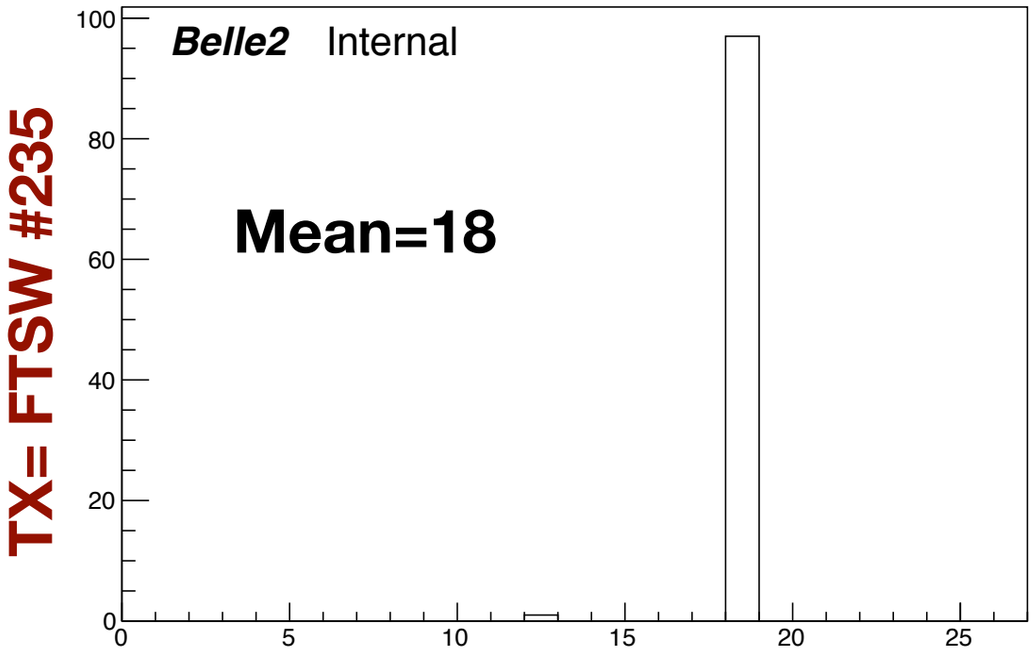
RX port number (#047)

TX port number (#240, ft3o)

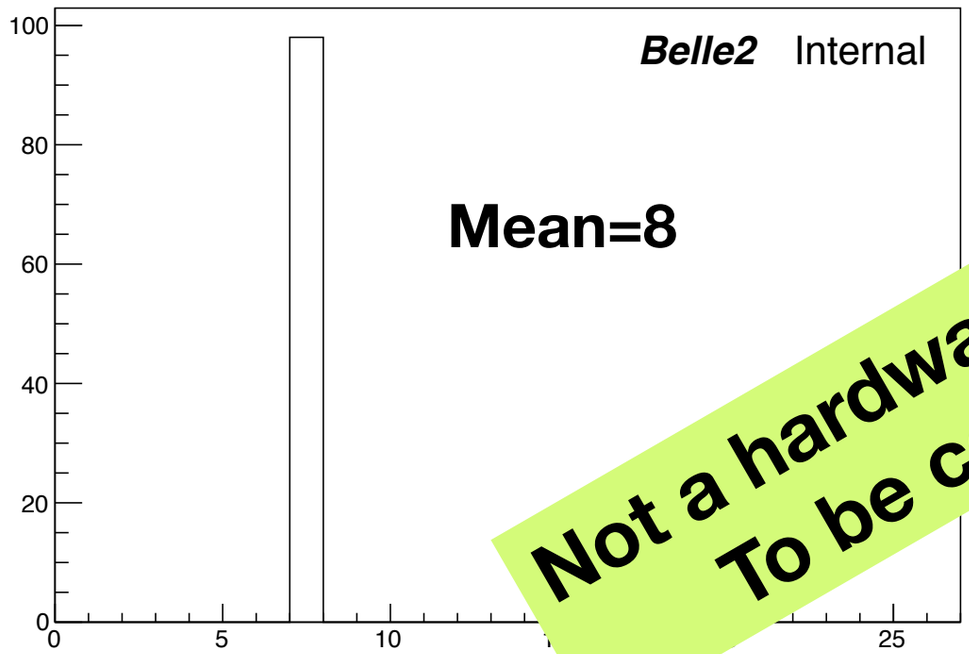
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 3 | 19 | 14 | 20 | 14 | 19 | 12 | 19 | 11 | 18 | 12 | 19 | 19 | 19 | 14 | 19 | 12 |
| 5 | 18 | 19 | 10 | 11 | 14 | 19 | 10 | 19 | 8 | 18 | 18 | 18 | 19 | 11 | 18 | 10 |
| 7 | 17 | 8 | 9 | 8 | 7 | 17 | 7 | 9 | 6 | 9 | 17 | 16 | 18 | 9 | 17 | 7 |
| 9 | 17 | 11 | 10 | 11 | 10 | 18 | 9 | 8 | 23 | 17 | 18 | 17 | 12 | 11 | 9 | 9 |
| 11 | 18 | 19 | 18 | 18 | 14 | 18 | 18 | 18 | 16 | 17 | 17 | 12 | 18 | 18 | 14 | 18 |

# Test #1: Results cont'd

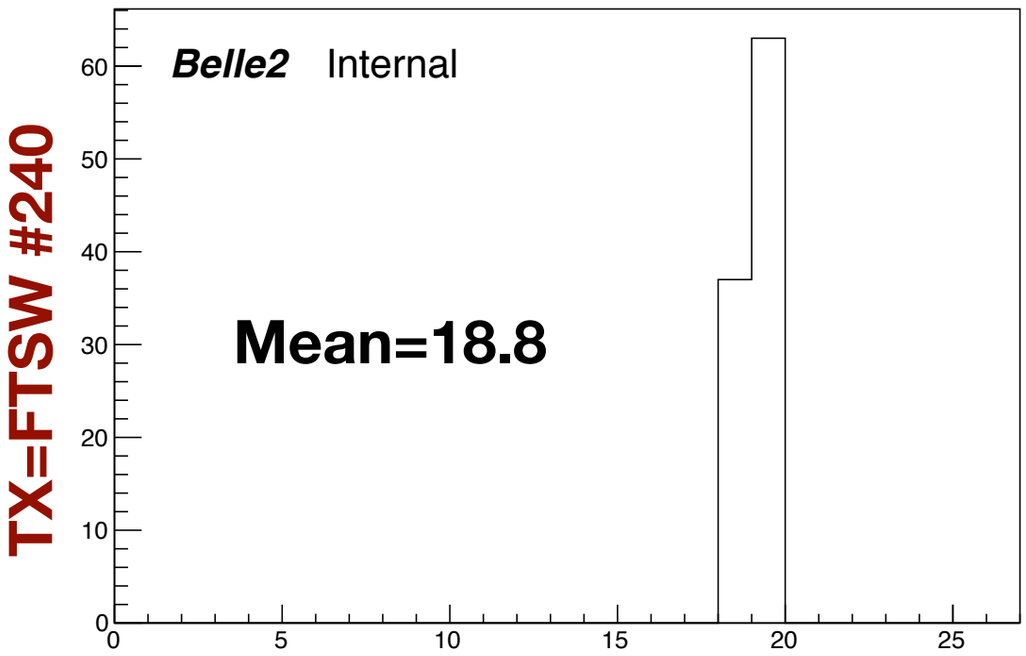
## TX port#5 - RX port#1

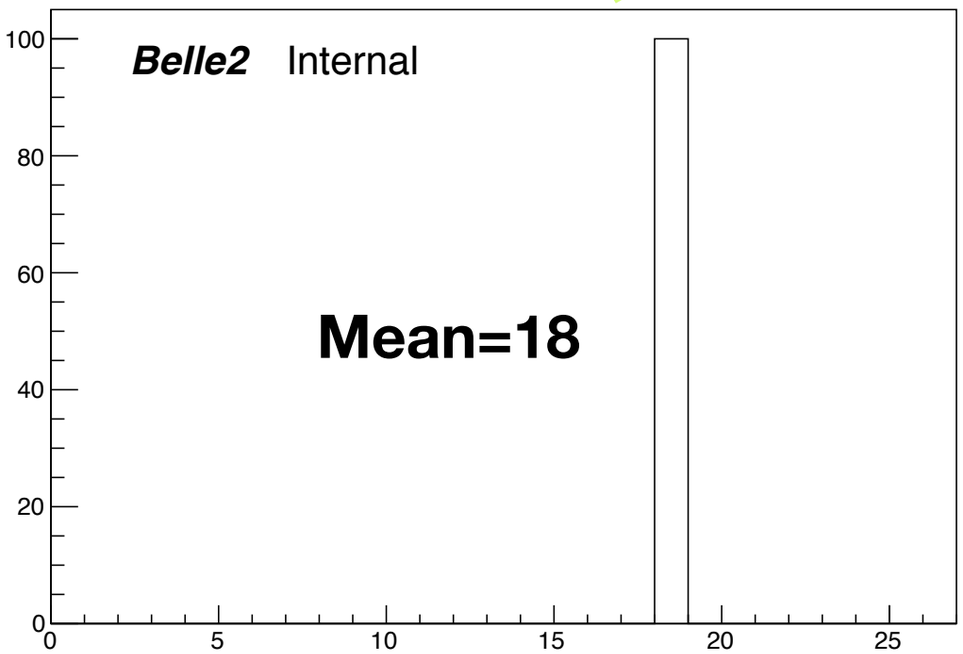



## TX port#7 - RX port#2

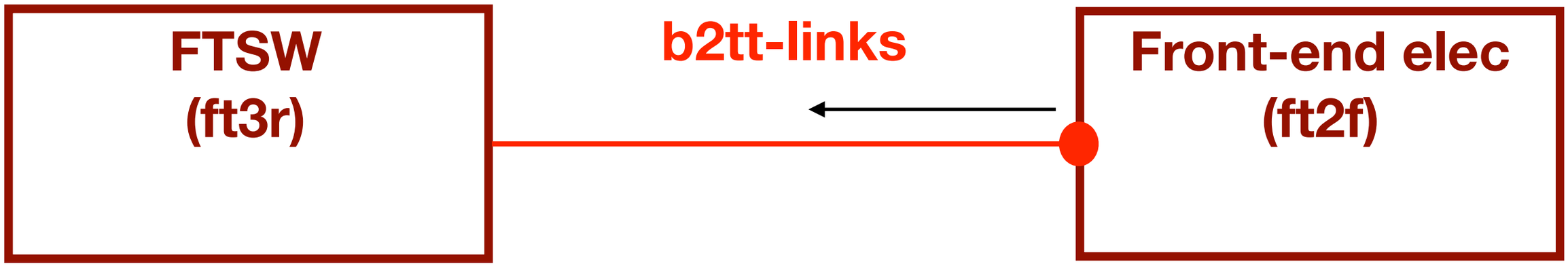


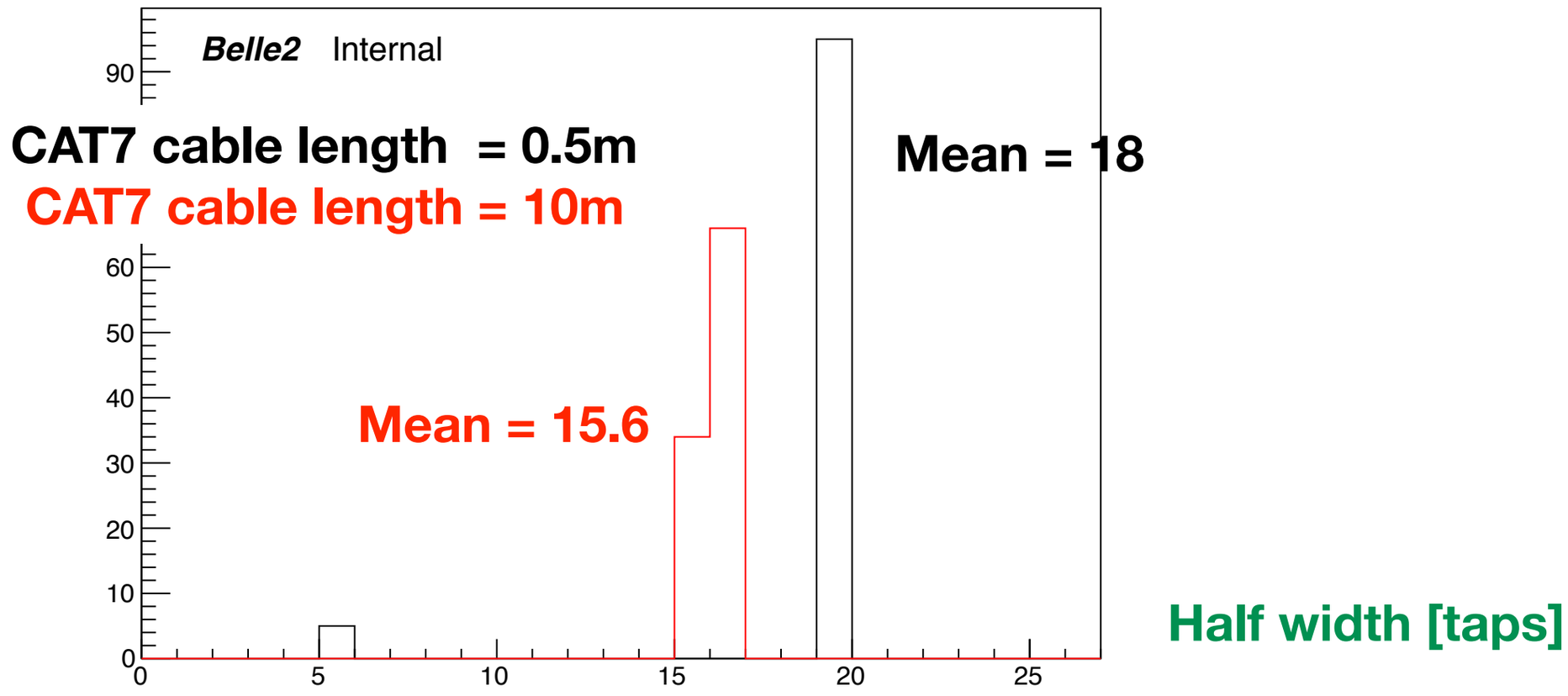

**Not a hardware fragility?**
**To be confirmed**



# Test #2: cable-length dependence

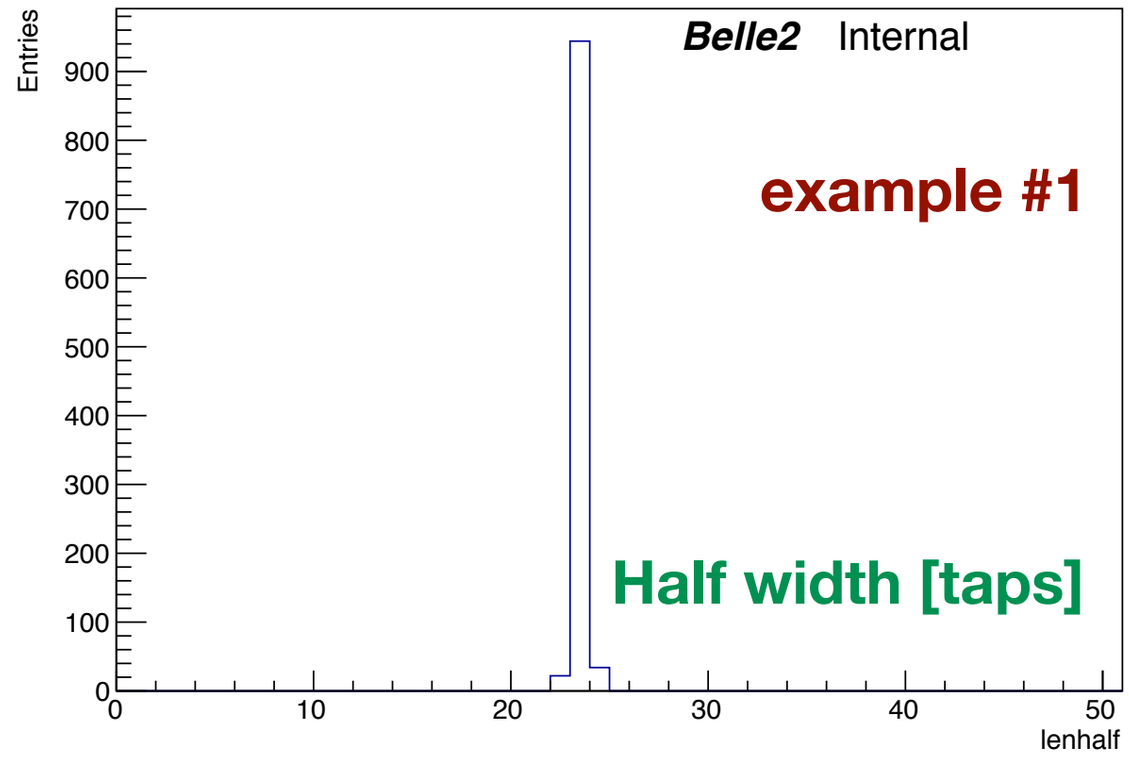


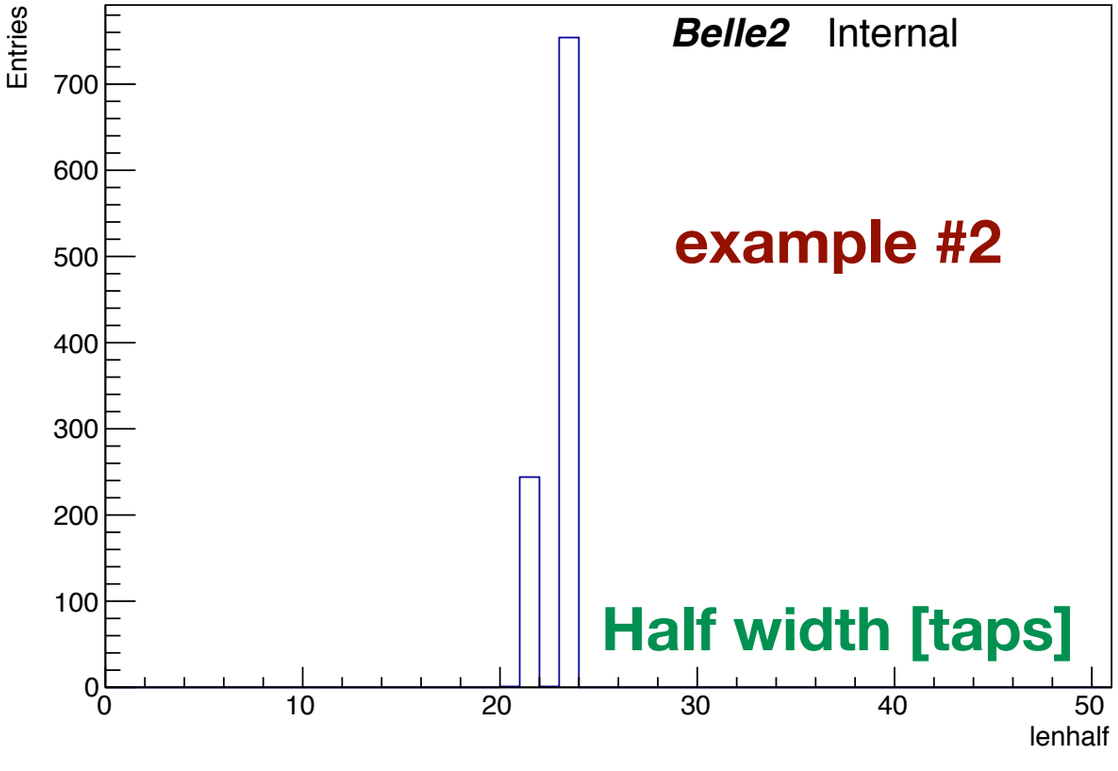



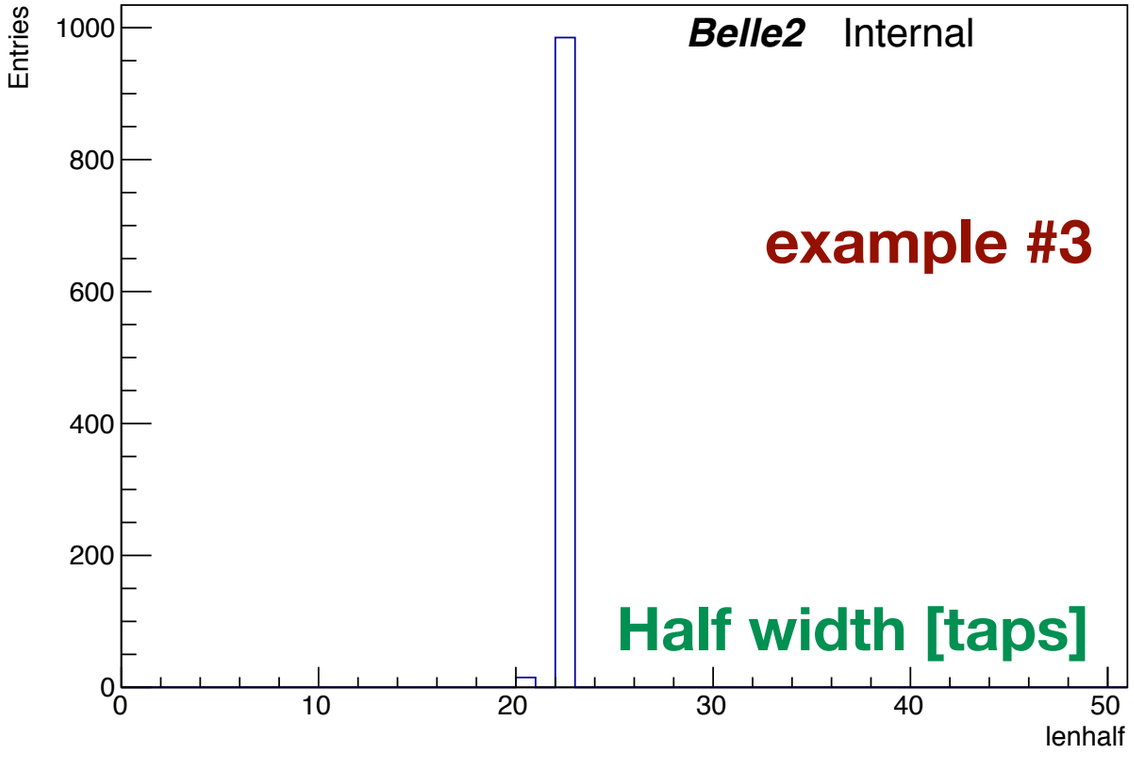

- Half width **worsened by 3 taps**
  by changing the cable length (**from 0.5m to 10m**)

# Test #3: Stability test

- **Fairly stable for re-connection**
- **seems to have some "characteristics" in stability**



# Test with ECL FEEs

- Updated b2tt implemented in ECL FEE to confirm its functionality

**ttaddr output**

```
5=07700 reg=0a000000 1300b463 ready tag=0 idly
 10=19900 33006033  idly
  0=19901 53049013  idly [b29 cpr5015a]
  1=19902 5302d113  idly [b30 cpr5015b]
  2=19903 5302b123  idly [b31 cpr5016a]
  3=19904 5302a143  idly [b32 cpr5016b]
  4=19905 5302b133  idly [b33 cpr5017a]
  5=19906 53047403  idly [b34 cpr5017b]
  6=19907 53027493  idly [fe7 cpr6007a]
  7=19908 5302a1f3  idly [fe8 cpr6008a]
  8=19909 530281f3  idly [be8 cpr6008b]
```

TX port #  Half width in hex

Summary table →

**170 taps covers 3.9 ns in Spartan-6 FPGA**

| TX port # | value |
|---|---|
| 0 | 73 |
| 1 | 45 |
| 2 | 43 |
| 3 | 42 |
| 4 | 43 |
| 5 | 71 |
| 6 | 39 |
| 7 | 42 |
| 8 | 40 |

- Confirmed that the **updated b2tt works fine** not only in FTSWs but **also in FEEs**

# Alex's slide, yesterday

## ttlost problem

**ttlost happened for crate #4 just after power cycle or collector firmware reload.**

**After several ttlosts the connection became stable.**

**After cable unplug/plug the problem has disappeared.**

**We continue to monitor the stability**

Result in the last page also indicates that we were not able to revisit this problem; in other words the problematic connection seems good from the b2tt quality

# Summary + To do

## Summary

- In order to improve the DAQ efficiency/stability, b2tt-link quality plays an important role
- Updated b2tt HDL to add a new feature; link-quality monitor
- Several tests performed using the updated b2tt;
  - Large port dependency
  - Cable length dependency
  - Fairly stable by re-connection but there is some characteristics
  - Tested with ECL FEE successfully

## To do

- Currently the updated HDL is available only in my (Takuto's) git repo.

➡ To deploy it to the whole Belle2 system

➡ Threshold optimisation (different thresholds for different FPGAs)

# Bonus slides

# HDL structure（RX）

top.vhd

b2tt(b2tt/b2tt.vhd)

b2tt_payload(b2tt/b2tt_payload.vhd)

elsif regsel = TTREG_IDLY then — 13
regs <= “000” & regsel & idly

b2tt_decode(b2tt/b2tt_decode.vhd)

b2tt_iddr(b2tt/b2tt_ddr_v5.vhd)

b2tt_iscan(b2tt/b2tt_iscan.vhd)

lenhalf(9 downto 0)

buf_idly <= "00" & lenhalf & '0' & cnt_idelay & "00" & sta_iddr

# HDL structure （TX, not needed)

ft3o.vhd

o_collect(common/o_cocllect.vhd)

o_decode(common/o_decode.vhd) in MINO to MAXO

b2tt_iddr(b2tt/b2tt_ddr_v5.vhd)

b2tt_iscan(b2tt/b2tt_iscan.vhd)

m_gdldecode(common/m_gdl.vhd)

b2tt_iddr(b2tt/b2tt_ddr_v5.vhd)

b2tt_iscan(b2tt/b2tt_iscan.vhd)

m_gdl(common/m_gdl.vhd) x5

b2tt_iddr(b2tt/b2tt_ddr_v5.vhd)

b2tt_iscan(b2tt/b2tt_iscan.vhd)

# I/O delay primitive in Xilinx FPGA

| | Number of taps | Maximum delay | Average delay per tap | Taps to cover 3.9 ns |
|---|---|---|---|---|
| **Virtex-5** | 63 | 4.9 ns | 78 ps | 51 |
| **Spartan-6** | 255 | 13.5 ns | 53 ps (30ps) | 73 (130)<br>* Nakao-san 170 |
| **Virtex-6** | 31 | 2.4 ns | 78 ps | |
| **Kintex-7<br>Zynq** | 31 | 2.4 ns | 78 ps | |