ADC cut in CDCFE

Yun-Tsung Lai

KEK

ytlai@post.kek.jp

Belle II TRG/DAQ workshop 2019

August 27, 2019

ADC cut in CDCFE for TRG data path

- TRG info from CDCFE: 1b wire hit and 3b timing, from TDC.
- ADC info: separated path from TDC in CDCFE firmware.
- Koga-sa

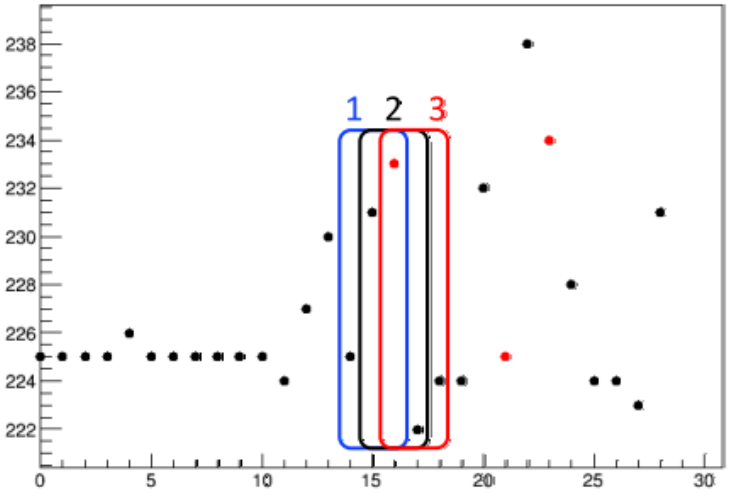
Proposal of ADC cut

-To reduce crosstalk, I propose to apply following cut:

ADC sum of three points > X (X=10 or 15, as described later)

-Three kind of sums are taken per one tdc hit. One of them should be > X.

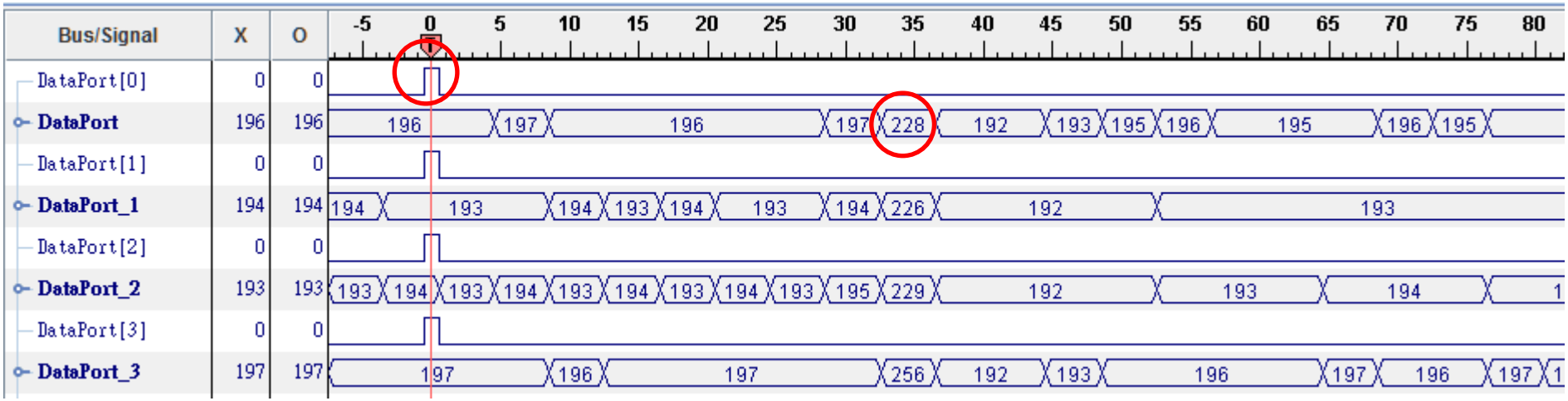
-1. $ADC_{i-2} + ADC_{i-1} + ADC_i$
-2. $ADC_{i-1} + ADC_i + ADC_{i+1}$ (i-th hit have tdc)
-3. $ADC_i + ADC_{i+1} + ADC_{i+2}$



- To implement the cut for TRG data path:
  - What is the timing offset between TDC info and ADC peak in firmware?

ADC cut in CDCFE for TRG data path (cont'd)

- By using CDCFE testbench with pulse generator:



- The ADC peak will appear ~32 clks (~256 ns) later than TDC hit (TRG hit).
  - Additional 256 ns delay in CDCTRG.

- With future updates on TSF and 2D, the latency might be reduced with 200~300 ns.
  - In my opinion, it should not be the first priority hence.
  - Still something worth trying to reduce fff rate (different definition of reduced 2D couting: aaa in GRL, making 3D/NN working etc).