CDC

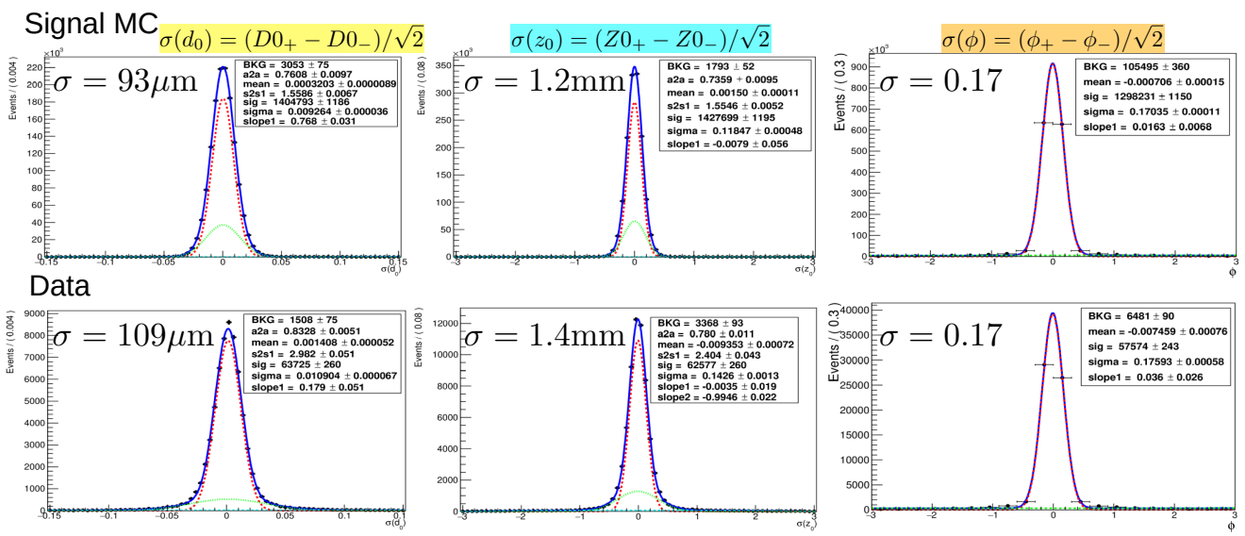
Nanae Taniguchi (KEK)

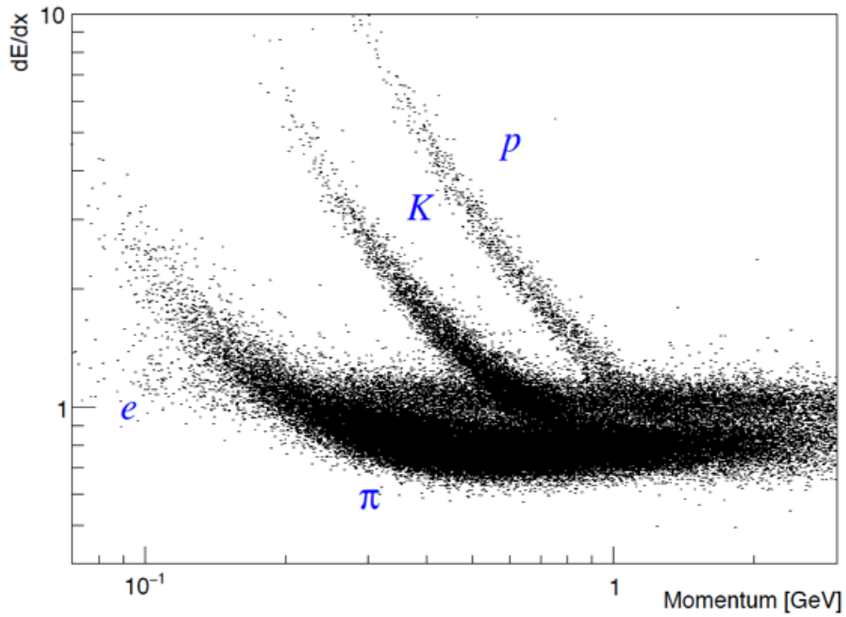
BPAC. 181022

performance in phase-2

- **CDC operation generally stable**
  - included in all luminosity runs
  - (ECL+CDC) was required as default
- **basic performance**
  - study with di-muon event sample is ongoing and resolution is reasonable compared with signal MC
  - monitoring and run dependent calibration are improved in dE/dx
    - hadron correction with fits is ongoing

di-muon event sample (barrel region)





hardware issues

- **There are 4 channels, which we could not supply nominal HV during phase-2 operation**
  - Layer(0-55) - Sector(0-3) : L4-2, L6-1, L15-1 and L19-2
    - L4-2 : HV line touches on ground level

      → put insulation tubes near feedthrough pins
    - L6-1 : HV line touches on ground level. It was occurred just before phase-2

      → one bad wire found and disconnected from HV line
    - L15-1 : reduced HV (1kV) can be supplied. It was occurred just after end-cap push in

      → nominal HV can be applied before opening CDC covers for summer maintenance work (we did nothing). HV cable might be pressed at end-cap closing. end-cap will be set at +5mm back position for phase-3
    - L19-2 : reduced HV (1kV) can be supplied. It happened in 2017 spring, but disappeared during investigating by opening CDC covers

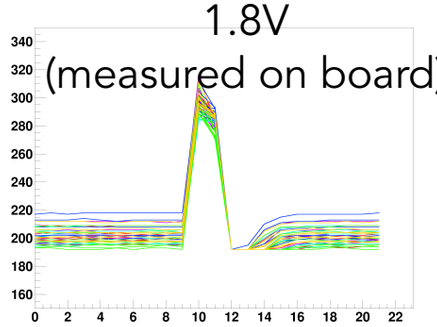
      → one bad wire found and disconnected from HV line

hardware issues

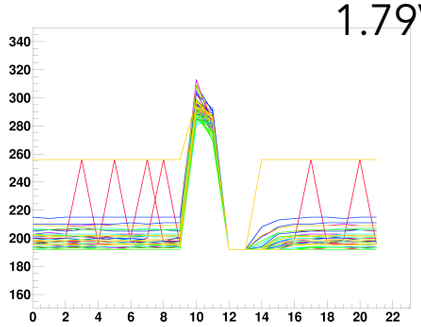
FADC:
- problem was reproduced at test bench before phase-2
- FADC use 1V8 from +2.0V. relation is clear
- output voltage is already at maximum
- new 2 DC power supply is overhauled
- replaced after phase-2
  (one of them malfunctioned in Sept.)

FADC waveform of test pulse

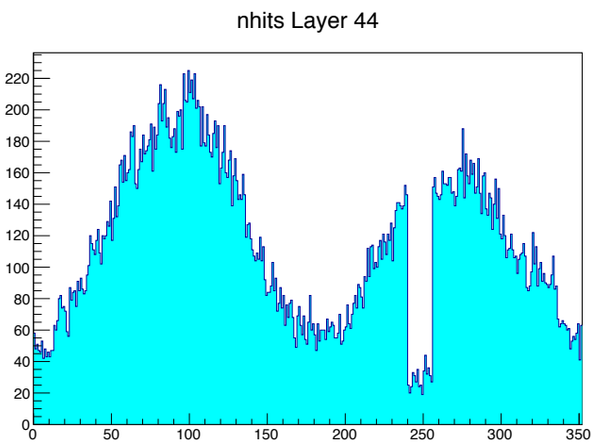
1.8V (measured on board)



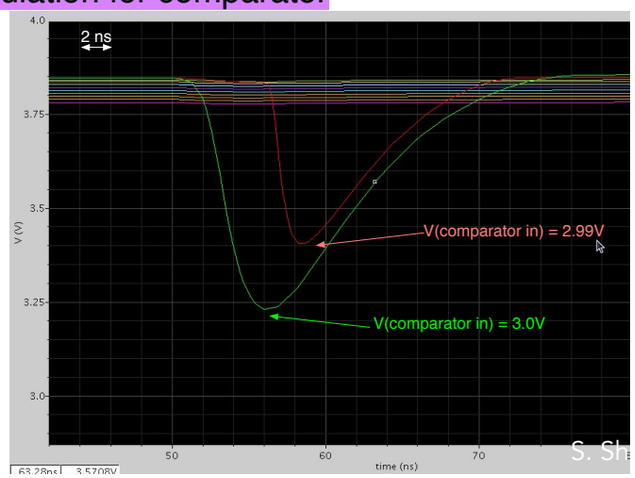
1.79V



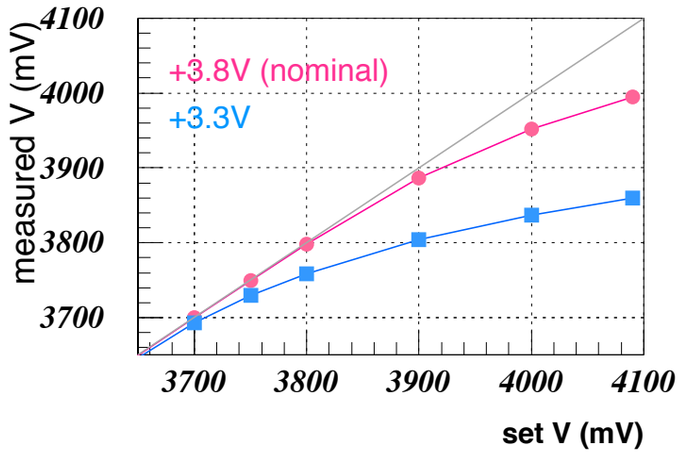
DAC:
- problem was not reproduced at test bench until we opened CDC
- DAC voltage use 5V0 from +5.5V, it is not a source of this problem
- we pin down by investigating installed FE and studying at test bench
  - +3.8V is lower, measured on board which has DAC problem
  - +3.8V produce 2V5 and 3V3 which are used for several part
  - checking diagram, one of 3V3 lines connected with VDDD of ASIC
  - According to expert developed ASIC, VDDD is related with comparator functions
  - there is a room to increase output voltage for +3.8V and increase by +0.2V



Simulation for comparator



comparison btw. measured and set values at test bench



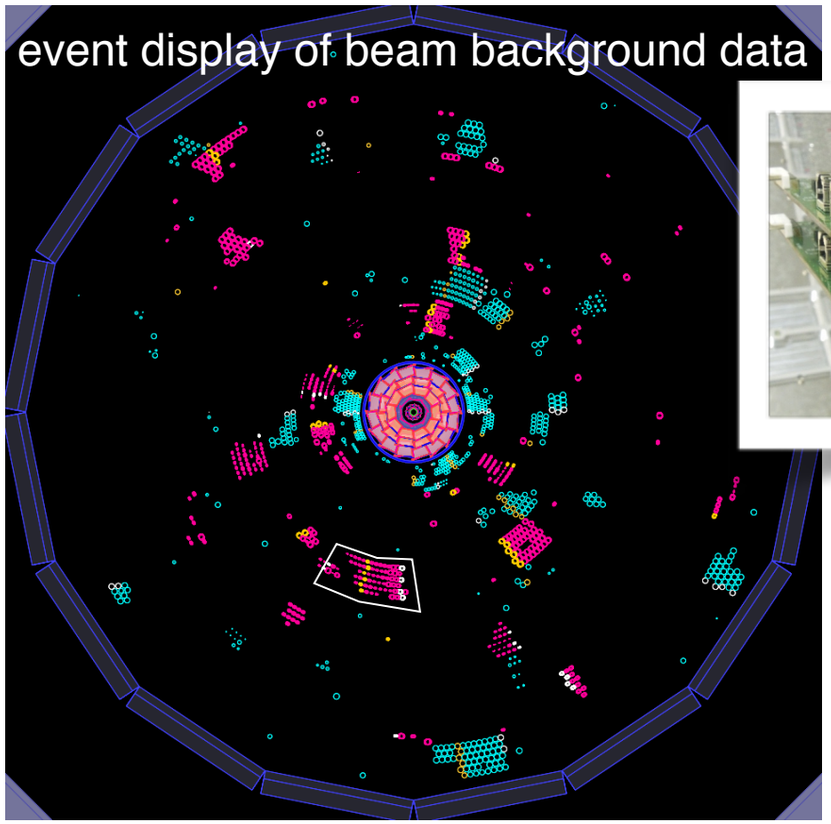
hardware issues

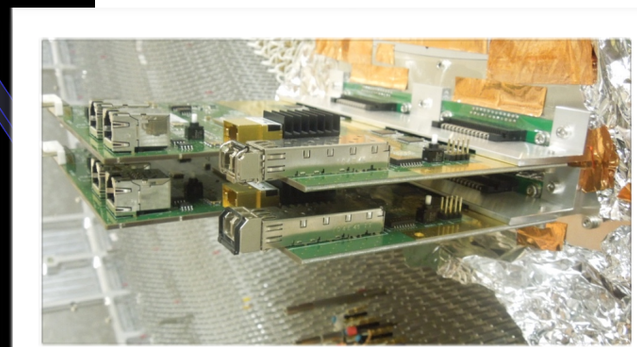
- **Sept. : Opening CDC covers to fix HV and readout issues**
- **perform power cycle of HV/LV everyday and check status**
  - hardware work during daytime and operation during night
- **additional problem haven't occurred so far**

- **plan to replace one or two more DC power supplies for driving FADC(+2.0V)**
- **consideration to suppress power consumption**
  - discussion with FPGA expert
- **plan for development of new FE readout board**
  - lower power consumption for FPGA and FADC should be achieved

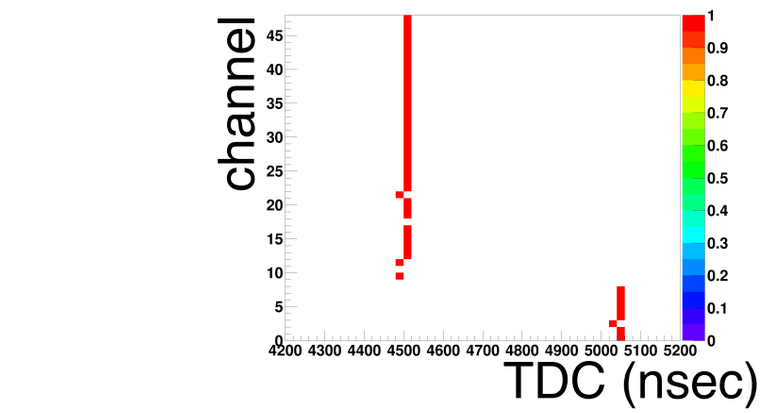
cross talk

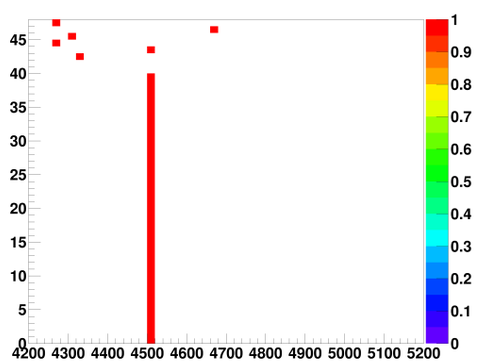
- clusters seen in random trigger data for beam background study
- most of cluster confined in the unit of FE board
- wire hits in same FE board have similar timing in event
- It is likely cross talk hits

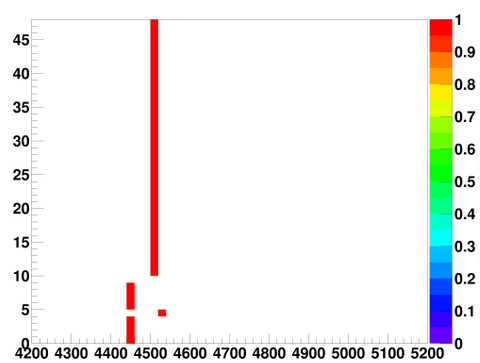




3 FE boards with more than 30 hits in a event

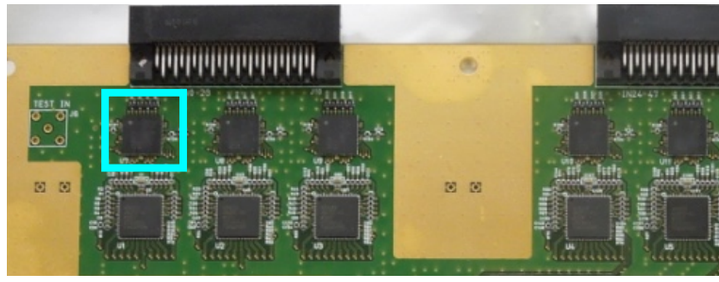




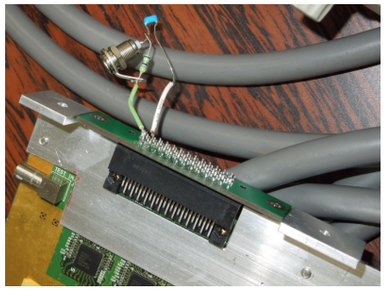


cross talk

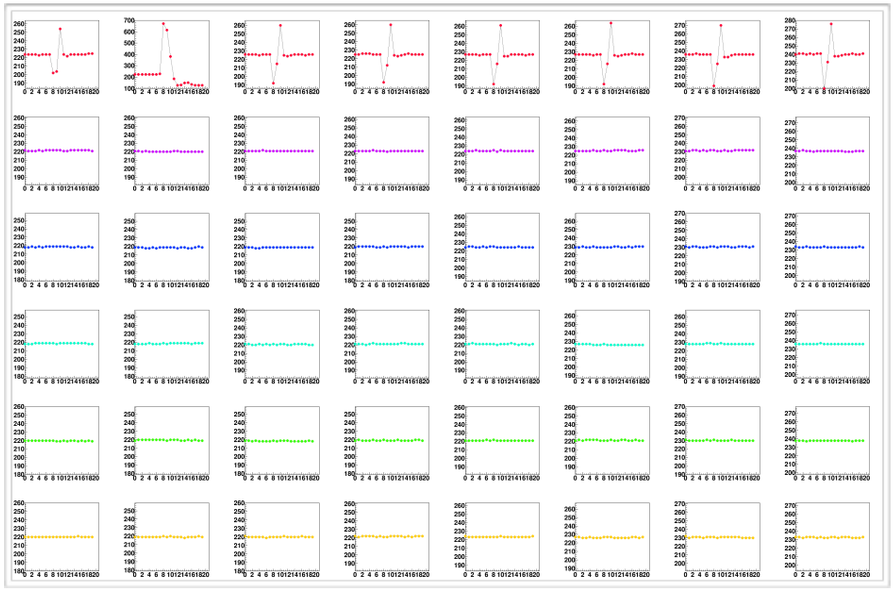
- **study for cross talk at test bench with single board**
  - large pulse input into one channel
  - time window is open 300 nsec after input signal



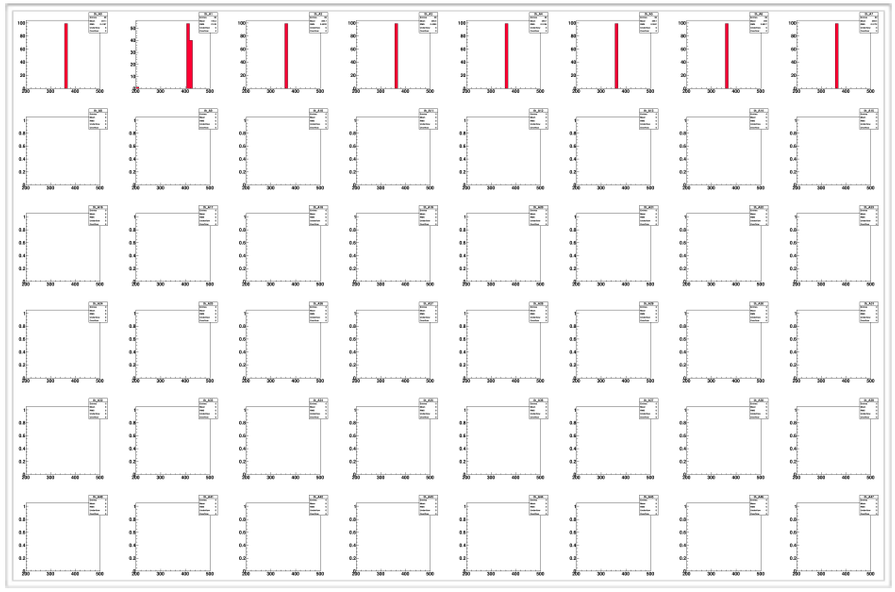
- cross talk are induced in only same ASIC
- time difference btw input signal and cross talk is ~ 60nsec

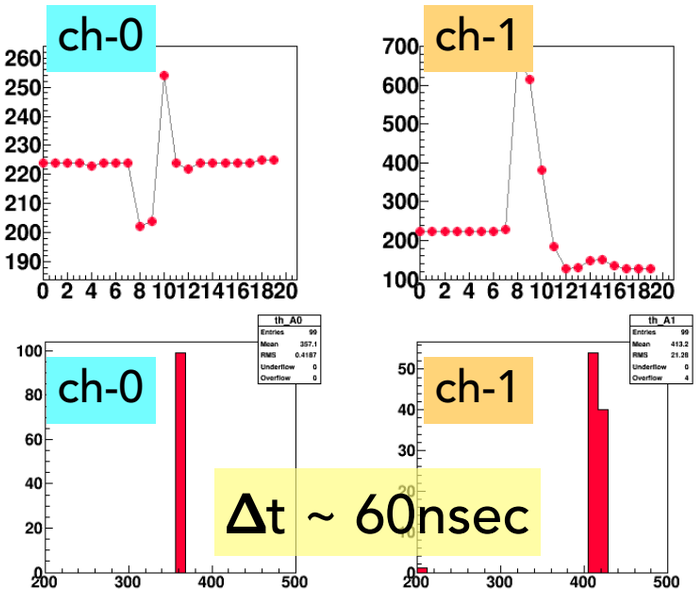


32MHz FADC waveform of test pulse



TDC distribution of test pulse



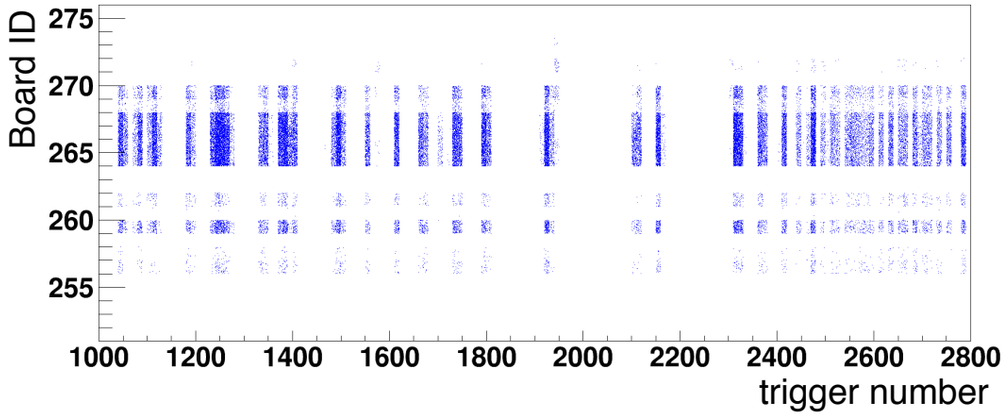


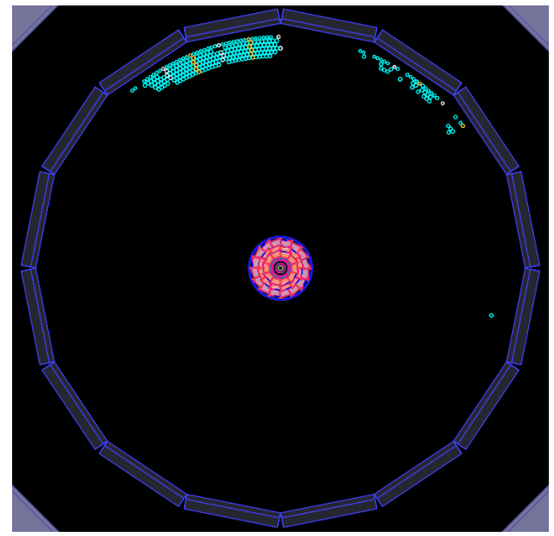
cross talk

- **study at test bench could not reproduce cross talk seen in the unit of FE board or signal connector**
- **Next to do**
  - analysis of cross talk hits; timing, FADC sum information, time over threshold (for FADC sum)
  - consider about threshold level for wire hit to suppress cross talk
    - it could be estimate using information analog/digital gains, FADC sum, time over threshold

noise study

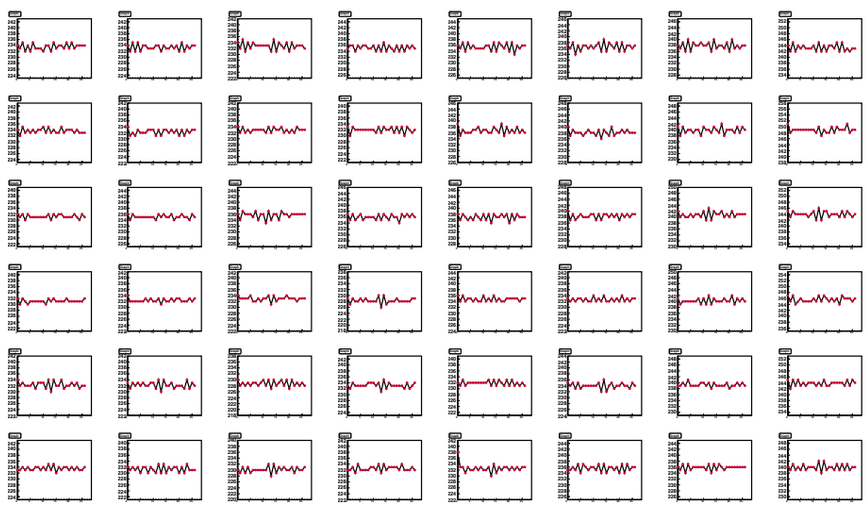
- **common noise hits in readout of outer layers**
  - it is appear on and off, not randomly



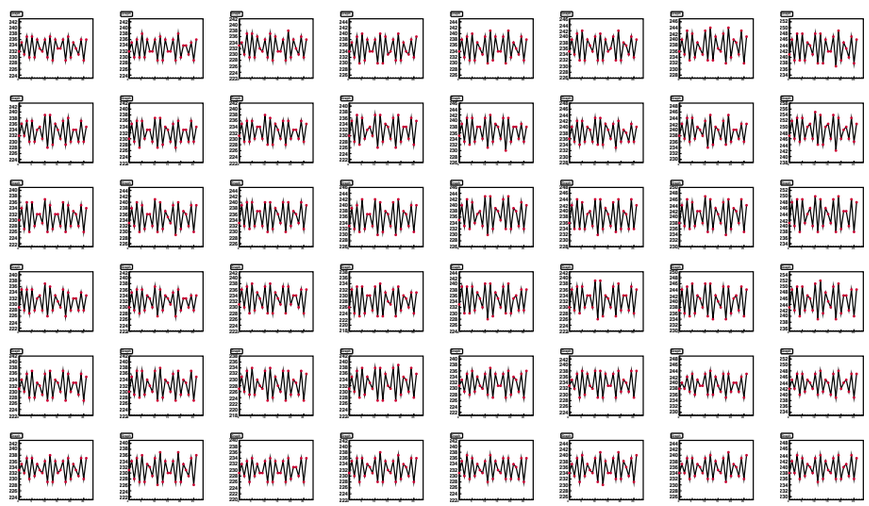


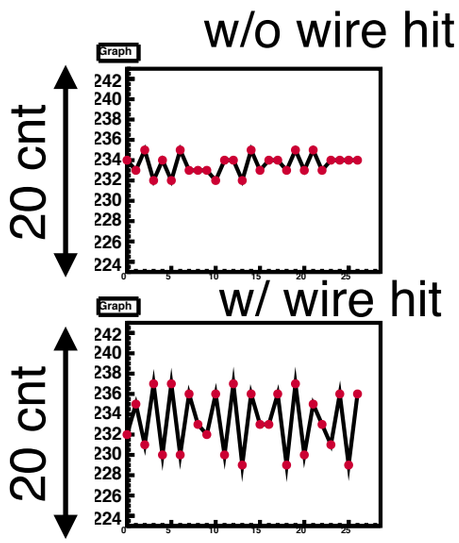
FADC waveform of pedestal data

board#256 event=2



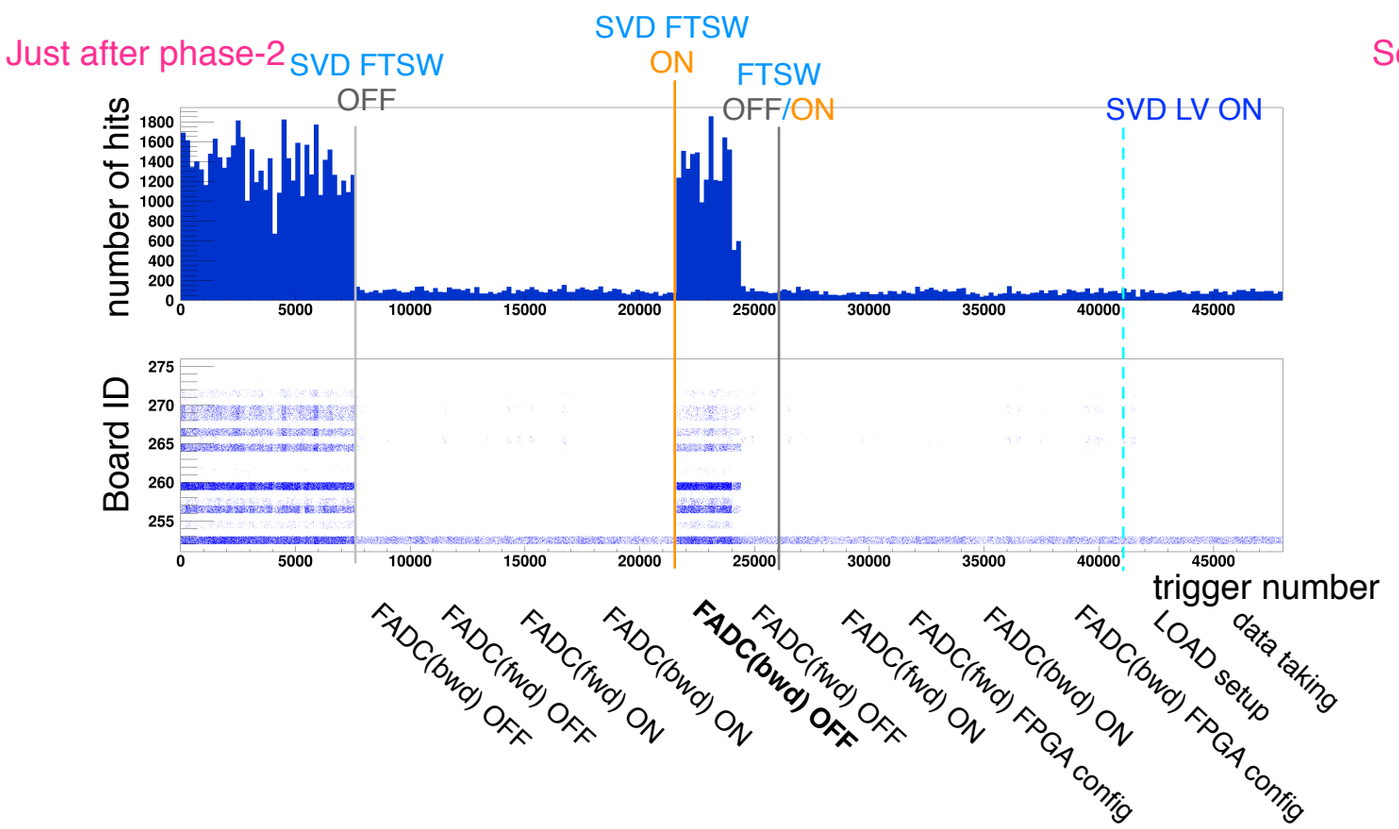
board#256 event=490

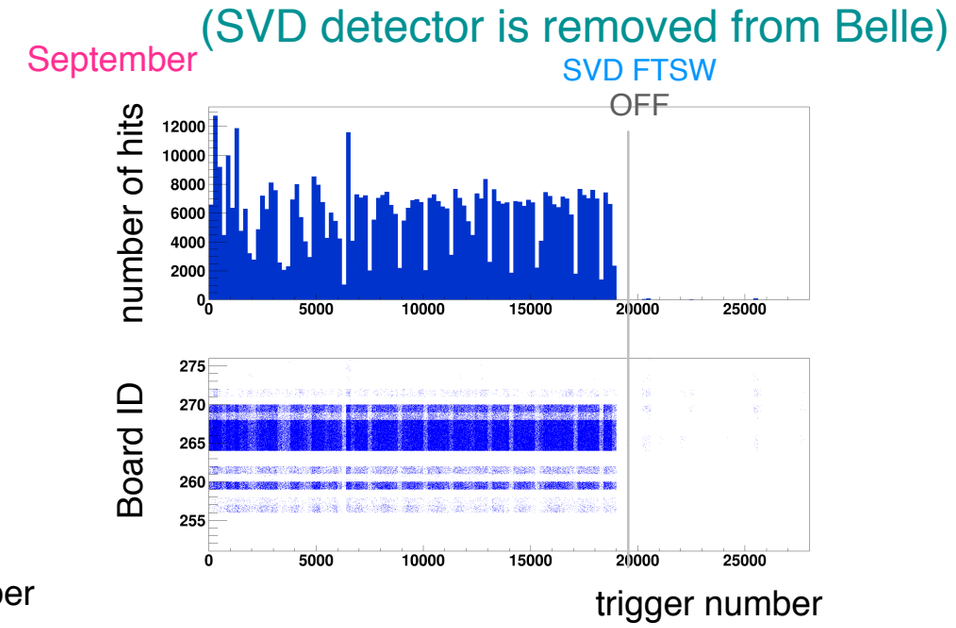




noise study

- **we perform survey relation with other sub-detectors**
- **Operation of crate for SVD FTSW located on roof of Belle structure seems to be related with CDC noise seen in outer layers**
  - it is hard to reproduce situation
  - continue to monitor and try to understand sources





for phase-3

- **adjustment of current limiter**
  - current limiter module decrease applying HV to keep leak current level
  - leak current range can be extended to be 500uA/layer from 50-100uA/layer
  - It should be determined by considering single wire rate
- **expert and operation shifters (still under consideration)**
  - ‘single points of failure’ should be solved
  - we will have training course in the coming global cosmic run
- **online and offline data quality check**
  - online data quality is checked by belle2 operation shifter
    - online DQM should be improved
  - offline data quality check is a task for CDC operation shifter

summary

- **CDC operation generally stable**
  - included in all luminosity runs
- **Hardware issues are mostly fixed**
  - all layers can be applied with nominal HV
  - FADC issue is mostly fixe
    - replacement of one or two more DC power supplies is desirable
  - DAC issues is fixed
- **Issues to be fixed before phase-3**
  - cross talk
    - further study of data analysis is need to understand
  - electric noise

backup

Hardware work during shutdown

- July : replace DC power supply for +2.0V to fix FADC error
  - worst boards (#52,53) is fixed
  - the power supply malfunctioned in September → removed and sent to company to repair
- July - Aug. : Ehut maintenance and power outage in KEK
- Sept. replace FE and investigate DAC problem
  - daytime : hardware work for HV and FE board, and study at test bench
  - night : HV and FE are ON to check status
  - check and replace TRG optical cable
- ~ 1 week in the end of Sept.
  - close both covers (Fwd/Bwd) and operating long time to check
- Oct. 2nd: VXD work around IR started
  - CDC is OFF during daytime for their work considering safety
  - CDC is ON 18:00 - 9:00

study for FADC error

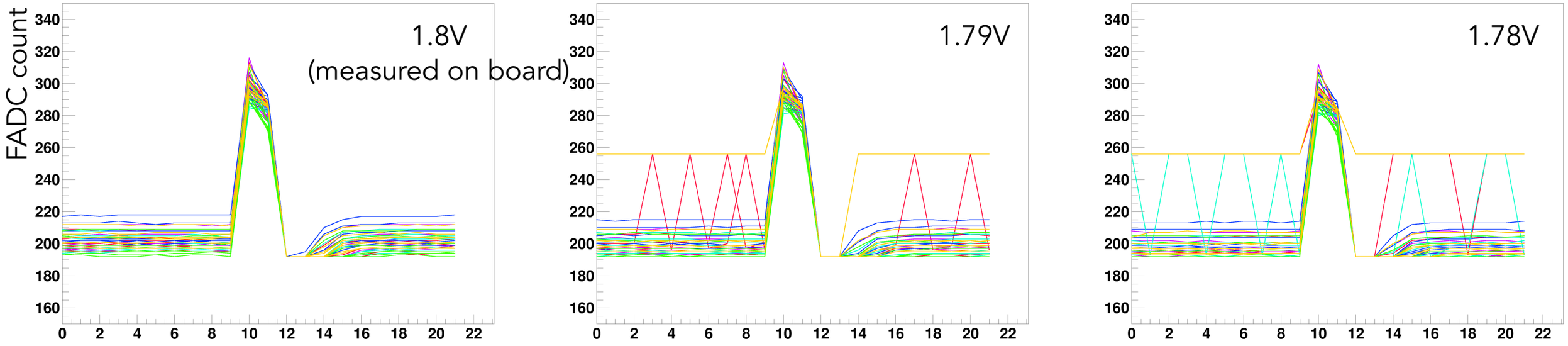
- FADC error is occurred in several FEs
  - inner FEs, far side from Ehut
  - reported at June 2017 and could not be fixed at 2017 summer maintenance
- lower supply voltage is a reason of FADC error
  - inner FEs, far side from Ehut : longer cable → larger voltage drop
  - +1V8 (1.8V) is supplied from regulator by +2.0V input
  - +1V8 is used for ADC
  - DC power supply operate with +2.8V(at Max)
    - [FYI] 12 DC power supplies for +2.0V: 11(max.+2.8V)+1(max.+3.5V)
  - Voltage drop is expected to be > 1V
- perform voltage supply scan for +2.0V at test bench

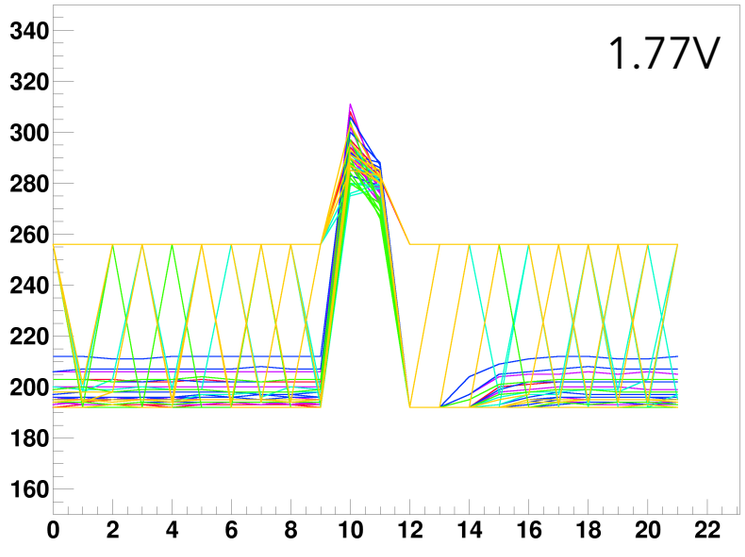
Nanae Taniguchi (181015)

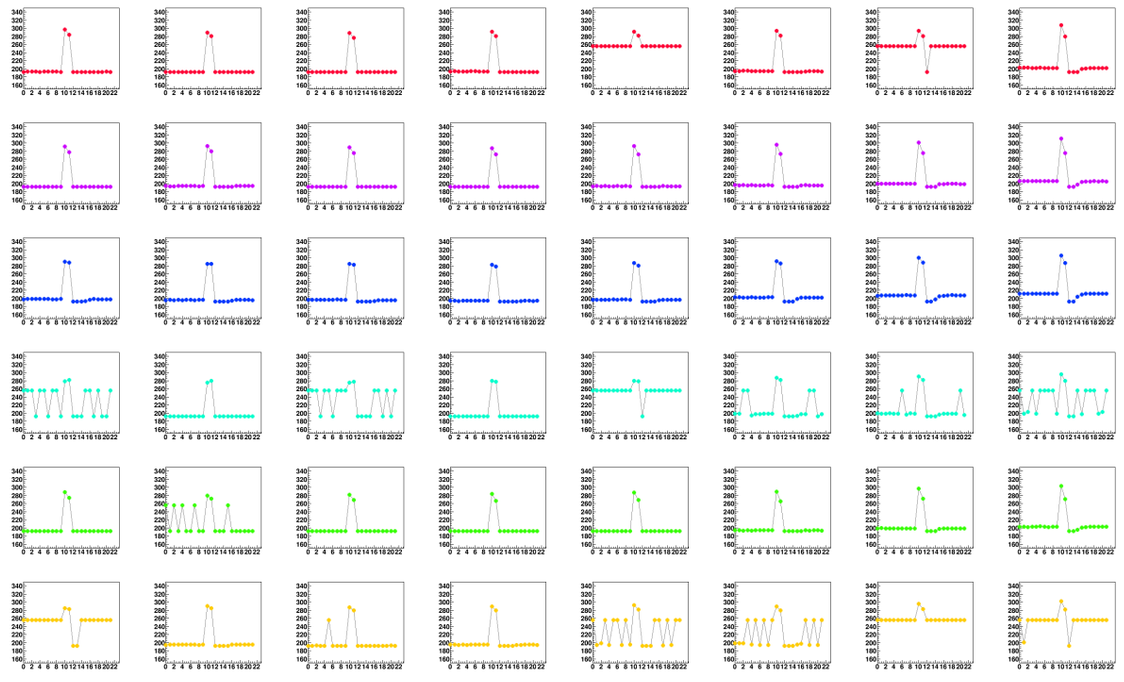
study for FADC error

Voltage supply scan for +2.0V

Overlay 48ch-test pulse waveforms for 1 event

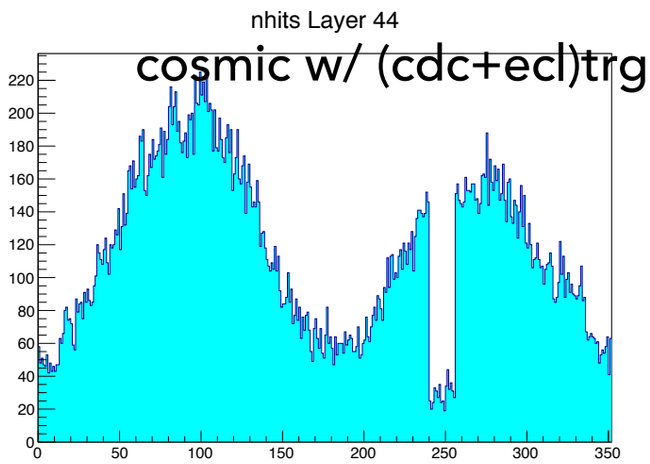






Chip or channel dependence is seen

DAC problem

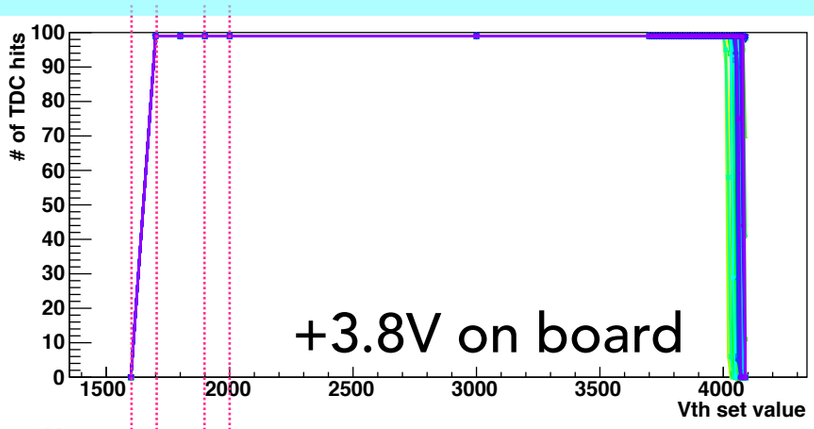


- DAC problem occurred for a few FEs
  - threshold does not work properly
- lower supply voltage is a reason of DAC
  - +5.5V is used for DAC voltage, but increasing apply voltage did not work
  - +3.8V is a source of this problem
  - +3.8V generate +2V5(+2.5V) and +3V3(+3.3V)
    - 2V5 can be monitored using FPGA function and voltage is enough
    - I have overlooked +3V3
  - +3V3 is used for VDDD : digital output of ASD
  - study at test bench can reproduce the problem

Nanae Taniguchi (181015)

DAC problem

threshold scan for TDC hits of test pulse (overlay 48ch)

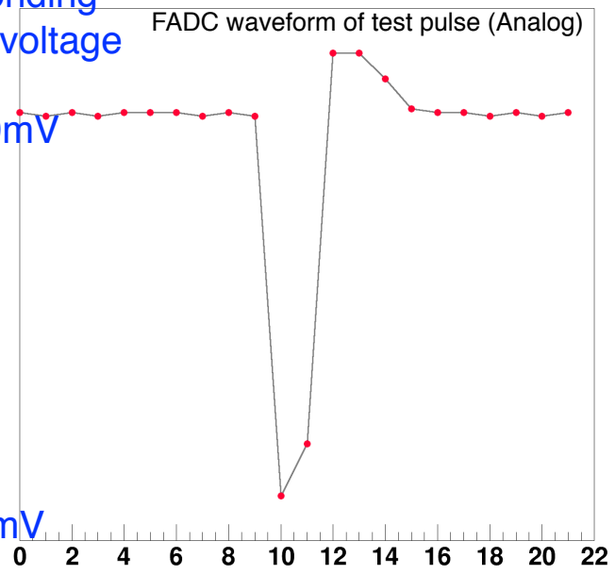


TDC hits with Vth=1700mV

No TDC hits with Vth=1700mV

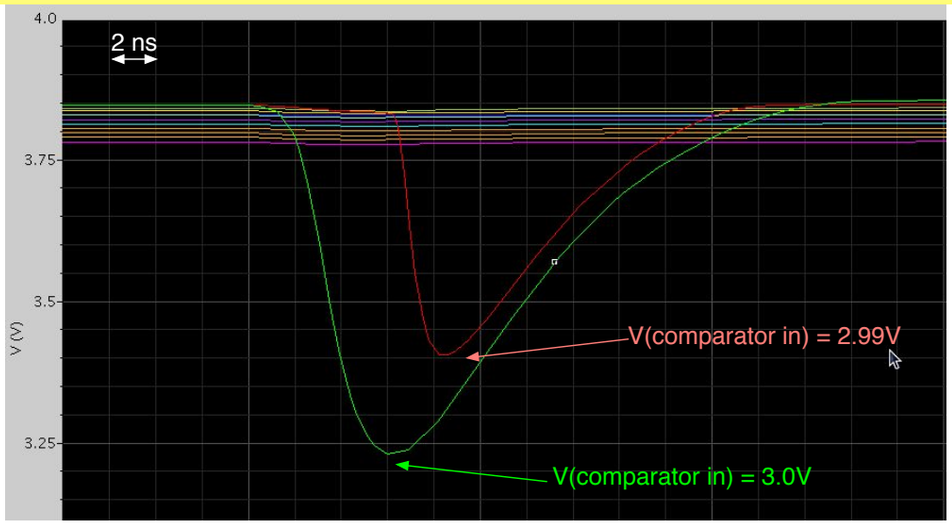
corresponding threshold voltage

~3800mV



(Analog output is not affected)

simulation for comparator. S. Shimazaki(KEK, e-sys)

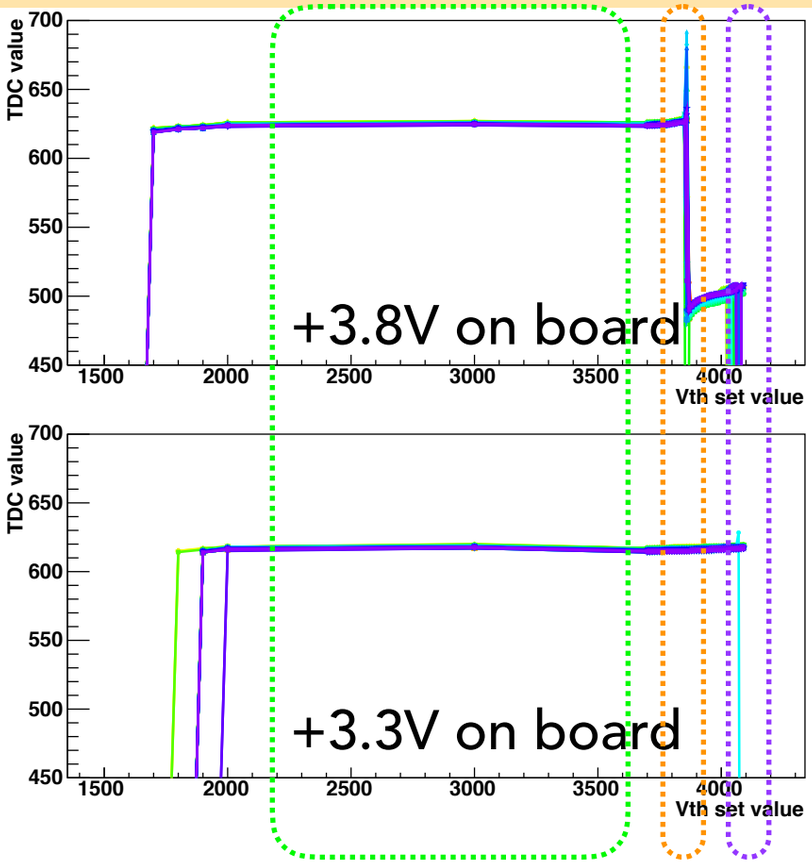


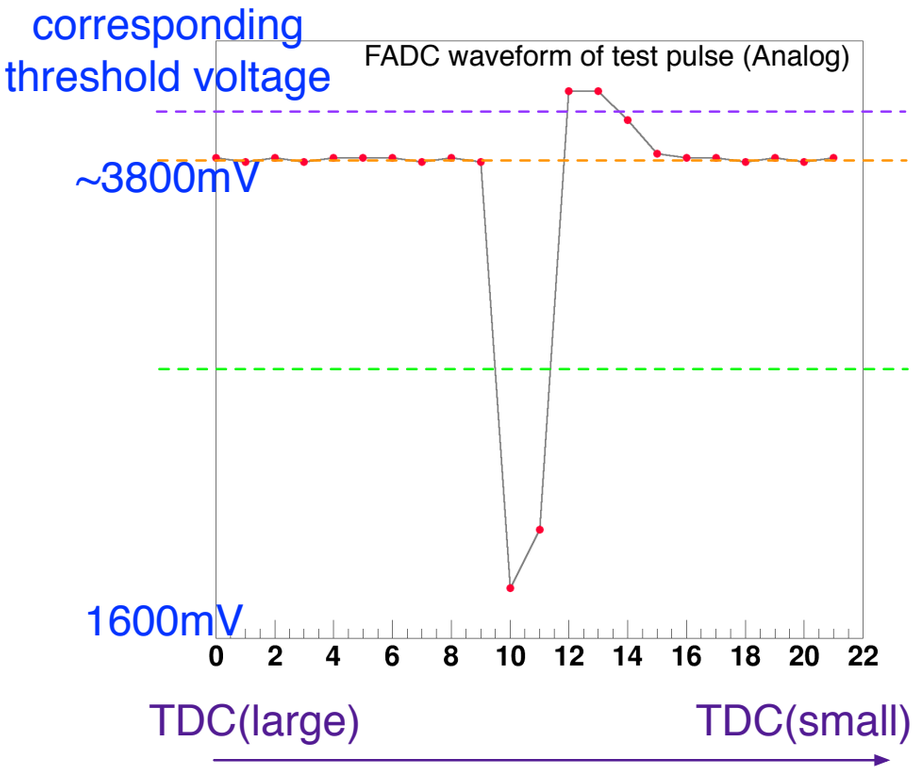
- Simulation for comparator
  - input charge is different from test pulse
  - digital gain decreased as input voltage of comparator decreased
- tried set lower threshold close to base line in cosmic run → # of wire hit didn't change
- problem is not only digital gain

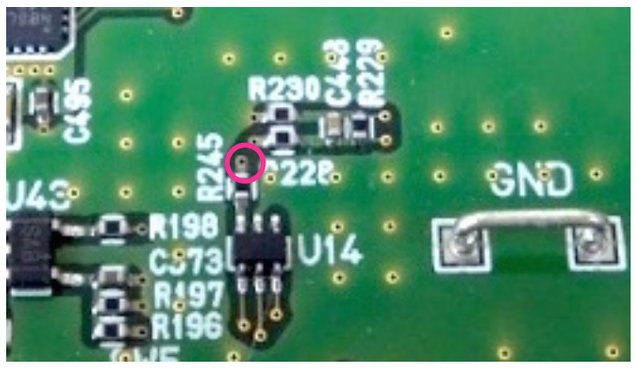
Nanae Taniguchi (181015)

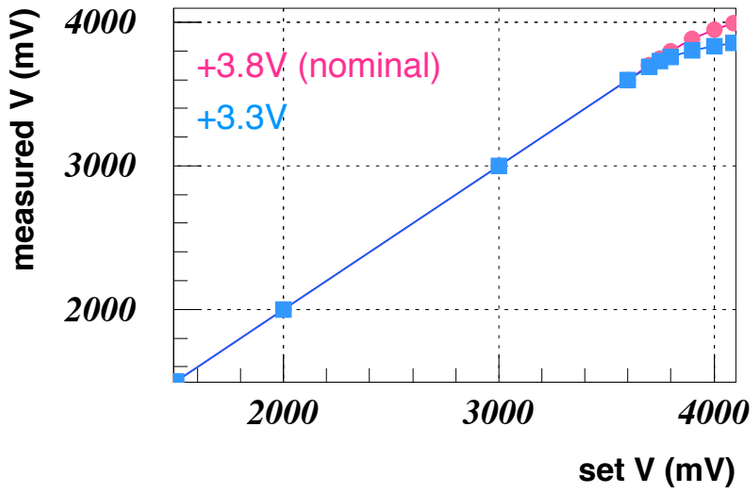
DAC problem

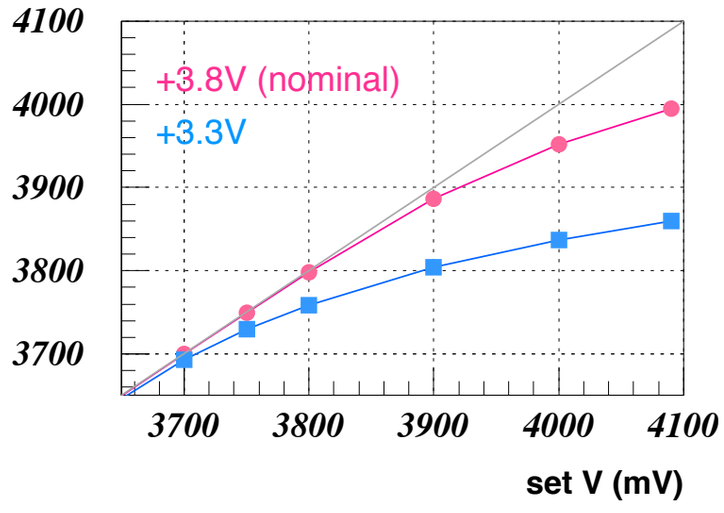
threshold scan for TDC value of test pulse (overlay 48ch)





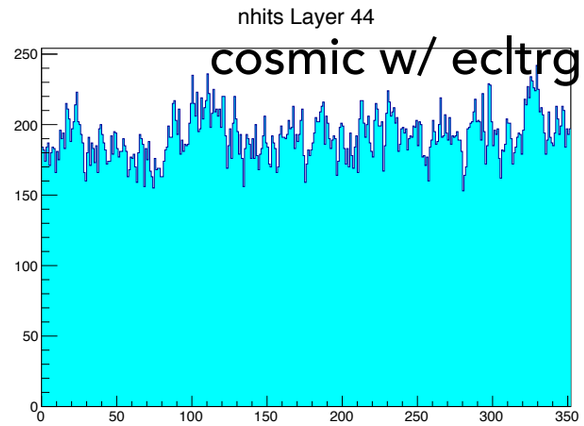


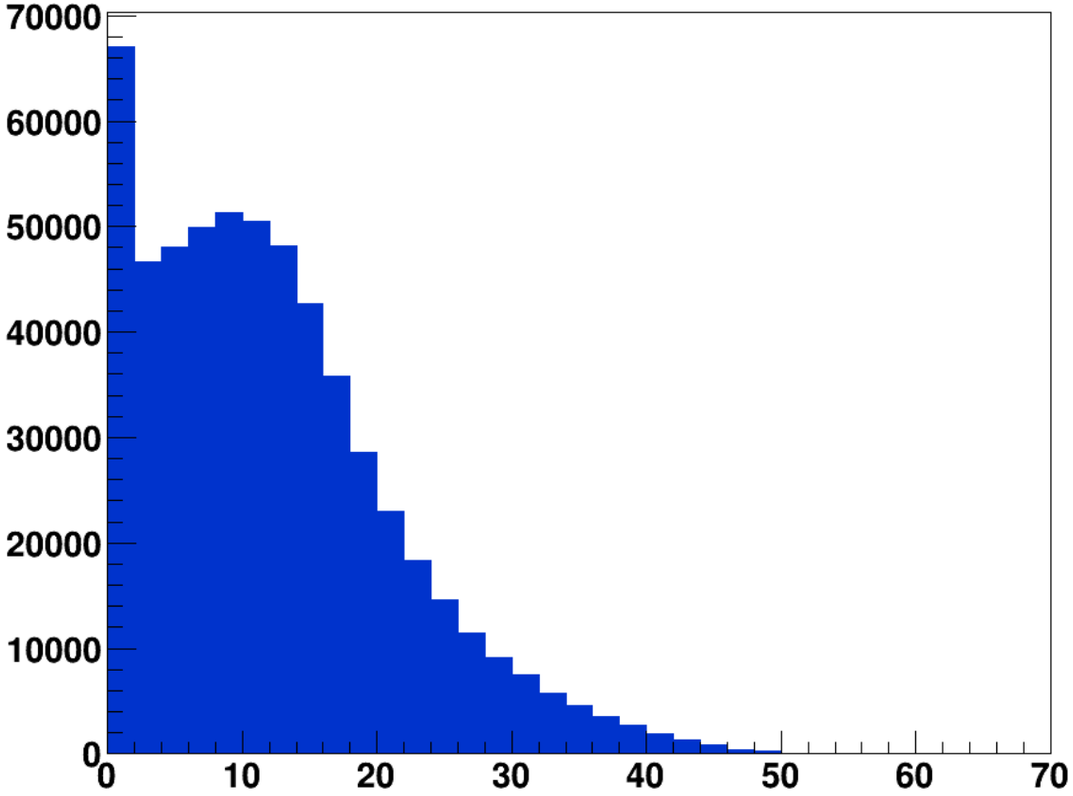




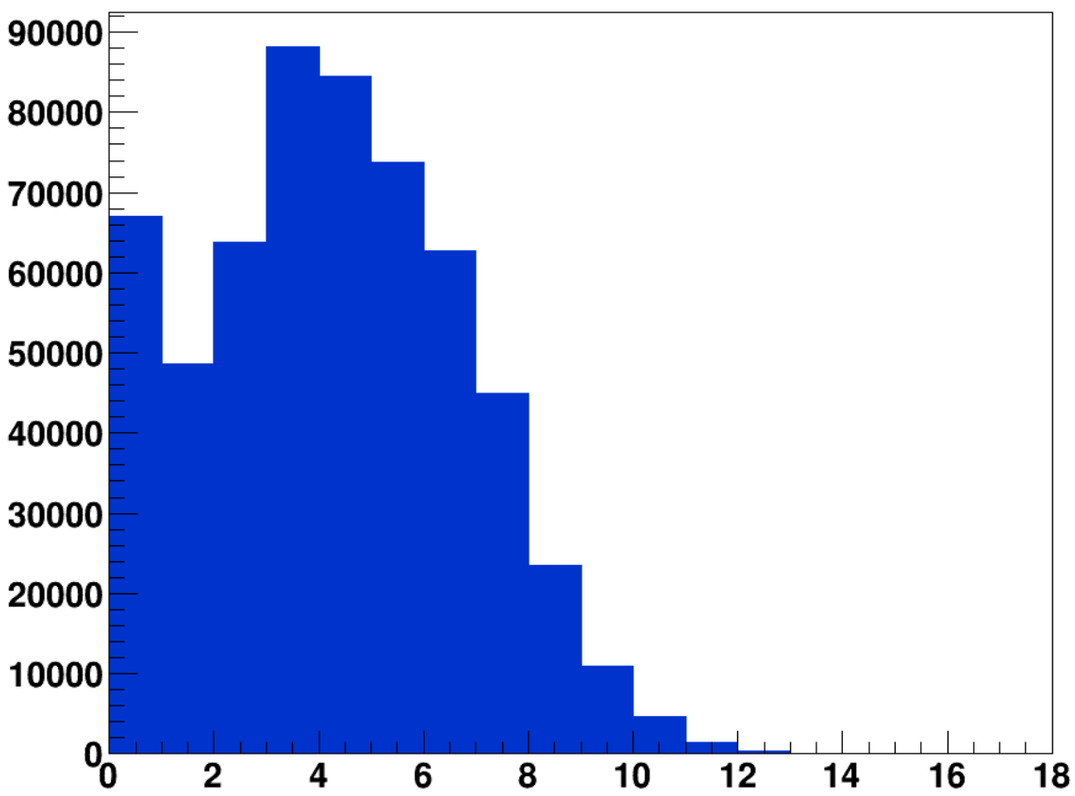
Error of FADC and DAC

- lower supply voltage is a reason
  - It was O.K just after installation, but some FE boards likely have been working with low voltage
  - power consumption may be increased
    - updates of firmware
    - aging ? ; mass production in 2014
- [DAC problem] replaced FEs board to check
  - test removed board at test bench. but there is no significant problem
- [DAC problem] increase voltage for +3.8V by 0.2V for corresponding FEs
  - DAC problem seems to be fixed so far
  - FADC error occurred in a few FEs with increased voltage of +3.8V. DC power supply for +2.0V need to be replaced with higher one to fix

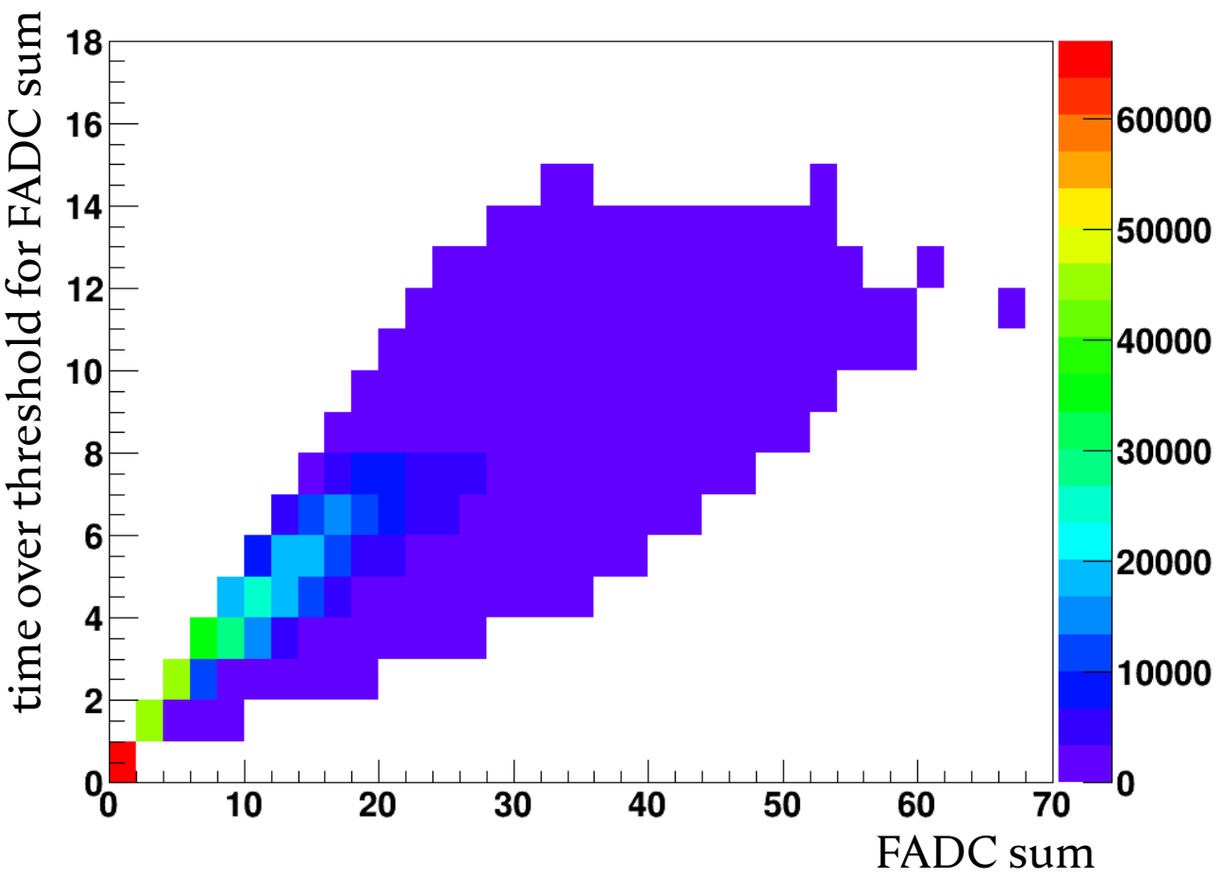




FADC sum



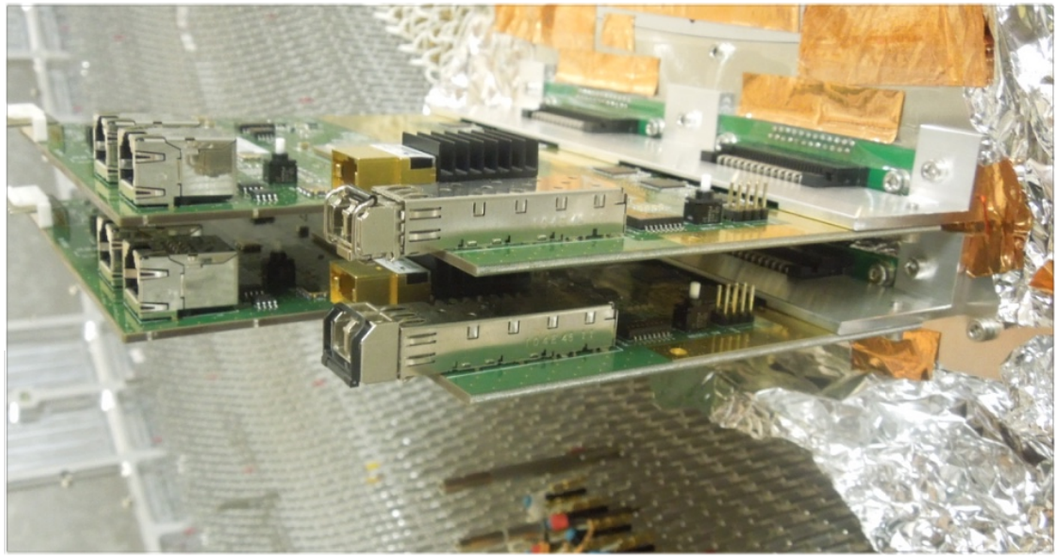
time over threshold for FADC sum

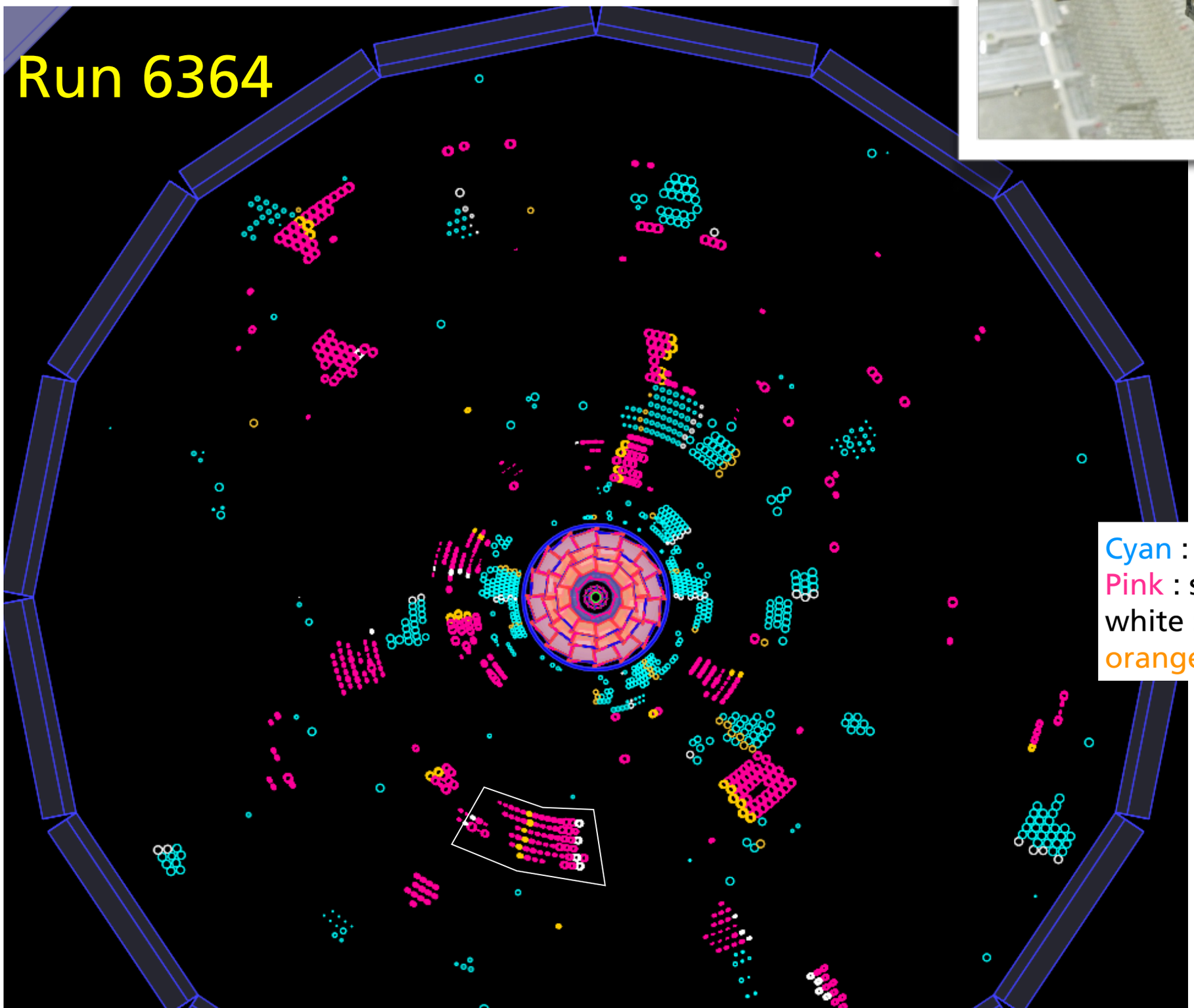


exp4, r1078
pedestal run for noise study

beam background data

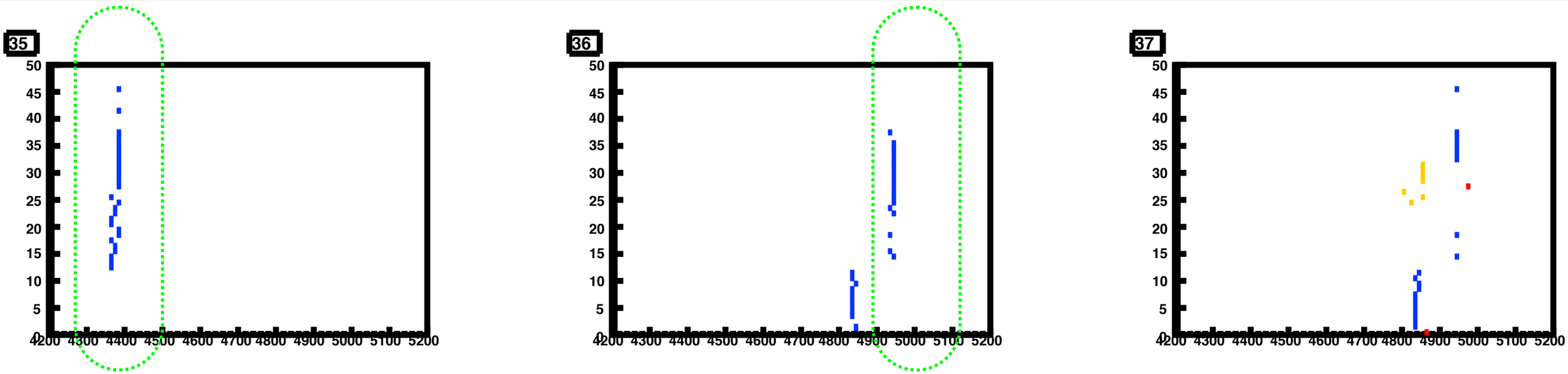
1 FE board read 3-layers X 16 cells
1-super layer is read by 2 FEs



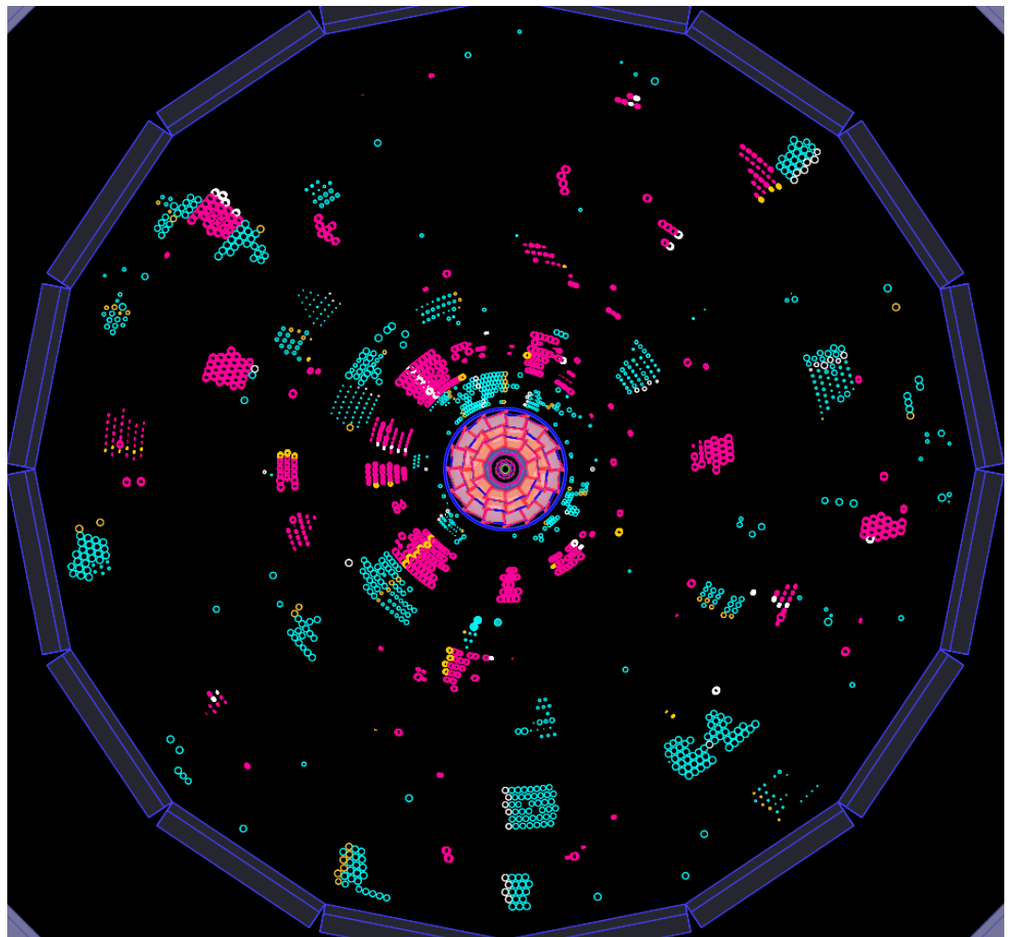


Cyan : axial
Pink : stereo
white : cell-ID%16=0
orange : cell-ID%8=0 && cell-ID%16!=0

X(horizontal) : TDC (nsec) 1 div = 10nsec
Y(vertical) : Channel ID of FE



Remarks: larger TDC value is corresponding to faster timing



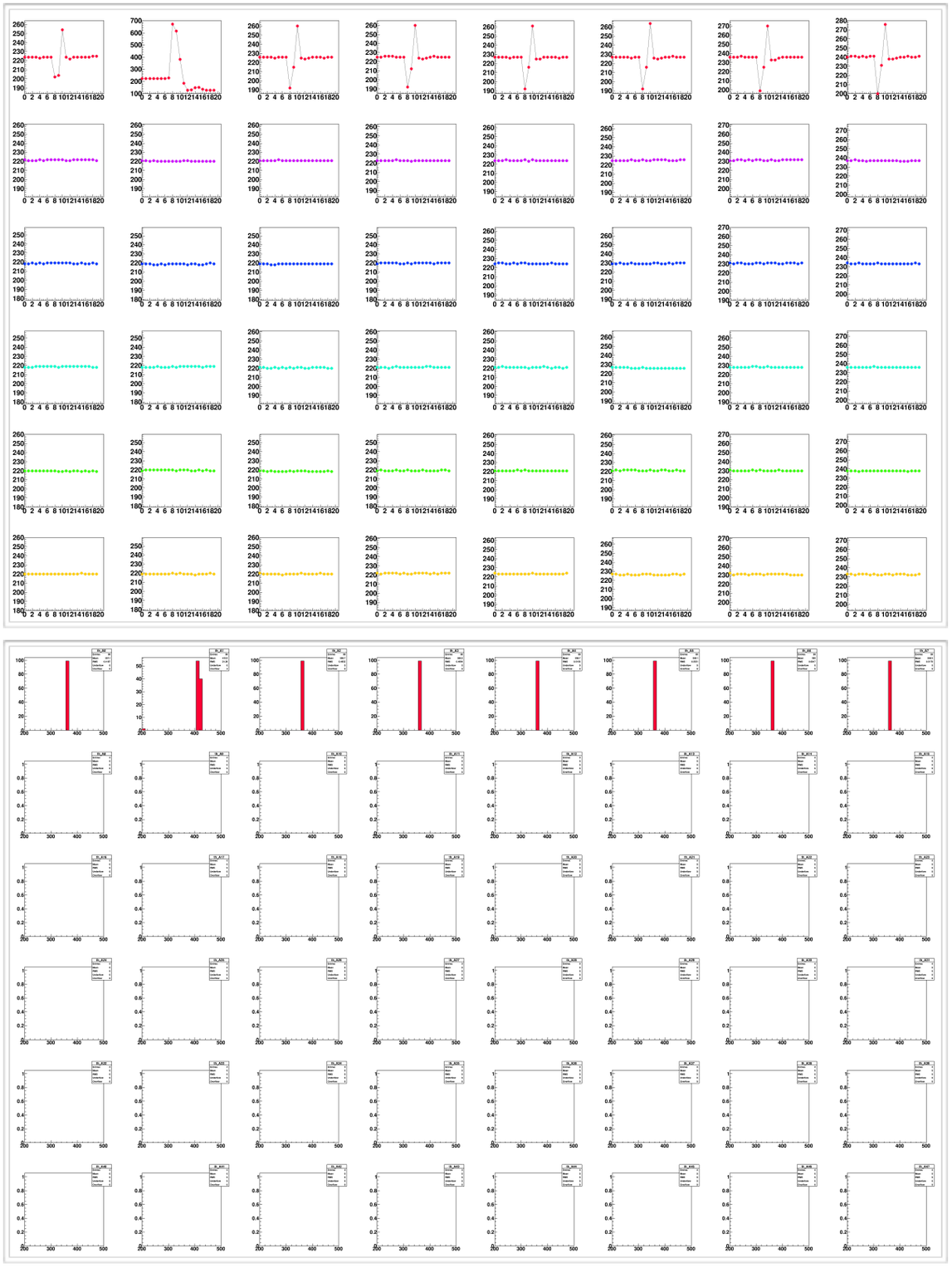
number of hits channel per board > 15
Blue : ADCsum<20
Orange : ADCsum>=20 && ADCsum<500
Red : ADCsum >=500

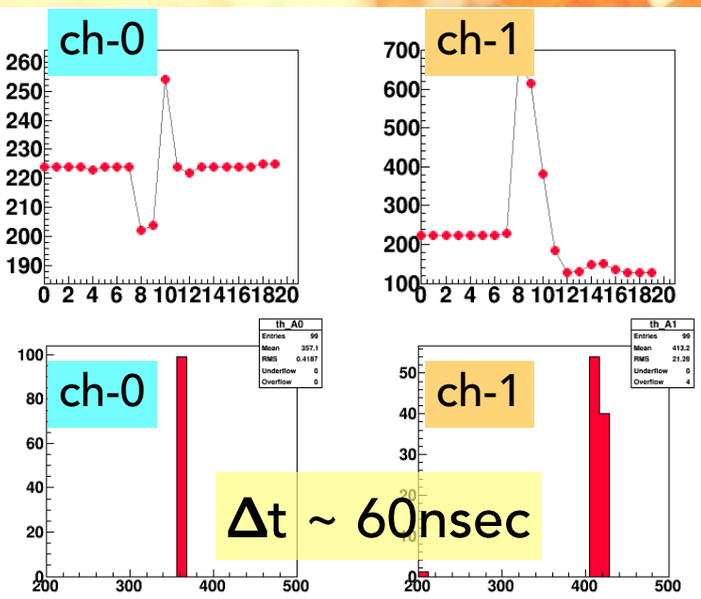
- Clusters are localized within the unit of readout board
- Most of hit channels have almost same timing and small charge

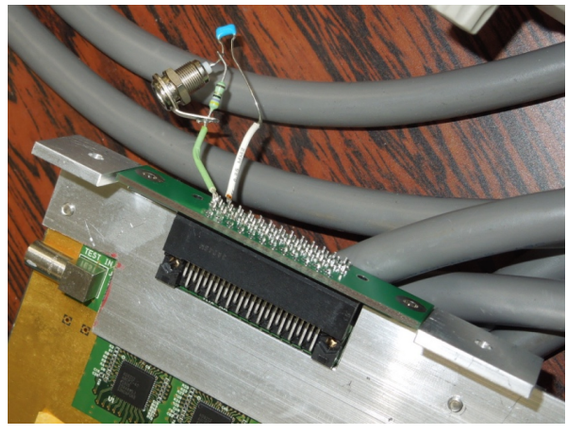
-> many hits come from cross talk

Nanae Taniguchi (181015)

cross talk study



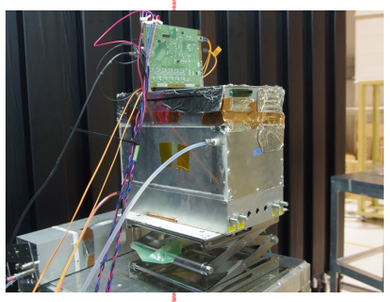


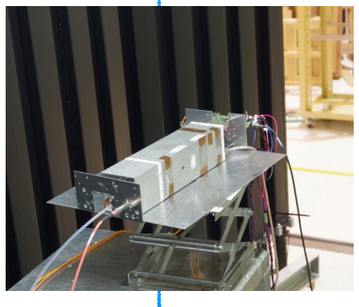


- cross talk study at test bench with spare board
- signal input into ch-1 from pulse generator
- Vth=3750mV (default)
- TDC hit due to cross talk is seen in the only same ASIC
  - input signal is large to see TDC hit with Vth=3600 in ch0-7

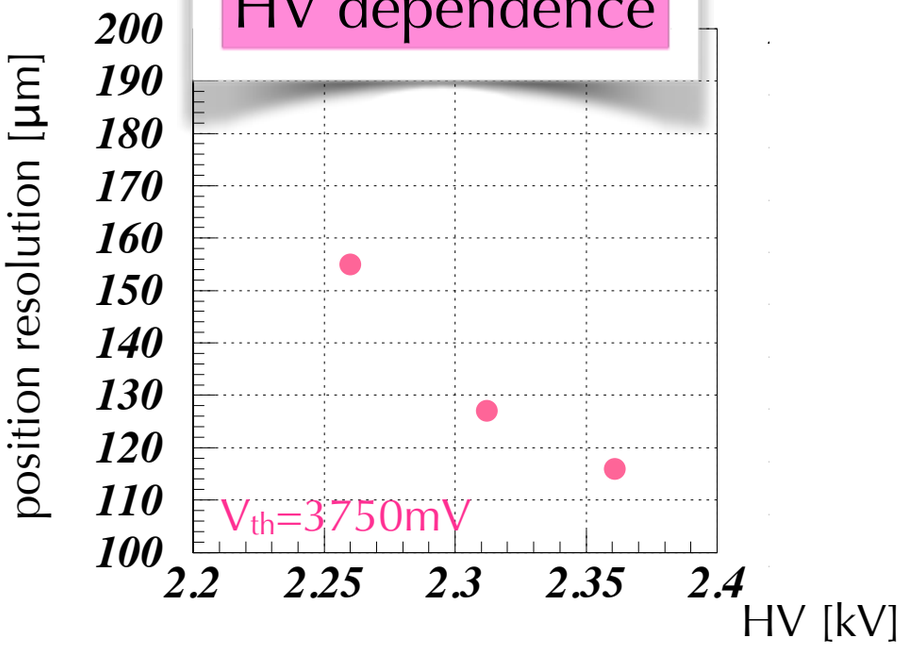
preliminary !!!

dependence on HV/V_{th}/incident angle

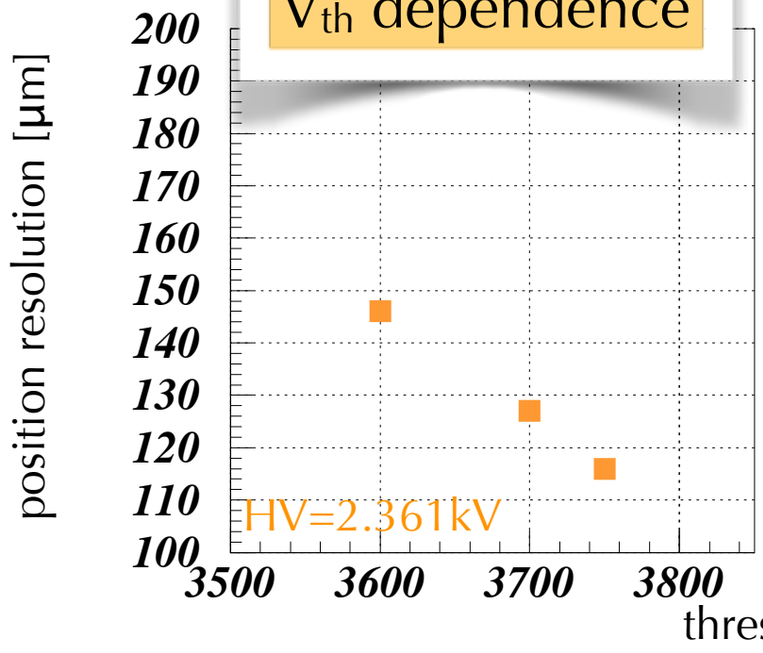




HV dependence

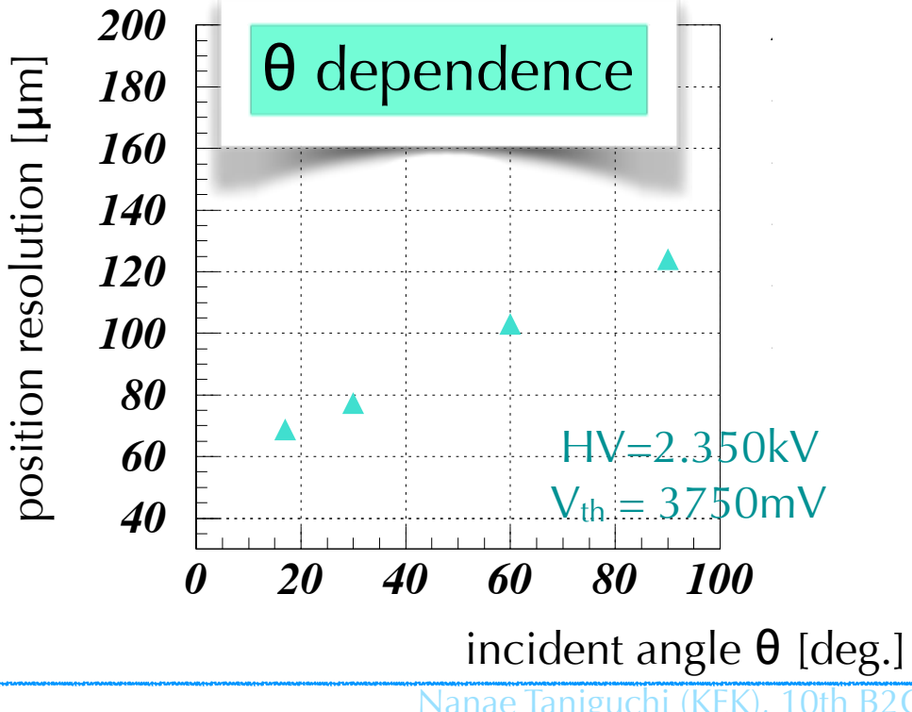


V_{th} dependence



baseline ~ 3850

θ dependence



θ dependence