Neurotrigger Trigger/DAQ Workshop 2019

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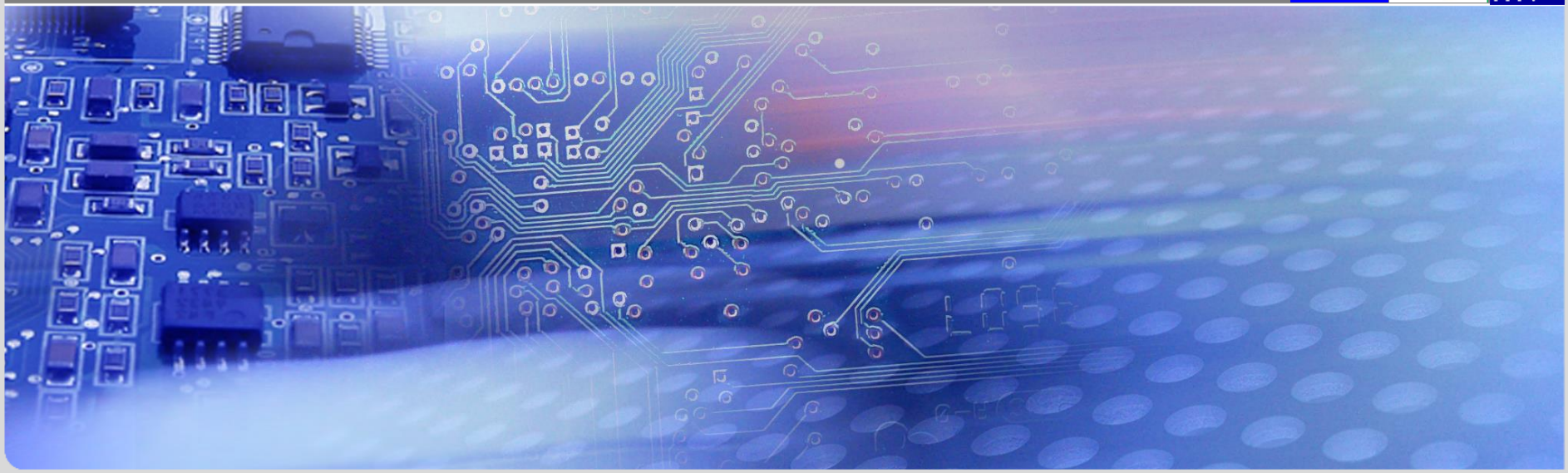
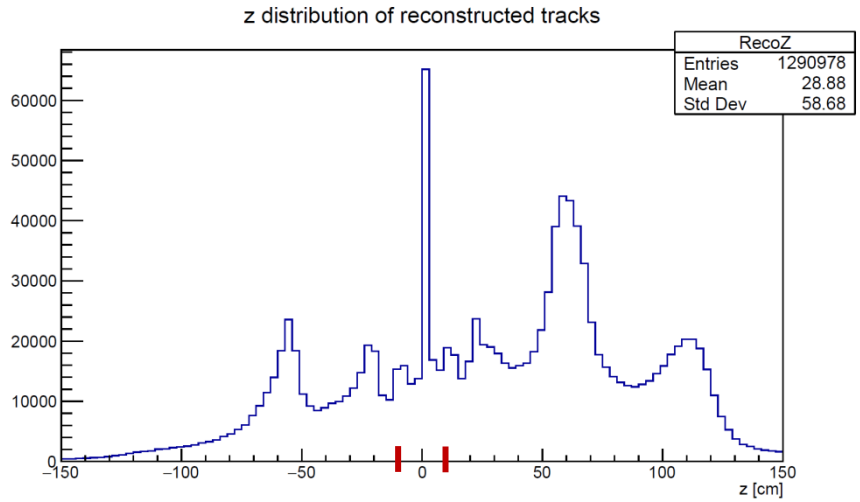
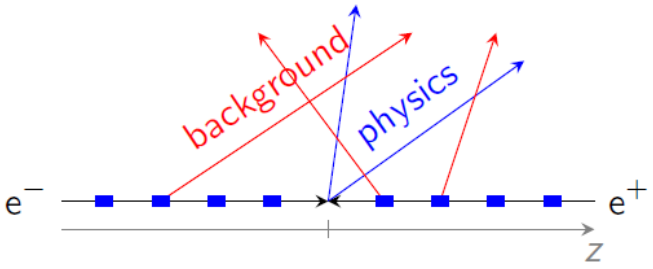


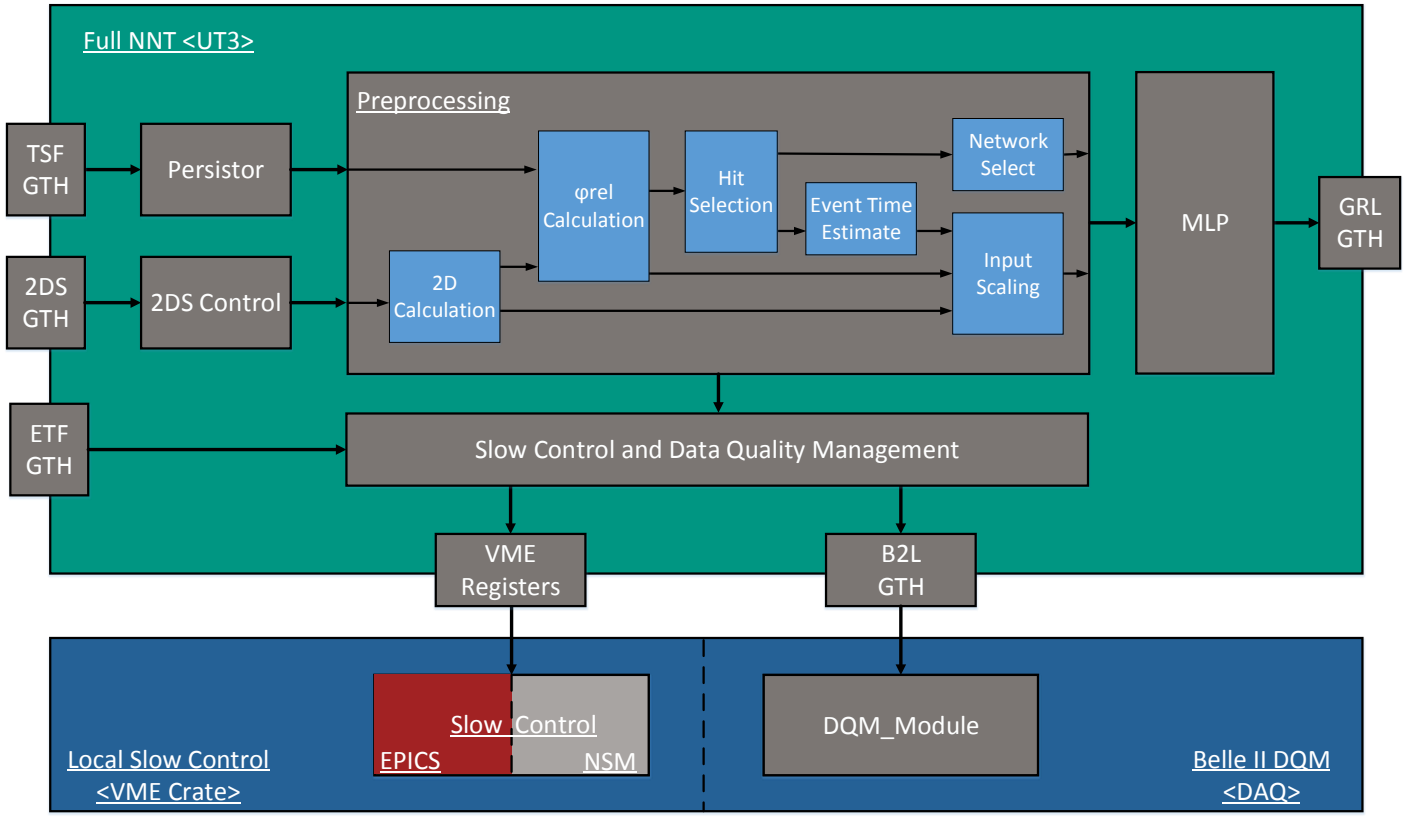
Neural z-Vertex Trigger

- Task :
  - Suppression of tracks outside of z=0
- Method :
  - Neural Networks using CDC data to estimate a tracks z-Vertex
- Implementation :
  - FPGA-based design fulfilling real-time requirements



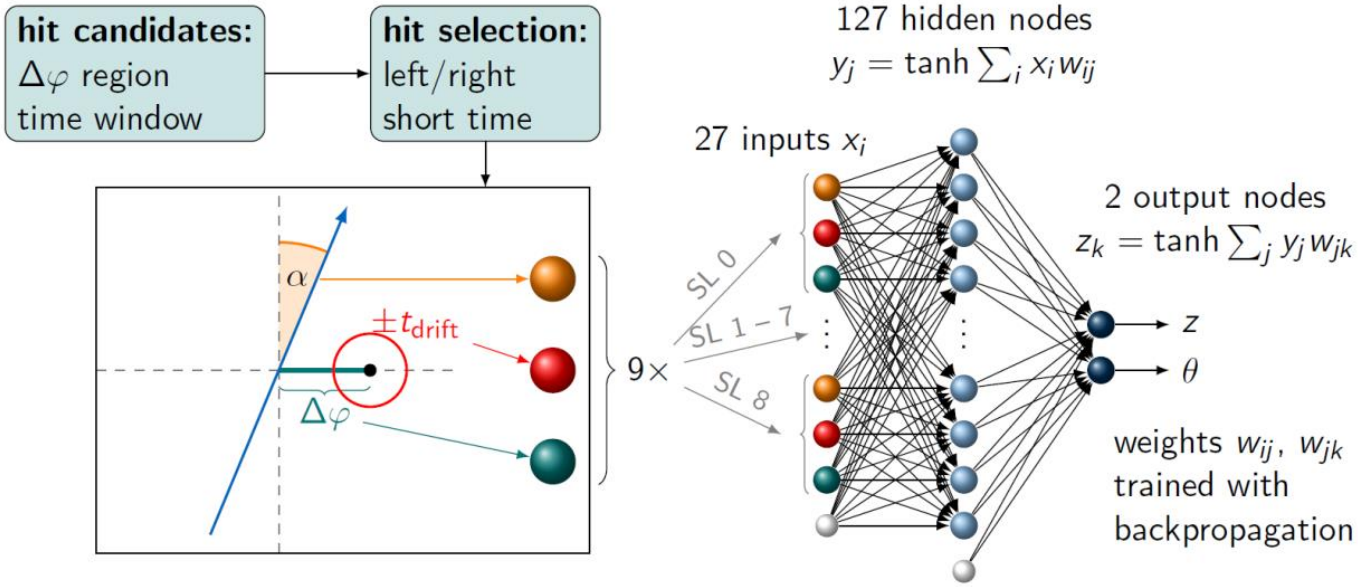


General Architecture



Neural Network approach

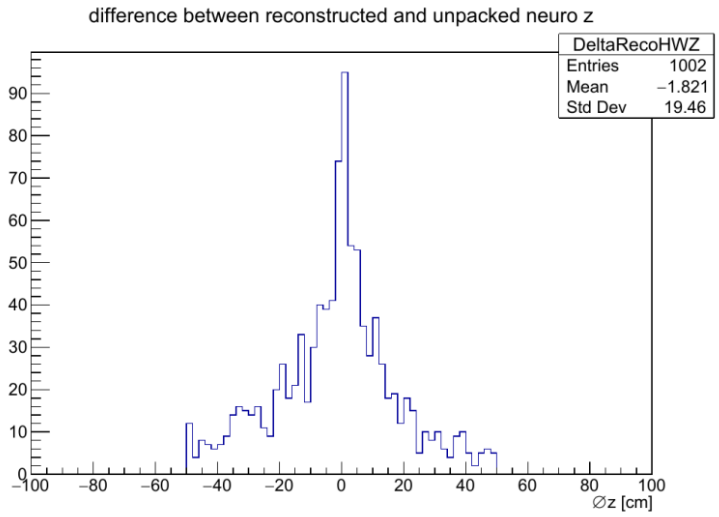
Name	Description
α	Crossing angle of the track relative to the normal of the crossing point of the track with the circular path of the layer.
$\pm t_{drift}$	Drift time of the TS. The sign indicates the direction of the passing particle either left or right. It is not used in case of an unknown direction.
φ_{rel}	Azimuth angle of the particle relative to the angle of the sense-wire.

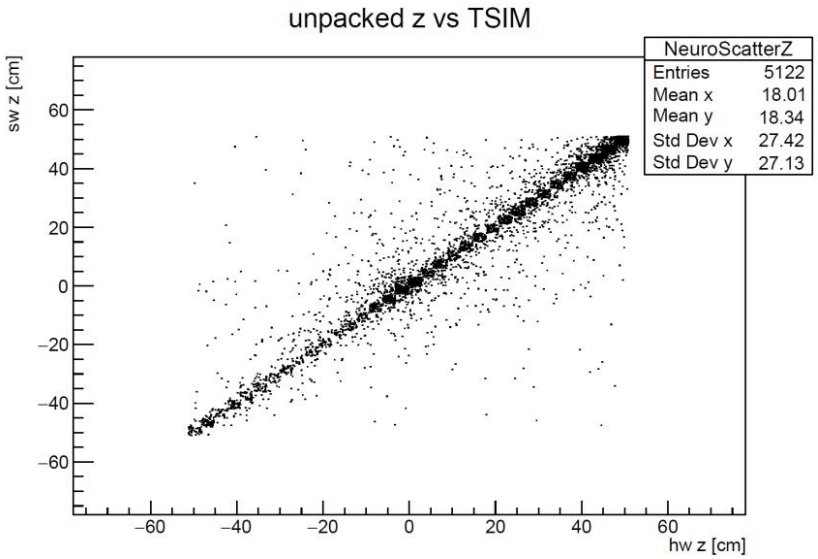


Current Status

- Full Implementation
  - Tests during Phase 3 in june
  - Recent Tests in august

- During the end of june runs large scale correctness of the firmware was achieved

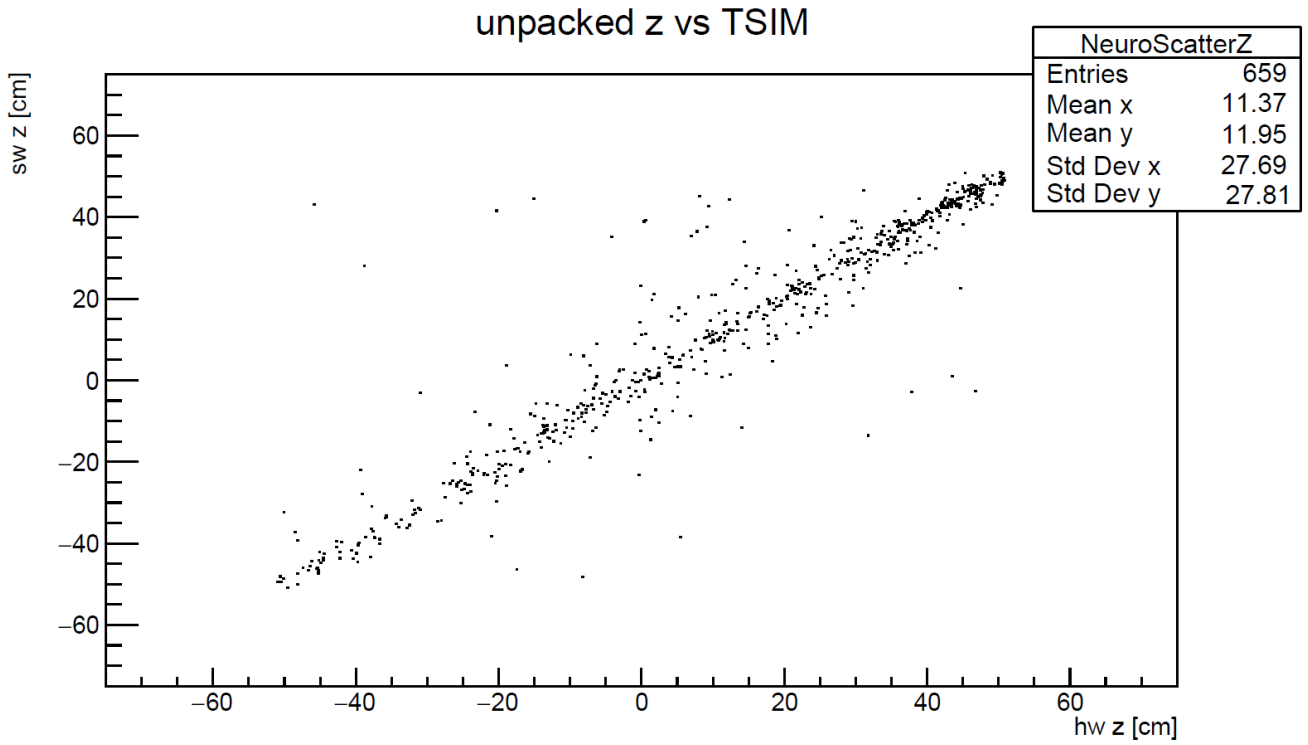




Current Working States

- Switch to cosmic networks for current tests

- B2Link format has some bugs in timing, data at wrong clock cycles



Additional Status

- Firmware using 15 TS is available for testing
  - 2k B2L Buffer, not the extended buffer

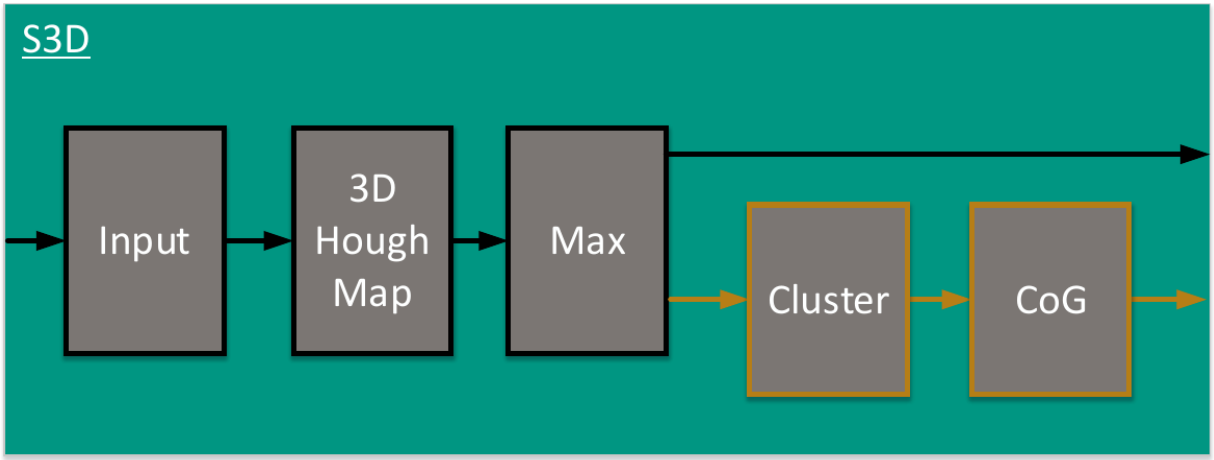
3D-HOUGH FINDER PREPROCESSING

3D-Hough Finder

- Preprocessing to improve neural z-Vertex Trigger performance
- 3D-Hough finder using the CDC with weighting based on Bayes Theorem
- Implementation :
  - FPGA implementation on UT4 (new FPGA Platform)

Implementation Approach

- 2 Phase implementation
- Phase 1 : Hough-Map and maximum finding (ready)
- Phase 2 : Clustering + Center of Gravity (in development/prototypical)



Simplified System Results

- Phase 1 Setup :
  - Platform : UT4 (XCVU80)
  - LUT 35% Resources
- Phase 2 Clustering Add-on :
  - 3D-Clustering Only
  - Platform : UT4 (XCVU80)
  - 5 % LUT ; 6 Clock Cycles Processing
  - CoG missing

FPGA Integration

- 3D-Hough and neural z-Vertex Trigger potentially implemented on the same FPGA

FPGA	Resources	DSPs	Networks
VU80	~70 %	50%	1
VU95	~50 %	35%	1
VU125	~50 %	50%	2
VU160	~30-40 %	60% / 80%	3 / 4
VU190	~30%	67%	4
VU5P	~50%	35%	4

Best Option is VU5P; best option due to spare resources
Price is 15k$ for -1Speed, -2 Speed 22k$
Check if compatible; packages is compatible (FLVB2104E / VU125 Option)

THANK YOU

FOR THE INTEREST IN THE NEURAL Z-VERTEX TRIGGER