Status on ECL trigger

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TRG/DAQ workshop
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Contents

- Recent HW and FW update
- Recent ETM FW update
- Status of 3D Bhabha veto to 2D
- TC timing problems
- Summary

Recent HW and FW update

- Frequent ttlost on 1 FAM
  - Fixed by replacing LAN(FTS-FAM) to next FAM
  - essential reason of ttlost is unknown yet

- 4 jumpers on Shapers were re-configured by Yuriy.
  - 3 by request from ecltrg for CC, 1 due to cut of 1 unstable pre-Amp
  - Calibration w/ test pulse needed, and w/ beam data later on.

- TC532(FAM47 ch10) was very unstable from April.
  - Recovered by fixing cable(FTSW-FAM) connection

- FAM CPLD and MCU firmware update and downloading at detector
  - all 3 TCP/IP PORTs are available for full operation as original plan
    - 2 for SLC, 1 for CUI
    - TC waveform extraction is possible by any PORT
  - essential reason of TCP/IP communication error is unknown yet
    - In the most of cases, MCU FW download can fix now.
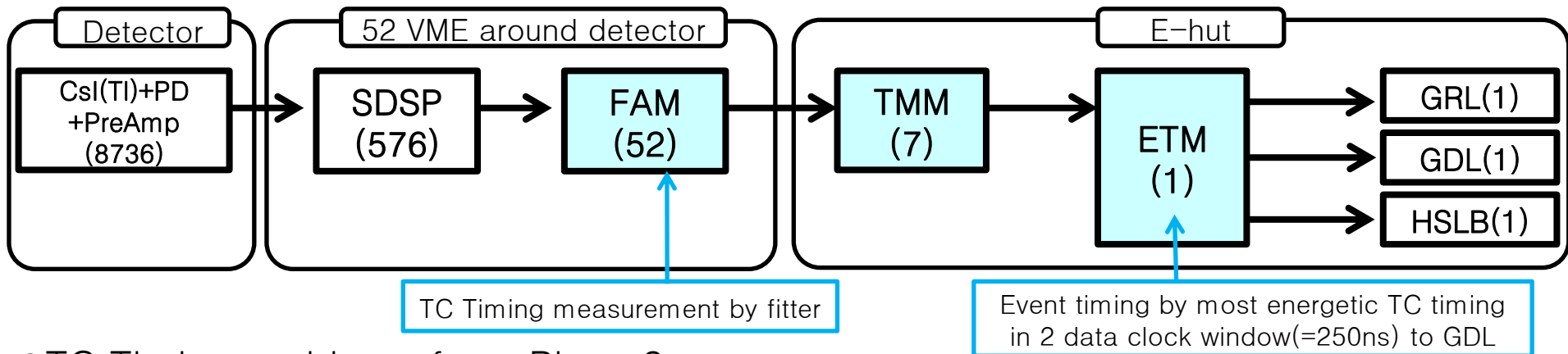
Recent ETM FW update

- Update logic to issue trigger to FTSW64 for "local" cosmic run
  - Timing peak in ECL is at T=0 with much better resolution than before
  - Local cosmic data became more reliable.

- ETM-GDL GTX → GTH to avoid instability of GTX protocol on GDL
  - Stability check at GDL side will be started after summer shut-down

- ecl_bst (Etot in θID=1-17 > 20GeV)
  - To avoid ERROR in ECL readout by vetoing "ECL burst" events
  - Inconsistency between ECL and ecltrg found → Sunghyun talk
  - ECL is developing FW to avoid the ERROR w/o ecl_bst veto trigger

- 3 cluster trigger bit (ImI0) → Highest trigger rate in ecl trigger
  - New 3 cluster trg(ImI11) proposed by Chris, and FW is ready.
    - Trg rate to 1/4, and $\varepsilon(\tau)$ to 87.6% from 89.5%
    - τ group is checking if it's ok or not.
  - L1 will be issued by "ImI0.OR.ImI11" during autumn run

3D Bhabha veto bit

- 3D Bhabha logic is available on GDL during Phase2.
  - logic worked as expected, proved by firmware and tsim.
  - Attenuator coeff. became much stable in Phase3 than Phase2.
- 2D is used in GDL, but 2D and 3D Bhabha recorded w/o pre-scale
- Iwasaki-san requests an approval from belle2 collaboration based on real data to replace 2D with 3D.
- Asking the approval for physics groups.
  - JIRA ticket(https://agira.desy.de/browse/BIIOPS-8)
  - Chris quickly checked data
    - Efficiency check using tight selection used for ecl calibration

    > I selected 71,465 Bhabhas (cross section 30 nb). 98.9% were identified as 2D Bhabhas, and 97.2% as 3D Bhabhas. There are 4693 gamma gamma events (2 nb); 96.9% marked as 2D Bhabhas, and 97.2% as 3D Bhabhas. Both vetoes are performing well at identifying these events.

    - For ππγ

    > Conclusion is the same as that reached by Maeda-san, that the 3D veto is better at retaining this physics process than the 2D veto.

  - τ group approved
    - https://agira.desy.de/secure/attachment/29730/29730_Tau_L1BhabhaVeto_28June2019.pdf
  - Waiting for approval from low multi and dark sector physics group

TC timing problems

Detector	52 VME around detector		E-hut	

```
Detector          52 VME around detector              E-hut
┌─────────┐      ┌──────────────────────┐    ┌──────────────────────────┐   ┌─────────┐
│CsI(Tl)+PD│  →  │ SDSP  →  FAM         │ →  │ TMM   →   ETM            │→  │ GRL(1)  │
│ +PreAmp  │     │ (576)    (52)        │    │ (7)       (1)            │   ├─────────┤
│ (8736)   │     │                      │    │                         │→  │ GDL(1)  │
└─────────┘      └──────────────────────┘    │                         │   ├─────────┤
                                             │                         │→  │ HSLB(1) │
                                             └──────────────────────────┘   └─────────┘
```

TC Timing measurement by fitter

Event timing by most energetic TC timing
in 2 data clock window(=250ns) to GDL

- TC Timing problems from Phase2
    - ① run by run TC timing shift due to
        - A) Wrong LUT for bitslip and tap on FPGA
        - B) Improper clock setting to capture ADC data on FPGA
        - C) Auto-reboot function in MCU
        - ➔ All fixed, TC T calibration is possible. Actually YJ got nice result.
    - ② Large TC timing resolution than expected
        - $\sigma(T)\sim$6ns in data, but ~1ns in tsim
        - ➔Ongoing
    - ③ TC timing bias from fitter on FAM
        - ~5ns shift as function of energy (+ noise)
        - ➔ not started yet
- 8ns event timing shift ➔ due to GDL(?)+FTSW(?)
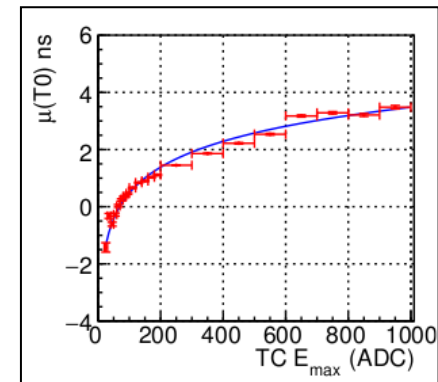
Large TC timing resolution

- tsim shows TC timing resolution is around **1ns** for Bhabha sample
- Offline eventT0 shows around 5ns. Why ?

- Xtal channel by channel timing differences were confirmed w/ test bench
    - Both shaperDSP and (cable+PreAmp) have large timing differences

- Anyway, no way to avoid in online trigger.
- Need to update tsim-ecl to take into account this effect…

- Check TC timing resolution by implementing ECL T CC into tsim-ecl
    - $\sigma(T)$ in tsim << data, still
        - (probably) effect on T from fast and slow shapers are different
    - Same test will be done using T CC from ecltrg data by test pulse

- If possible, check xtal ch by ch timing variations using beam data

Summary

- Many updates and progress in HW, FW, and understanding for problems since last b2gm

- Plan before (or during) autumn run
  - Noise check mainly for endcap (currently disconnected)
  - Fix TC timing related problems
    - variation in each Xtal ch. In tsim
    - bias from fitter
  - (Hope to) get an approval for 3D in September from physics coordinator.
  - ...

backup

ShaperDSP effect on timing

PreAmp

PreAmp

Shaper(ref)

Shaper(A)

FAM

Collector
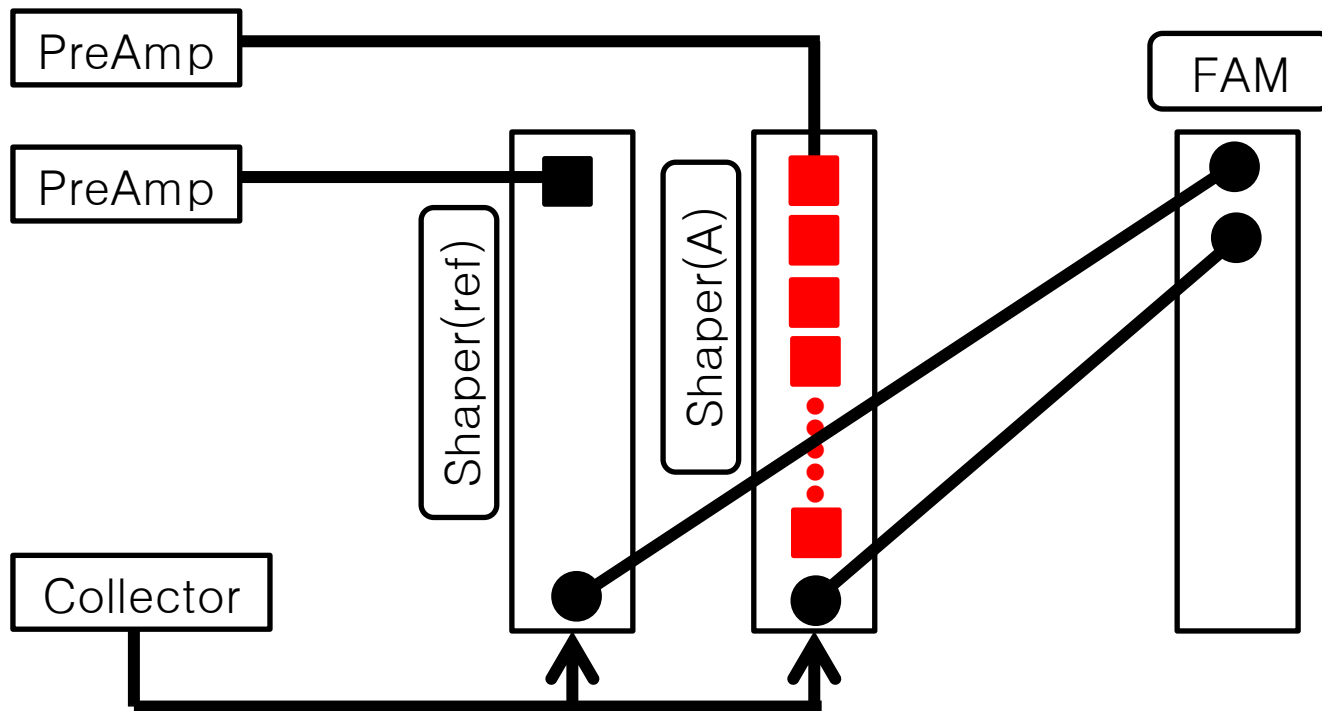
- All setup(module, cable, connection) are fixed, except for
  - Cable connection to ch#1, to #2,···#16 on ShaperDSP(A)
  - Also replace ShaperDSP(A) to (B), (C)

ShaperDSP effect on timing
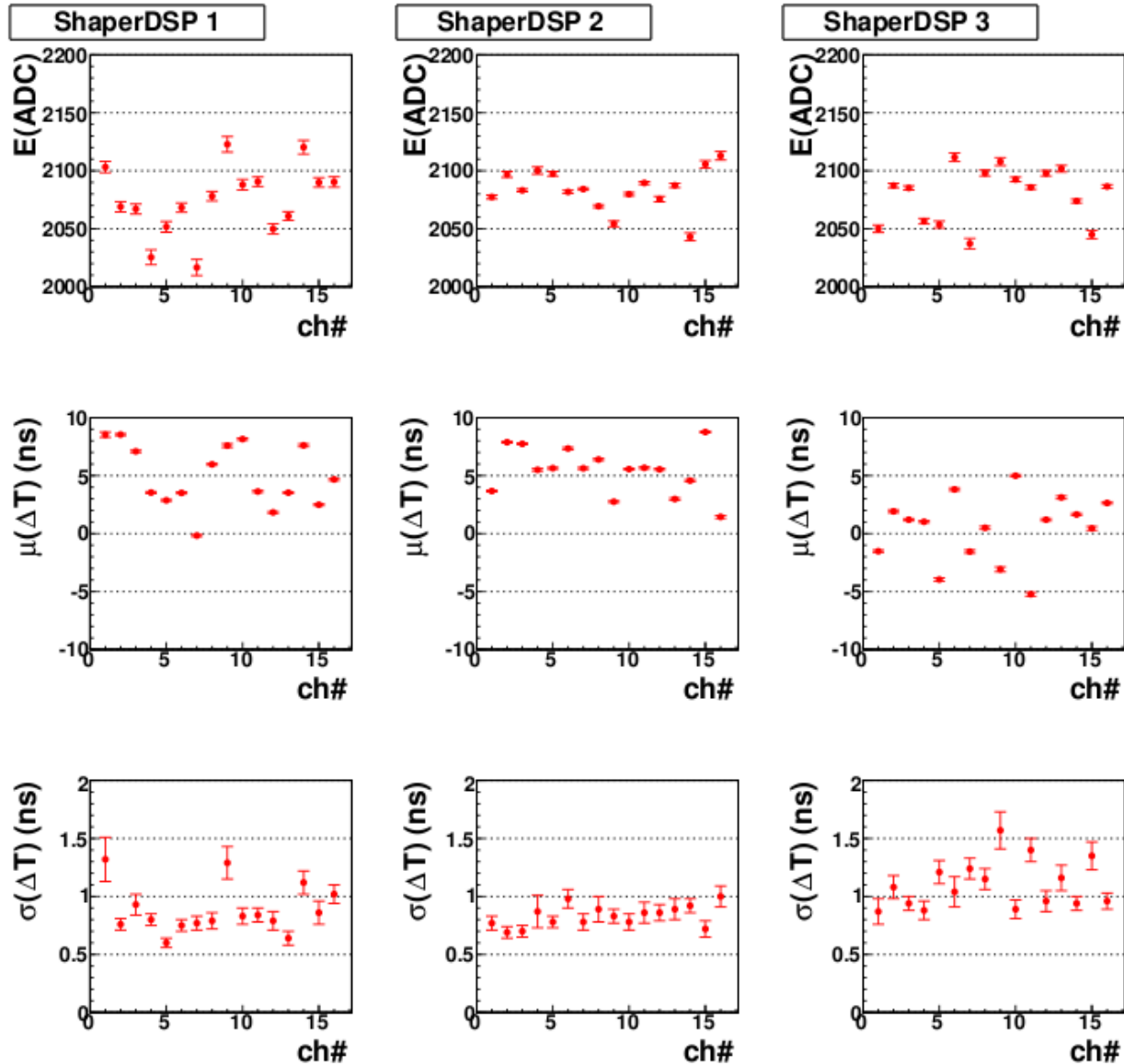
Cable+PreAmp effect on timing

PreAmp

PreAmp

FAM

Shaper(ref)

Shaper(A)

Collector
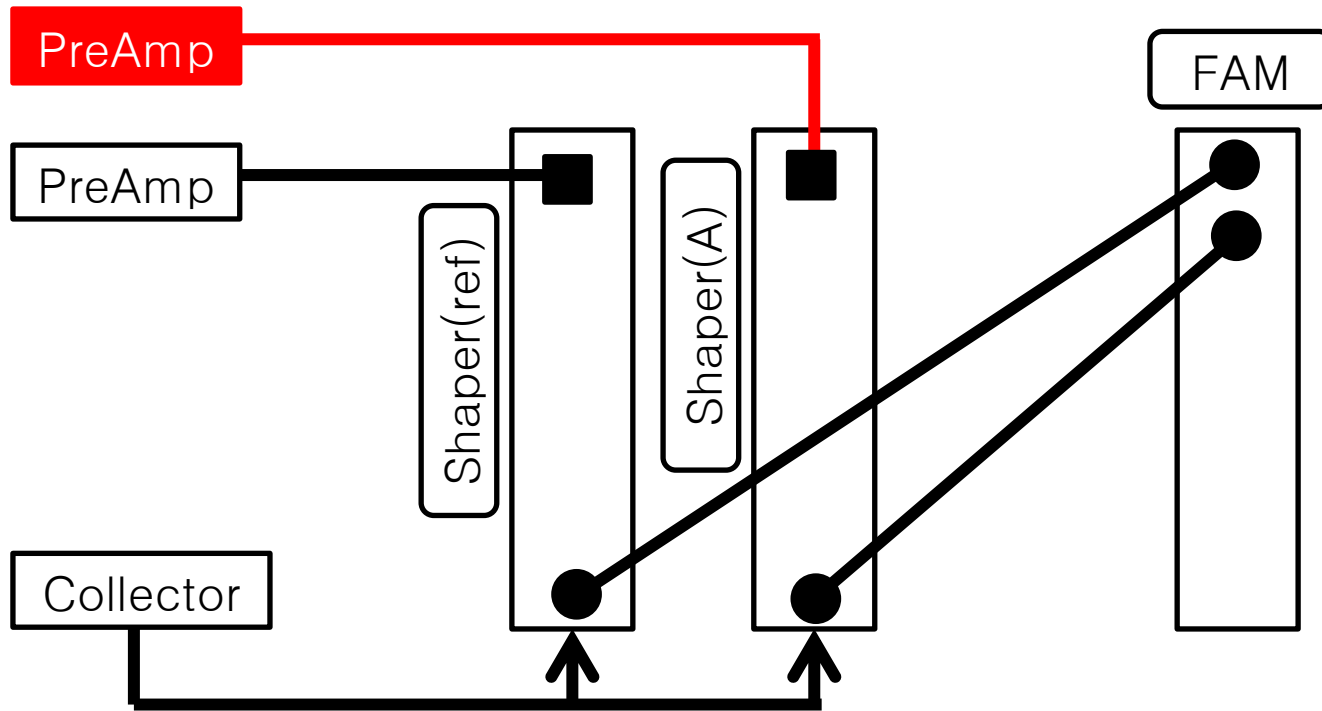
●All setup(module, cable, connection) are fixed, except for
   ●Cable+PreAmp connected to ShaperDSP(A)
   ●11 samples of Cable+PreAmp

Cable+PreAmp effect on timing
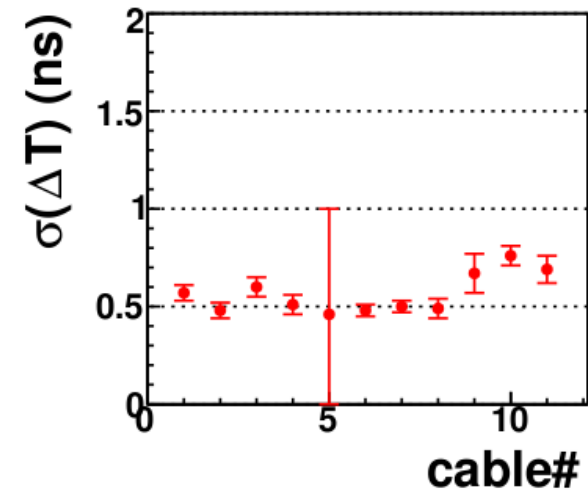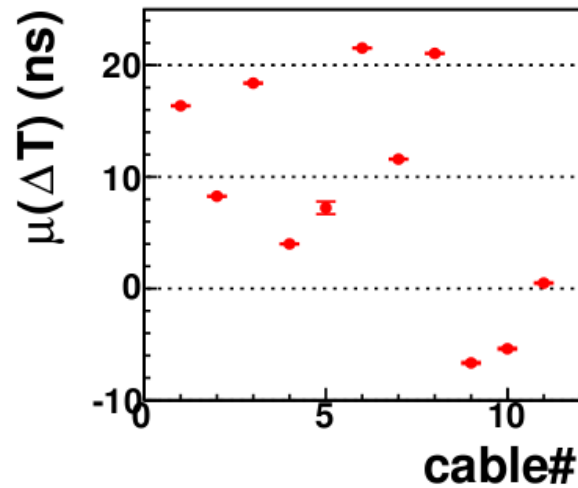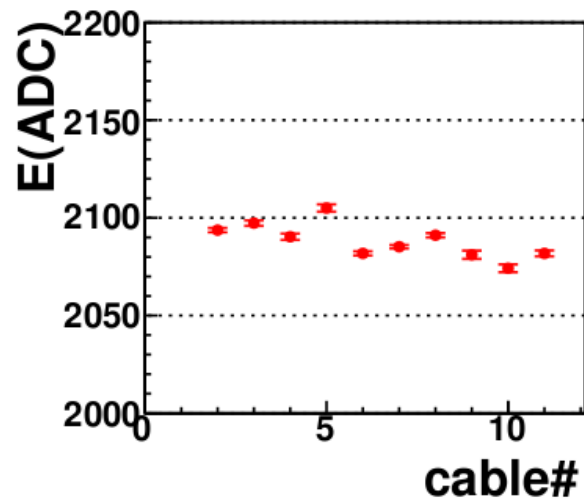
Belle2 ECL trigger system
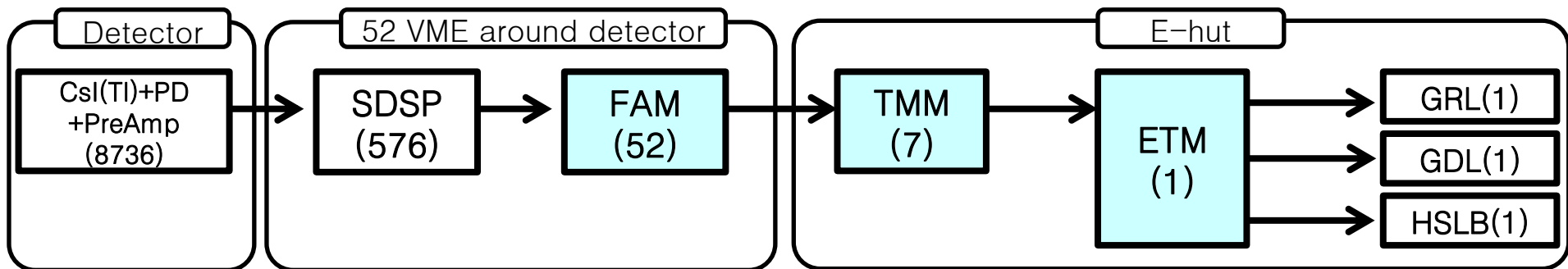
- <u>FAM</u>
  - Receive 576TC analog data from ShaperDSP
    - 1TC consists of 4x4=16Xtals
  - Digitization with FADC
  - TC E&T rec. by waveform analysis(χ^2 fit) on kintex7
- <u>TMM</u>
  - Play an role of merger on kintex7
- <u>ETM</u>
  - ECL trigger decision by all TC E&T on virtex6
  - Send ECL trigger summary to GDL
  - Send cluster data to GRL
  - Send fired TC E&T and trigger summary to HSLB

ECLTRG operation in exp7,8

https://confluence.desy.de/display/BI/ECL+Trigger+Operation

Exp	Run	Date	Module	comment
8	1998-	2019/06/05	ETM	Add new functionality for low multi-physcs bit to chose "at least X CL ≥ 300 MeV(Lab)" to reduce trigger rate. Keep default condition(1 CL >300MeV(lab)) so far.
8	1948 1783 1770	2019/06/04 2019/06/01 2019/06/01	ETM	Wrong b2link parameters on ETM. Bad runs for ecltrg. Trigger bits to GDL seem ok
8	551-	2019/05/16	FAM	Two problems about TC timing shift caused in FPGA and mcu are fixed.
7	3901-	2019/05/06	ETM	Tightened angle selection on mumu trigger
7	2794-	2019/04/23	ETM	Update of data format to GRL to have energy cut in CM from lab.
7	2718-	2019/04/22	FAM	bug fix of LUT for tap and bitslip. 16ns TC timing shift by FAM reboot due to wrong LUT was fixed.
7	2046-	2019/04/08	FAM	Firmware update, but no change in trg logic. Change only in monitor logic.
7	Before phy. run	2019/03/23	FAM	TC E threshold to 19 ADC from 20 to have 100MeV TC cut

●TC energy and timing calibrations are ongoing…(→YoungJun's report)

Status

- Frequent ttlost on FAM 20
    - Fixed by replacing LAN connected to FTSW with that used for FAM 21
    - The reason of ttlost on FAM 20 is unclear…
    - A few similar cases before…

- 4 jumpers on Shapers are reconfigured.

```
(before July/8) Yuriy changed jumper setting of ShaperDSP.

(1) TCID(199), CellID(7239), Collector(10), Shaper(11), Channel(11) : gain x2.0 (jumper install)
(2) TCID(271), CellID(6976), Collector(16), Shaper(11), Channel(13) : gain x2.0 (jumper install)
(3) TCID(485), CellID(5896), Collector(34), Shaper(9),  Channel(13) : gain x0.5 (jumper removal)
(4) TCID(479), CellID(2872), Collector(18), Shaper(3),  Channel(16) : gain x2.0 (jumper install)

In (4) case, Yuriy cut one Pin-diode since it is unstable (or noisy?).
```

Status

- Local cosmic run with ECL+ECLTRG (w/o GDL)
  - For calibration, and ecl+ecltrg consistency check
  - with WF saving, Askip=5 MeV, Awf=50 MeV

```
/ghi/fs01/belle2/bdata/group/detector/ECLTRG/data/e0009/cosmic
r00694 : TC energy threshold=19 ADC
r00698 : TC energy threshold=40 ADC
r00712 : TC energy threshold=40 ADC
```

  - Data analysis will be done by Sunghyun, Mikhail, YoungJun
  - ETM firmware update by Sunghyun and parameter turn by Mikhail
    - ETM issues trigger to FTSW64 with fine timing now.
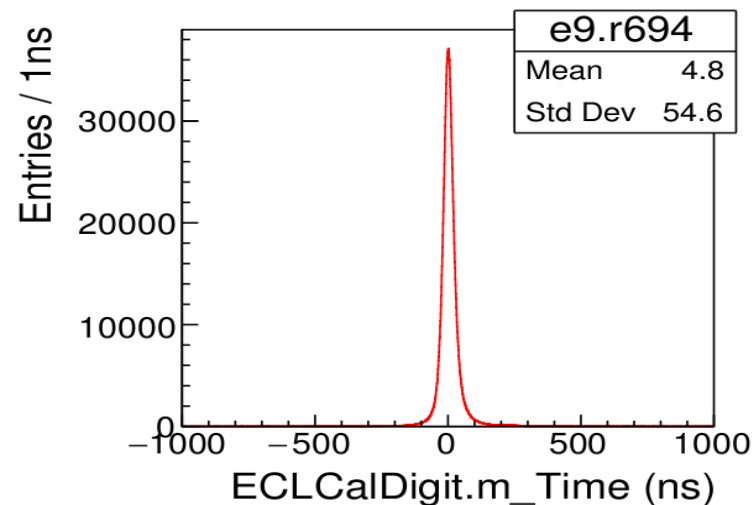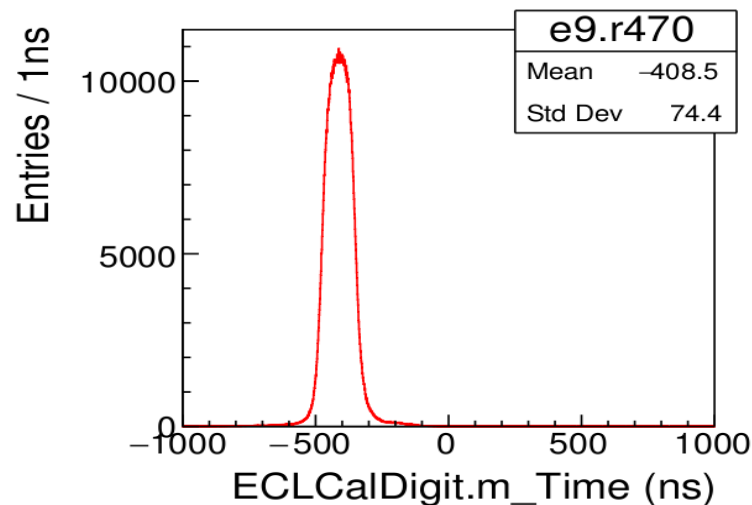
Status

● ETM-GDL GTX → GTH to avoid instability of GTX protocol on GDL

ETM	1GTX for GDL	1GTX	GDL
	4GTH for GRL	4GTH	GRL

ETM	1GTH for GDL 3GTH for GRL	PP	1GTH	GDL
			3GTH	GRL
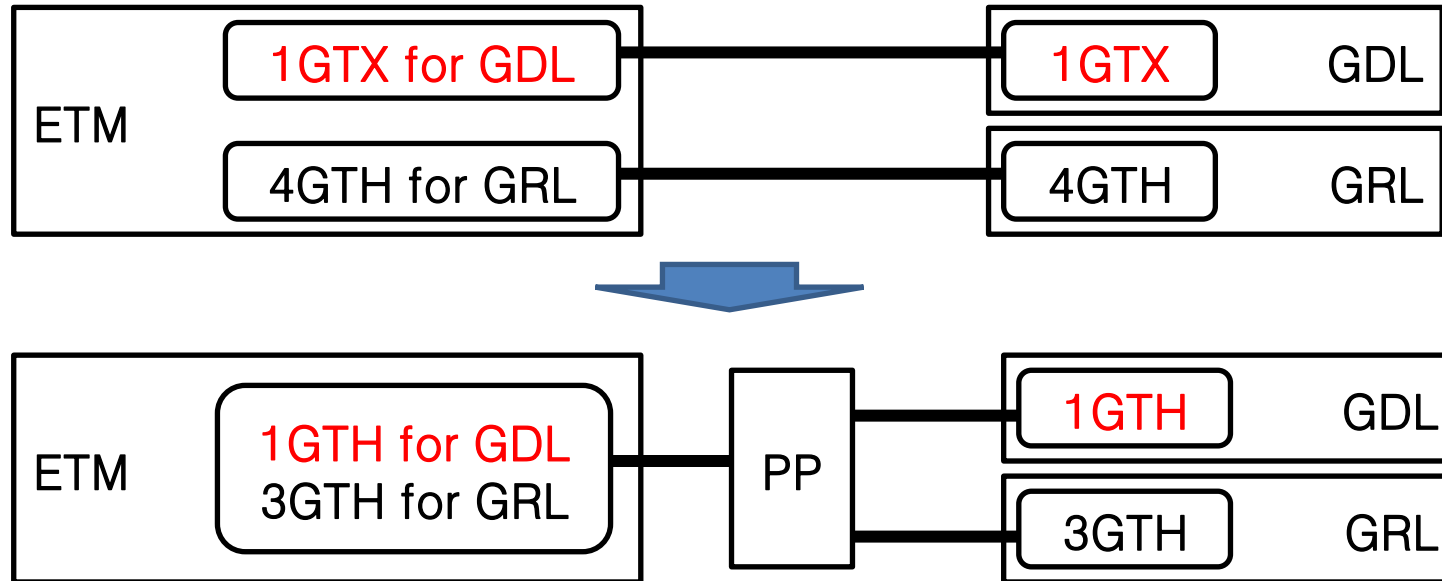
●Stability check at GDL side will be started after summer shut-down

●FAM CPLD and MCU firmware update and downloading at detector
  ●Only 1 TCP/IP port was available for full operation
    ●TC waveform check and remote update of MCU firmware
    ●When the 1 port had a trouble, VME power-recyle or
       MCU firmware download at detector was needed.
  ●Now all 3 ports are available for full operation as original plan.

TC 532 status

TC531   TC532

Noise

Hit rate

Jul/1   Jul/22   Jul/1   Jul/22
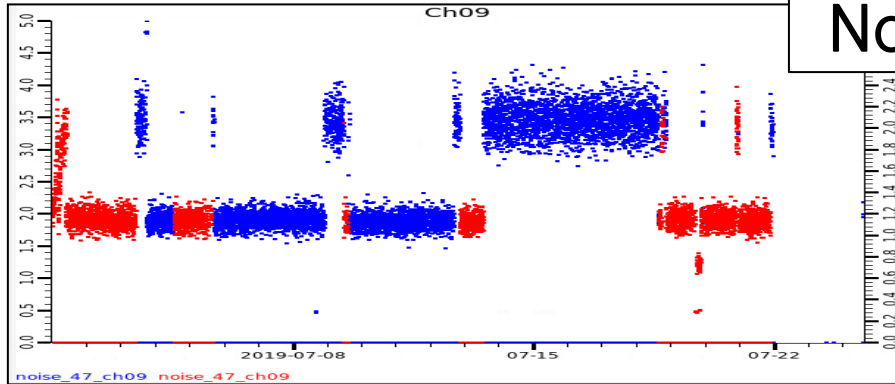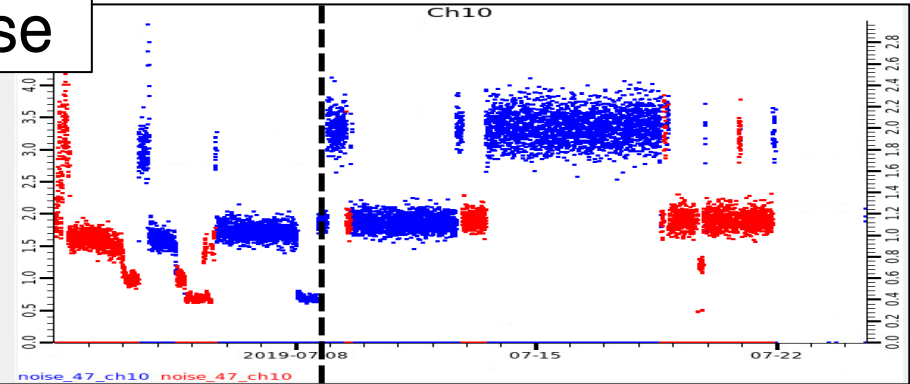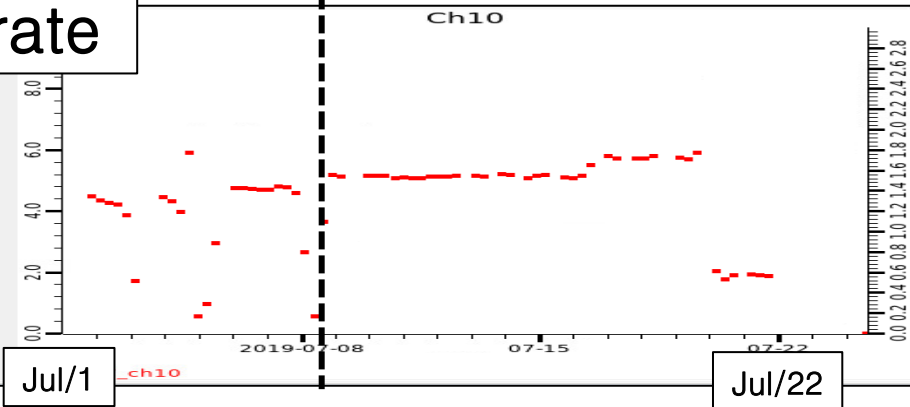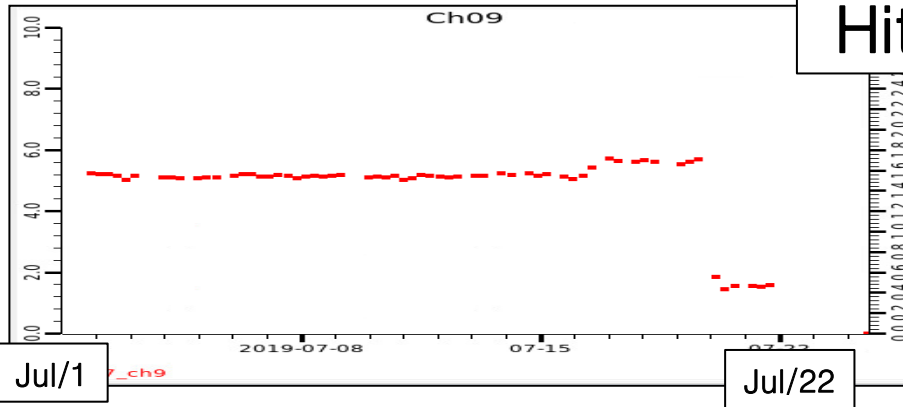
● TC532 recovered(?) after disconnection and connection of LEMO cable⋯
● If the problem appears again, replace LEMO cable and/or FAM

lml0

- LmI0
  - N(CL)>=3 in θ−ID=1−17, at least 1CL>=300 MeV(lab), not ECL 3D Bhabha
- New proposal
  - N(CL)>=3 in θ−ID=2−16, at least 1CL>=500 MeV(lab), not ECL 3D Bhabha

PSNM output bits (all events)

-PSNM output bits of all events
-Dominant bits are fff, ffo, ffb, hie, lml0

-exp8r1518 (physics) is used

ffo

hie

c4

3DBhabha

lml0

lmI0

Dear Unno-san; here are the numbers from my HLT study for experiment 8 run 1539. The HLT was in monitoring mode for this run.

Existing cluster trigger:
  - ≥3 clusters with Ecms>0.2 GeV, including ≥1 with 0.3 GeV < Ecms < 2 GeV
  - cross section = 24.9 nb
  - exclusive cross section (i.e. event passes no other filter) = 19.7 nb
  - overall generic tau efficiency = 89.5%
  - efficiency of cluster triggers for tau pairs = 46.0%

Proposed cluster triggers:
  - clusters must satisfy thetaLab>18.5 deg and thetaLab<139.3 deg (= trigger thetaID [2,16])
  - ≥4 clusters with Elab>0.18 GeV, including ≥1 with Elab>0.3 GeV and none with Ecms>2 GeV
  - OR exactly 3 clusters with Elab>0.18 GeV, including ≥1 with Elab>0.5 GeV and none with Ecms>2 GeV
  - cross section = 10.3 nb
  - exclusive cross section = 4.9 nb
  - overall generic tau efficiency = 87.6%
  - efficiency of cluster triggers for tau pairs = 45.9%

lml0

The proposed changes reduce the exclusive cluster trigger rate by a factor of four, at the cost of 1.9% in generic tau pair efficiency. On the other hand, as Torben noted, the new configuration has good efficiency for physics events that contain a muon pair plus another cluster, whereas the existing configuration has poor efficiency.

The drop in tau efficiency is from the reduction in the angular acceptance of the trigger, but it is partial compensated by the increased efficiency for minimum ionizing particles.

I also tried a variation in which the 3 cluster trigger was "exactly 3 clusters with Elab >0.18 GeV, including ≥2 with Elab>0.3 GeV and none with Ecms>2 GeV". The exclusive cross section increases from 4.9 nb to 5.7 nb, and the tau pair efficiency drops from 87.6% to 87.3%.

The looser variation, exactly 3 clusters with Elab >0.18 GeV, including ≥1 with Elab>0.3 GeV and none with Ecms>2 GeV" would have better physics efficiency, but the exclusive cross section is 12.6 nb.

    - Chris

ImI0

- At first, need to wait an approval from τ group.
- Issue trigger with both ImI0 and ImI in autumn run
    - How long (short or all autumn run or)?
    - Better to compare ImI0 and new ImI with beam data in autumn run
- case1
    - keep current ImI0, and mask it at GDL later
    - Prepare new ImI12 (?) for new ImI
    - Firmware and software need to be updated at both ETM and GDL
- case2
    - Simply replace ImI0 to new ImI
    - →GDL does not require any change

CPLD and MCU

- 3 ports of TCP/IP are available on each FAM for control and monitoring.
    - Only one of them (port=5000) is available to check TC waveform somehow…
    - 1 port needs to be kept open for SLC
    - It turned out there was a bug in CPLD
        - Always sends TC waveform to port=5000
        - Need to update firmware and download(remote download is not possible)

- MCU
    - Sometimes TCP/IP communication down happened.
        - Worst case we need to visit detector to fix it when remote firmware download is failed by TCP/IP port=5000.
    - Application firmware can be downloaded remotely only from TCP/IP port=5000
    - Plan to update bootloader MCU firmware to make remote download of application firmware possible by other TCP/IP port

- Both CPLD and MCU(bootloader) firmware cannot be downloaded remotely
    - Need to visit 52 VMEs located detector one by one to update the firmware…

FAM

FTSW
127MHz

RJ45 → CLK generator

127MHz → FPGA 384, 256, 127, 64, 8 MHz

64MHz → 3 ADC

FPGA ↔ CPLD ↔ RJ45

CPLD ↔ MCU

RJ45 ↔ btrgctr0

Clk generator

DAC

ADC

ECL test pulse

unit (mm)
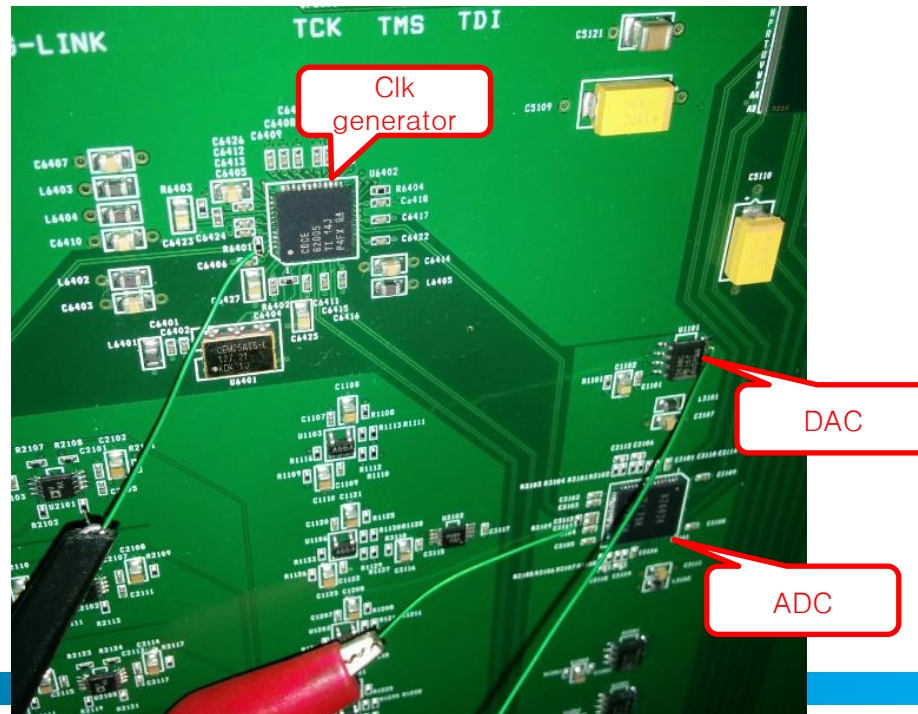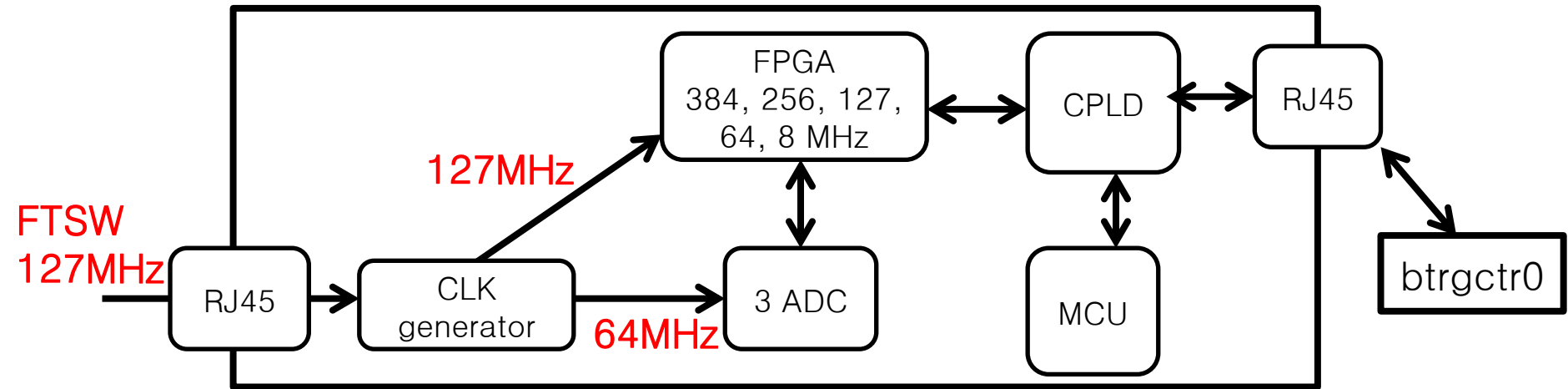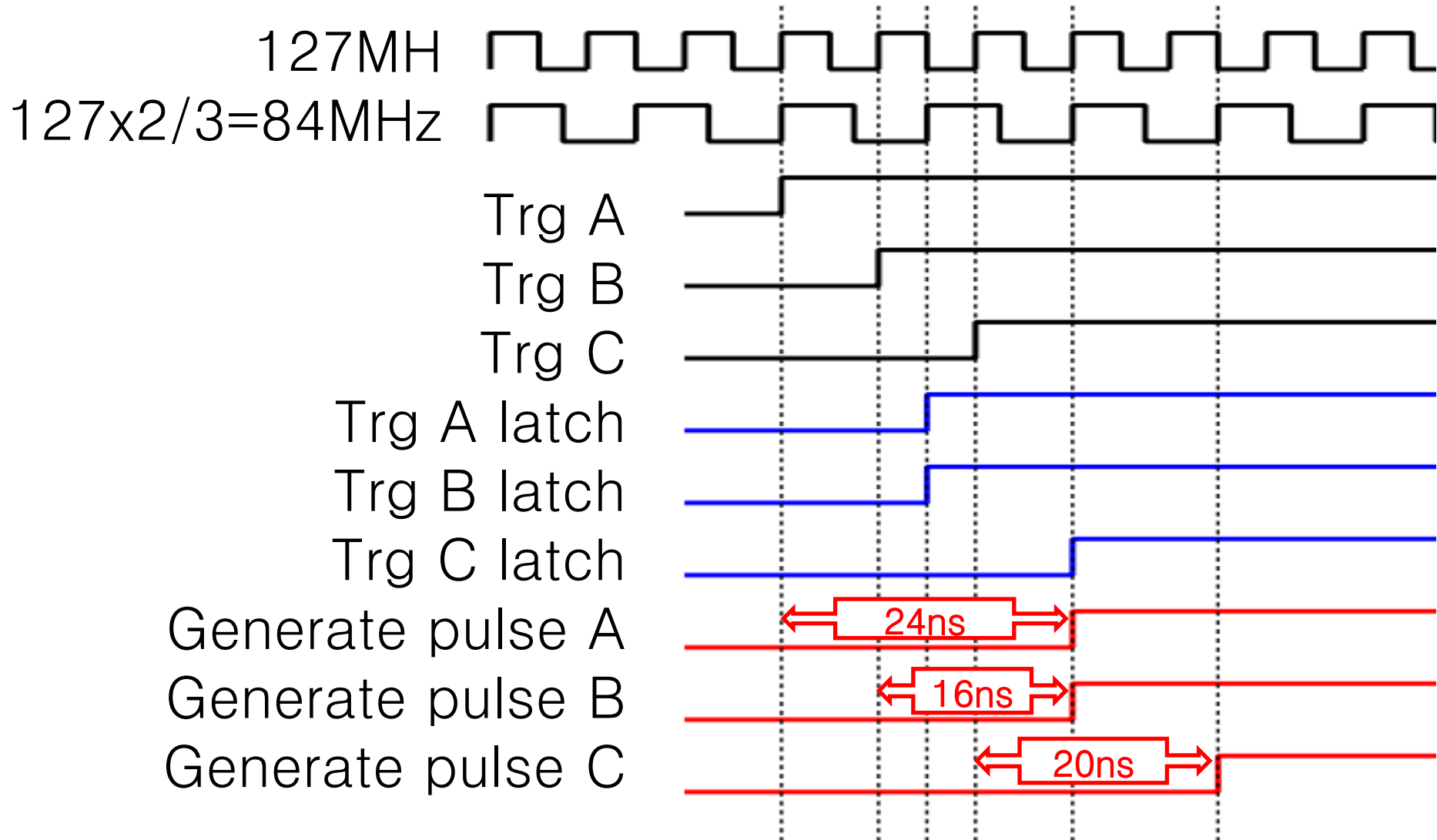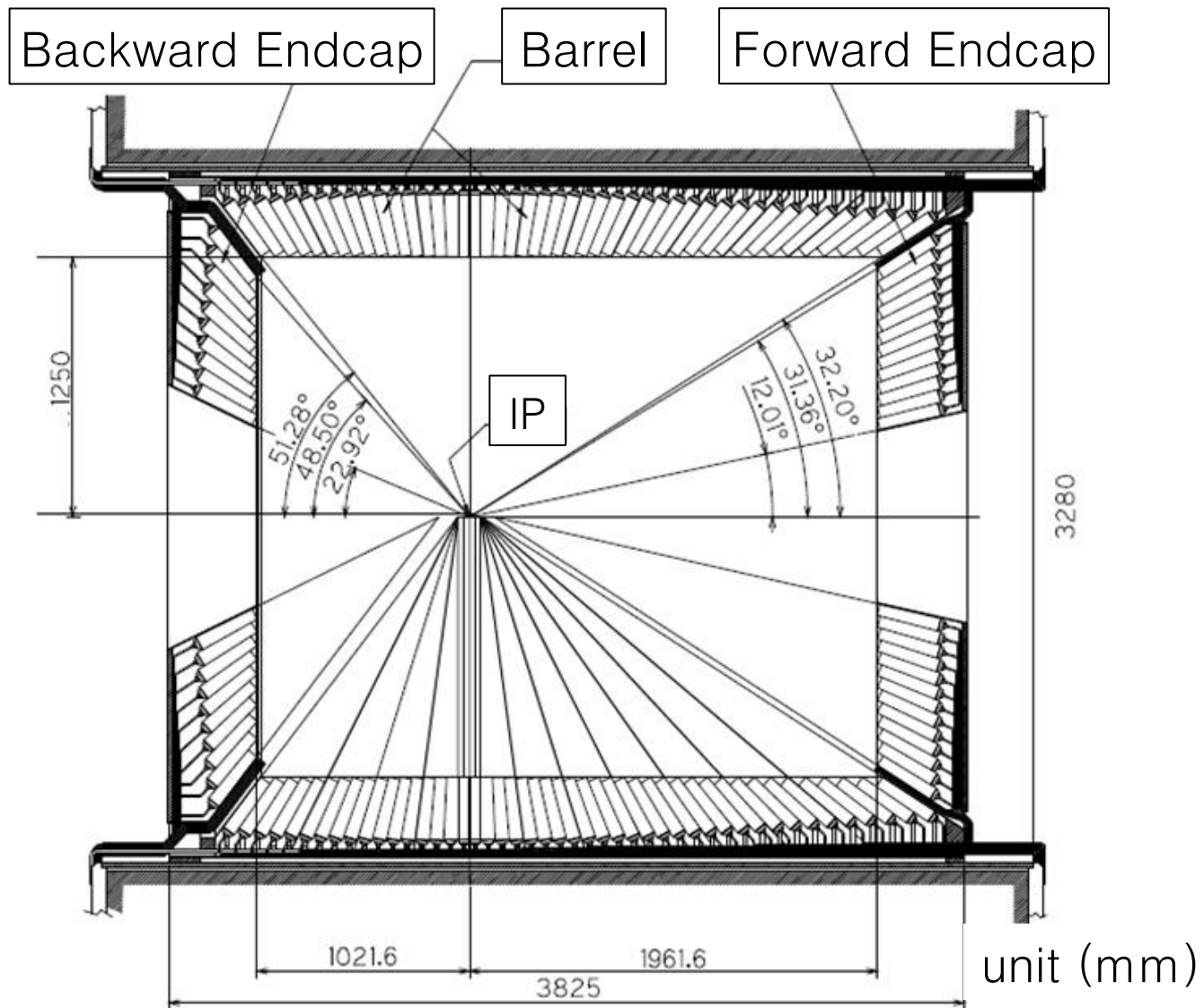
Status on noise problem

●1 ADC ~ 5MeV
●TC E Threshold=20 ADC

| Normal | (A) | (B) | (C) | (D) |
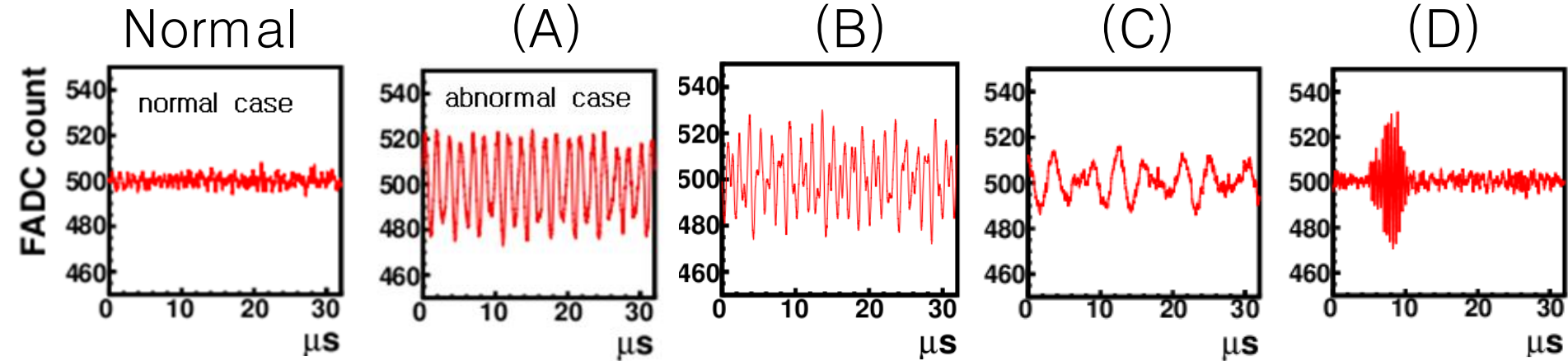
(A) ARICH FTSW
   ●Many FAM in FW and BR → fixed last Dec.
(B)TPC
   ●FAM3,46,47 due to TPC → OK if TPC is not there.
(C)ECL
   ●FAM45 ch3, FAM45 ch9, FAM52 ch4
(D)Unknown source : Noise bunch
   ●FAM48, 49, 51
●ECL experts found imperfect grounding method in endcap
   ●Found significant improvement in partial VME w/ new ground design
   ●Noise test can be done after eclcap is connected, next year⋯

Run by run TC timing shift

Phase 2 data by YoungJun

FAM 6
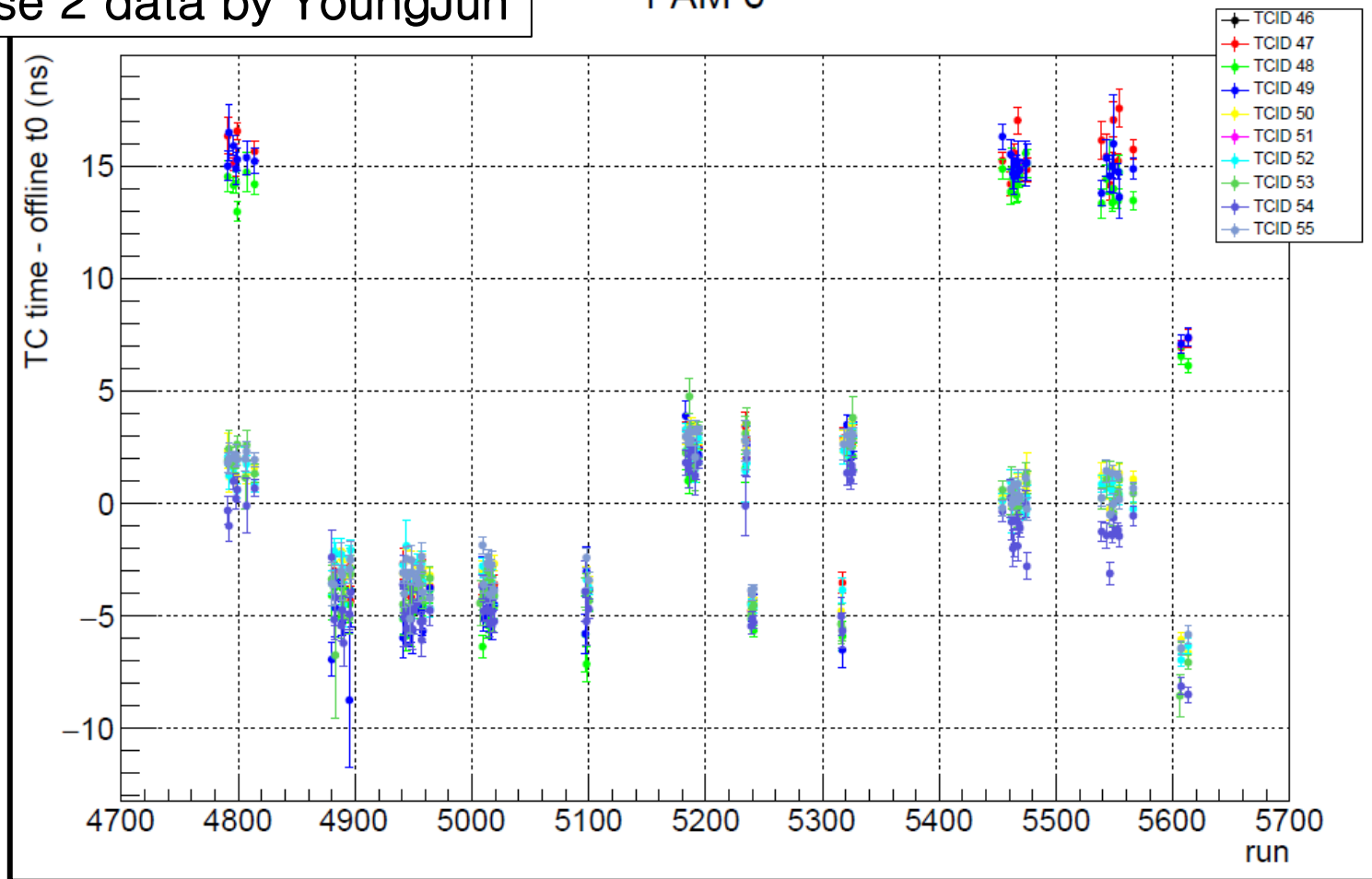
- ●Run by run TC timing shift even in single FAM board!
- ●TC timing calibration cannot be done, it's almost meaningless…

beam background overlay

SDSP — FAM(52) — TMM — ETM → HSLB

>100MeV TC data

A >100MeV TC data

Ethernet

B Waveform can be extracted

TRG server
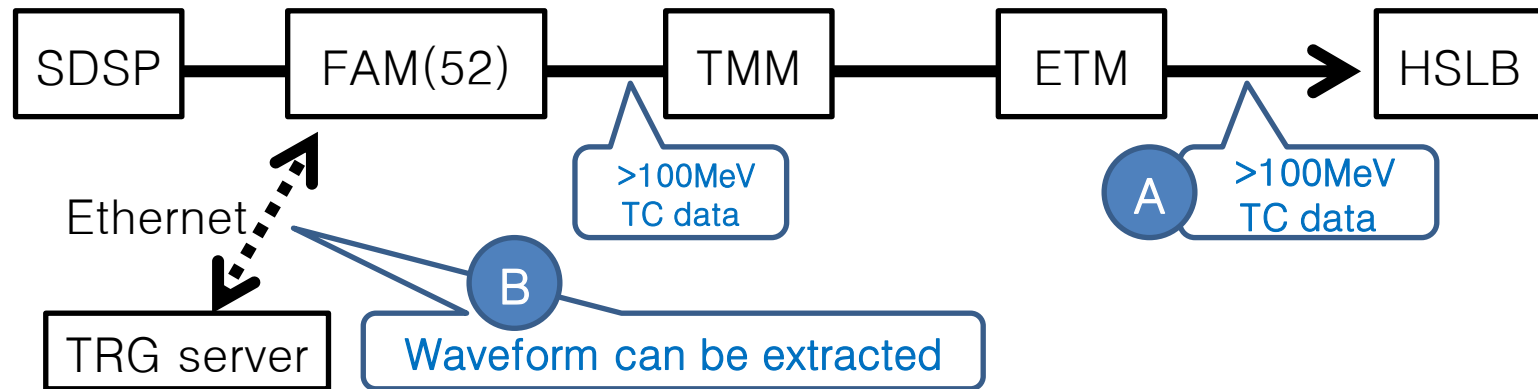
- FAM does not have b2link, no optical transceiver.
  - Difficult to take waveform data of all TC for each random trigger
- Alternative idea is to utilize data from (A) and (B)
  - (A) TC data(not WF) 100% associated with random trg by GDL
  - (B) waveform taken random trg by FAM
    - Check averaged noise level in each run and store into conditionDB

① ECLHit   ② make WF   ③ ②+(B)   ④ Fit on ③ and Get TC E&T   ⑤ Result ④+(A)
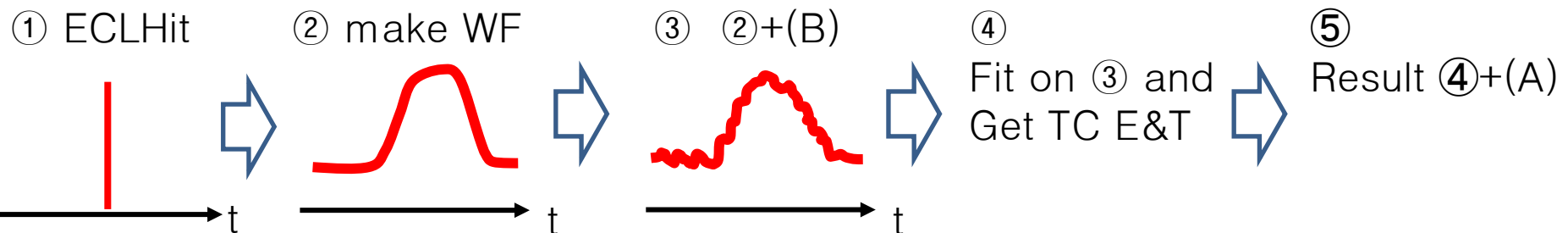
- No objection for this method in trg/soft session at last b2gm, but no actual progress since then…

ECL test pulse
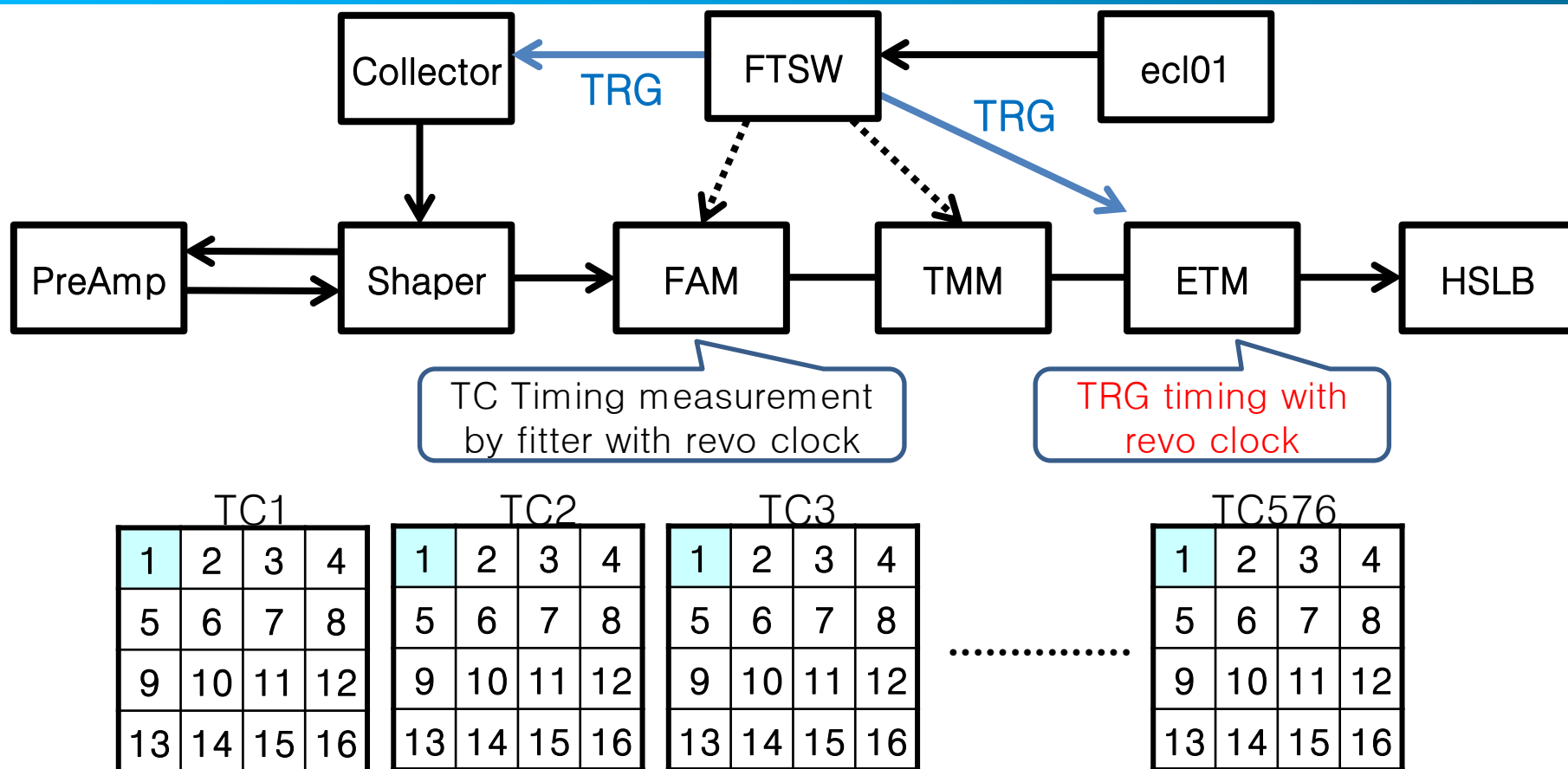
(0) "single channel test pulse" script on ecl01 by Mikhail (Thanks to Mikhail)
(1) Generate test pulse to ch1 of all TC (E~3 or 6GeV, 10k event, 0.5kHz)
(2) Repeat (1) 16 times by changing ch# (ch1 to ch16)
(3) **Repeat (1)** or (1)+(2) **after rebooting FPGA** or VME power-recycle

ECL test pulse

FAM1 ch1

h1000	
Entries	1001
Mean	−0.77
Std Dev	3.67

Entries vs T(trg) - T(ch 1) (ns)

FAM1 ch1

h3000	
Entries	341
Mean	3.11
Std Dev	1.69

Entries vs ΔT(ns)
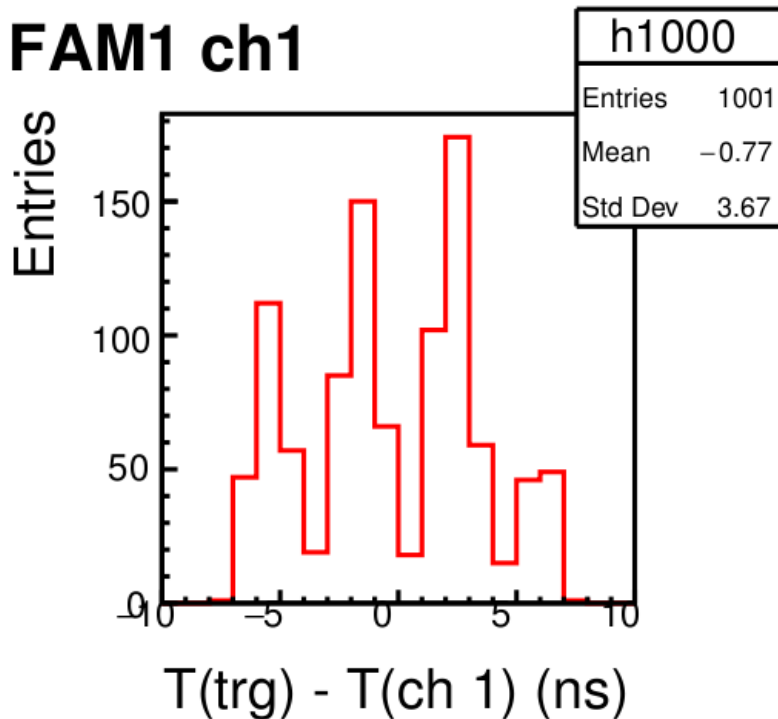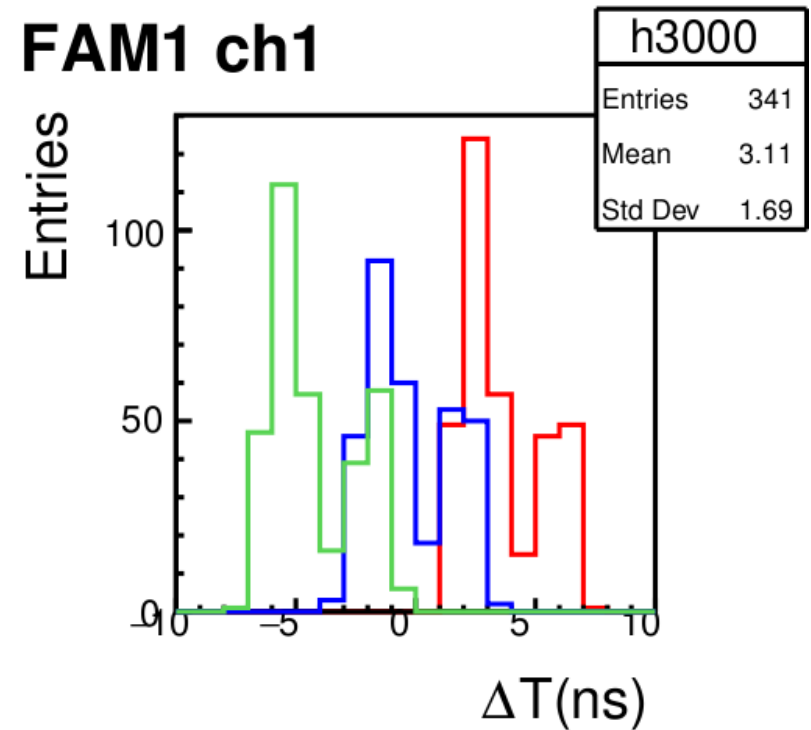
- T(trg)−T(ch) shows 4 peaks.
- 3 peaks by ECL uses 127MHz x 2 / 3 = 84MHz to generate test pulse.
- 4 peaks can be reduced to 2peaks using clock info. from ECL data.
- The reason of 2 peaks is under investigation.
- "Mean" in 4 peaks is used in this study.

ECL test pulse

FAM23 ch1

$T_{ref} - T$ (ns)

$\mu(set\#4) - \mu(set\#1)$

FAM FPGA reboot

set #
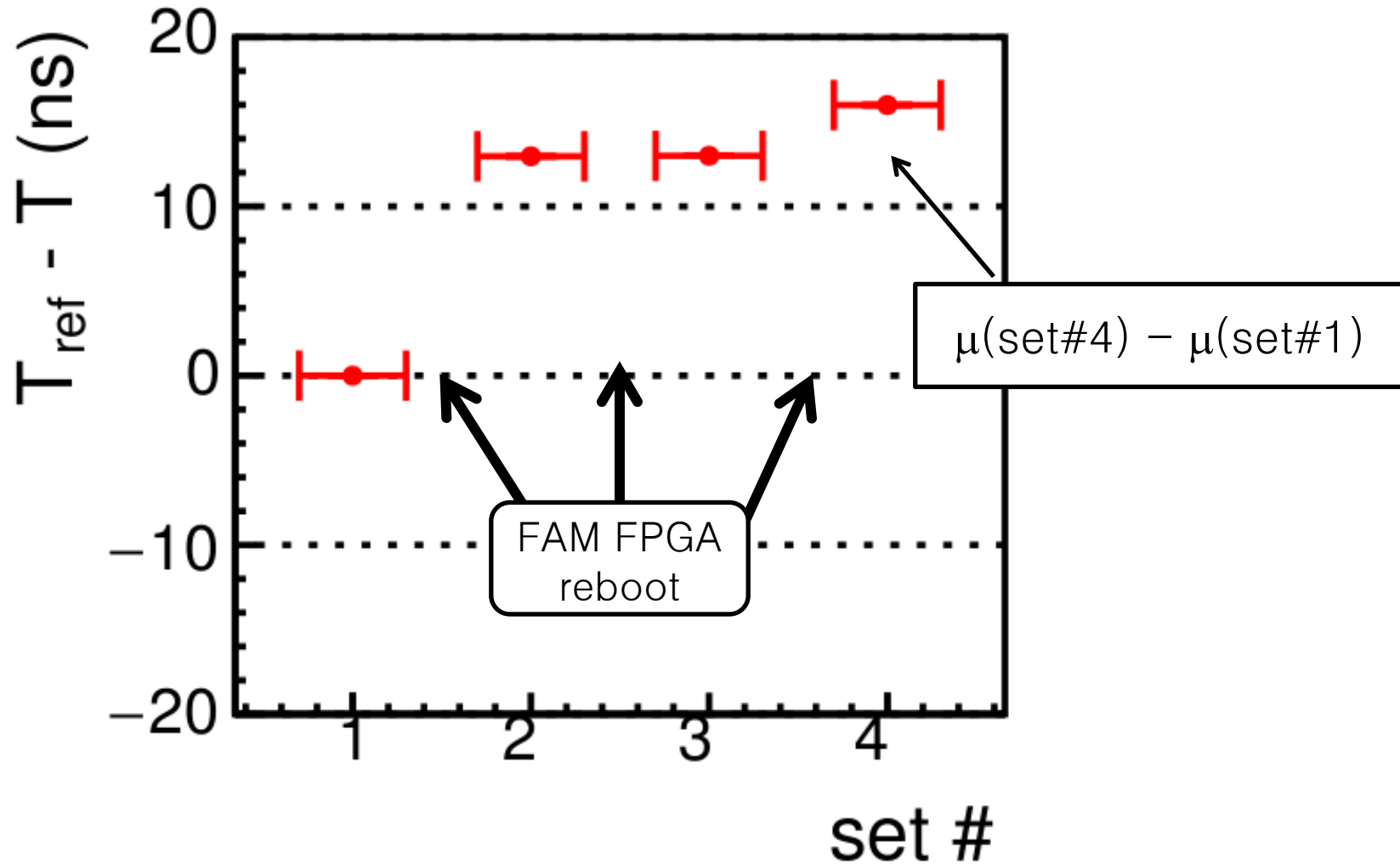
ECL test pulse
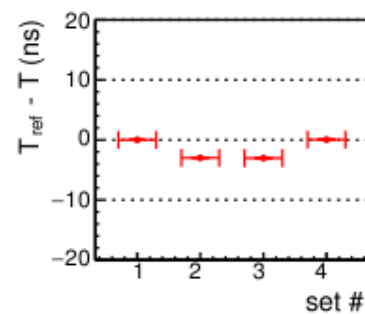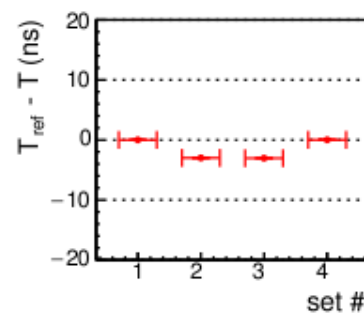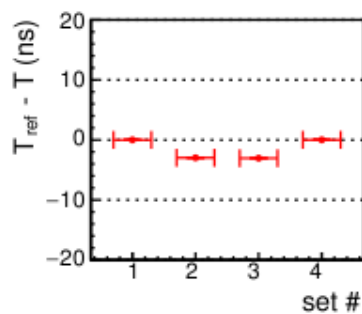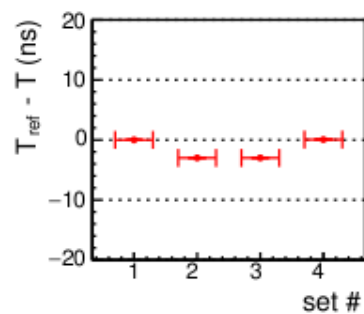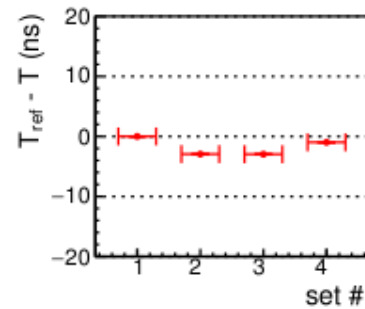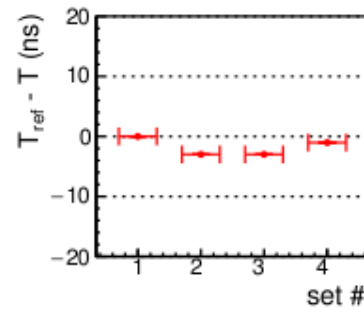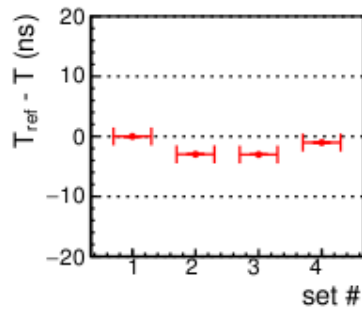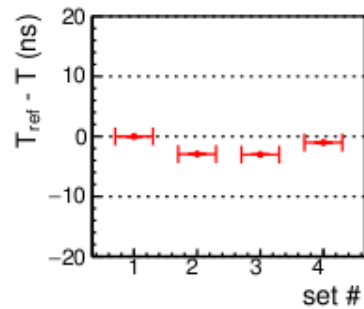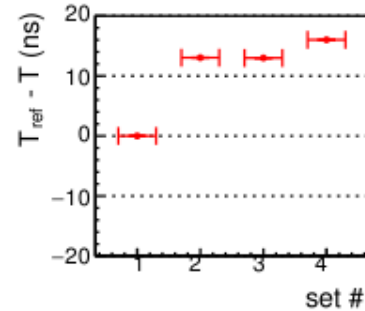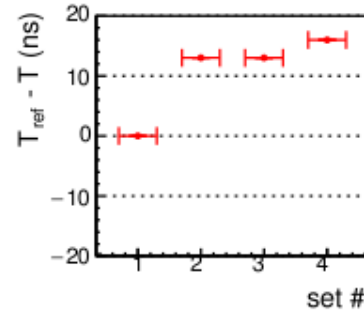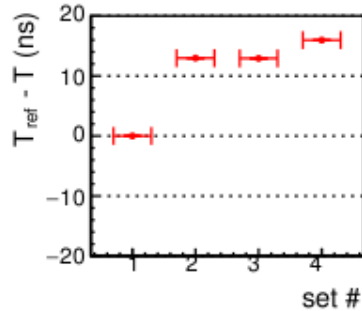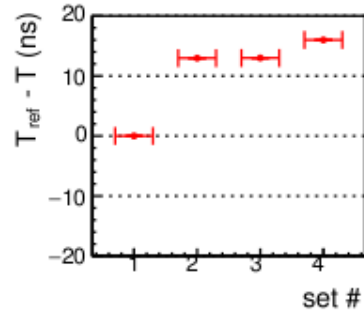
Correction of bitslip and tap

- ADC data capture by two parameters, bitslip and tap
  - bitslip: slip 12bits data by 0-5 bit (1bitslip=3ns) to find correct set of 12bit data.

192MHz clk

12 bit ADC data
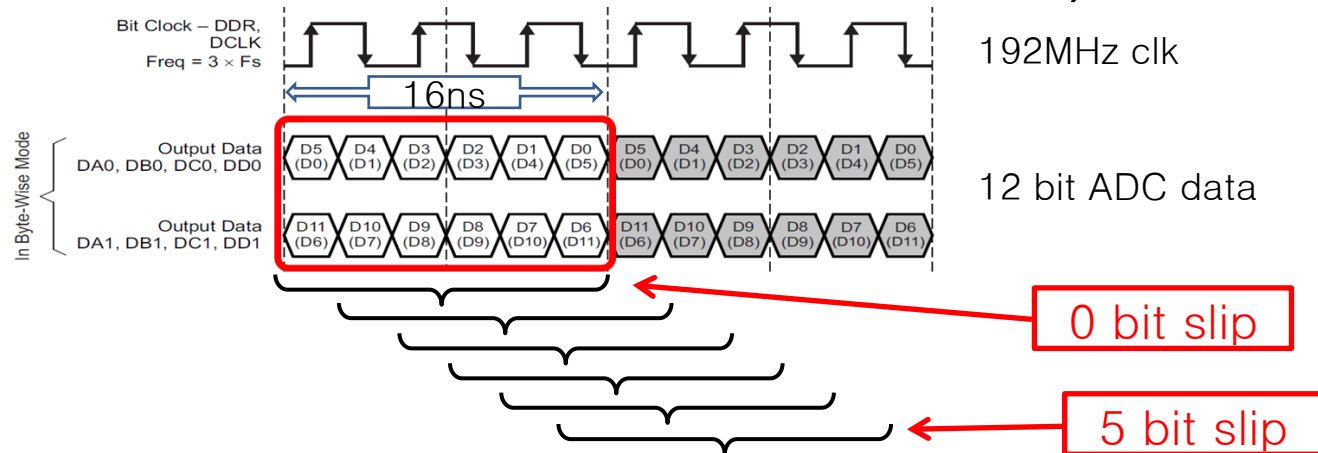
0 bit slip

5 bit slip

  - tap : shift ADC data with 0-31 tap(=0.0-2.3ns) with 75ps interval in order to adjust position of middle of data to clock edge(192MHz).
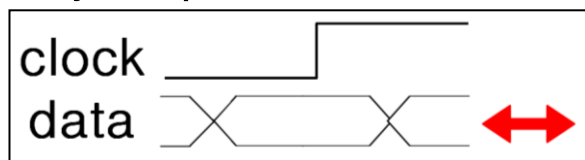
- Correction of data timing from N(bitslip) and N(tap)

FPGA

FADC
FADC
FADC

bitslip tap

fitter

LUT

Data timing shift by N(bitslip)+N(tap)

Timing correction by N(bitslip)+N(tap)
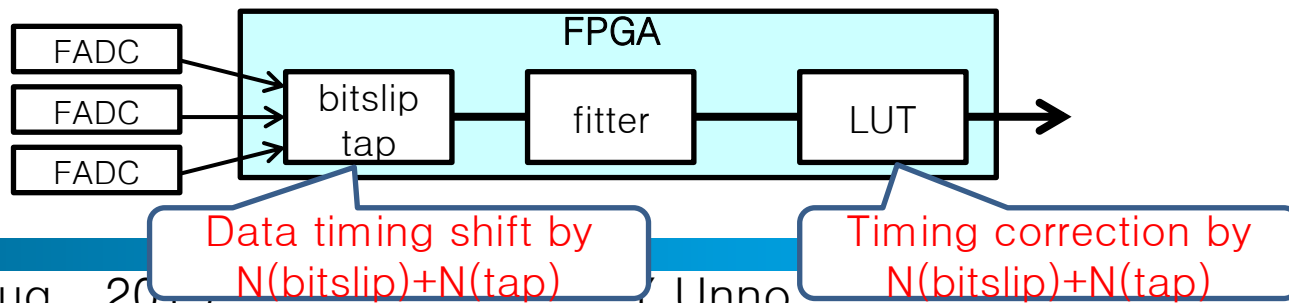
Correction of bitslip and tap
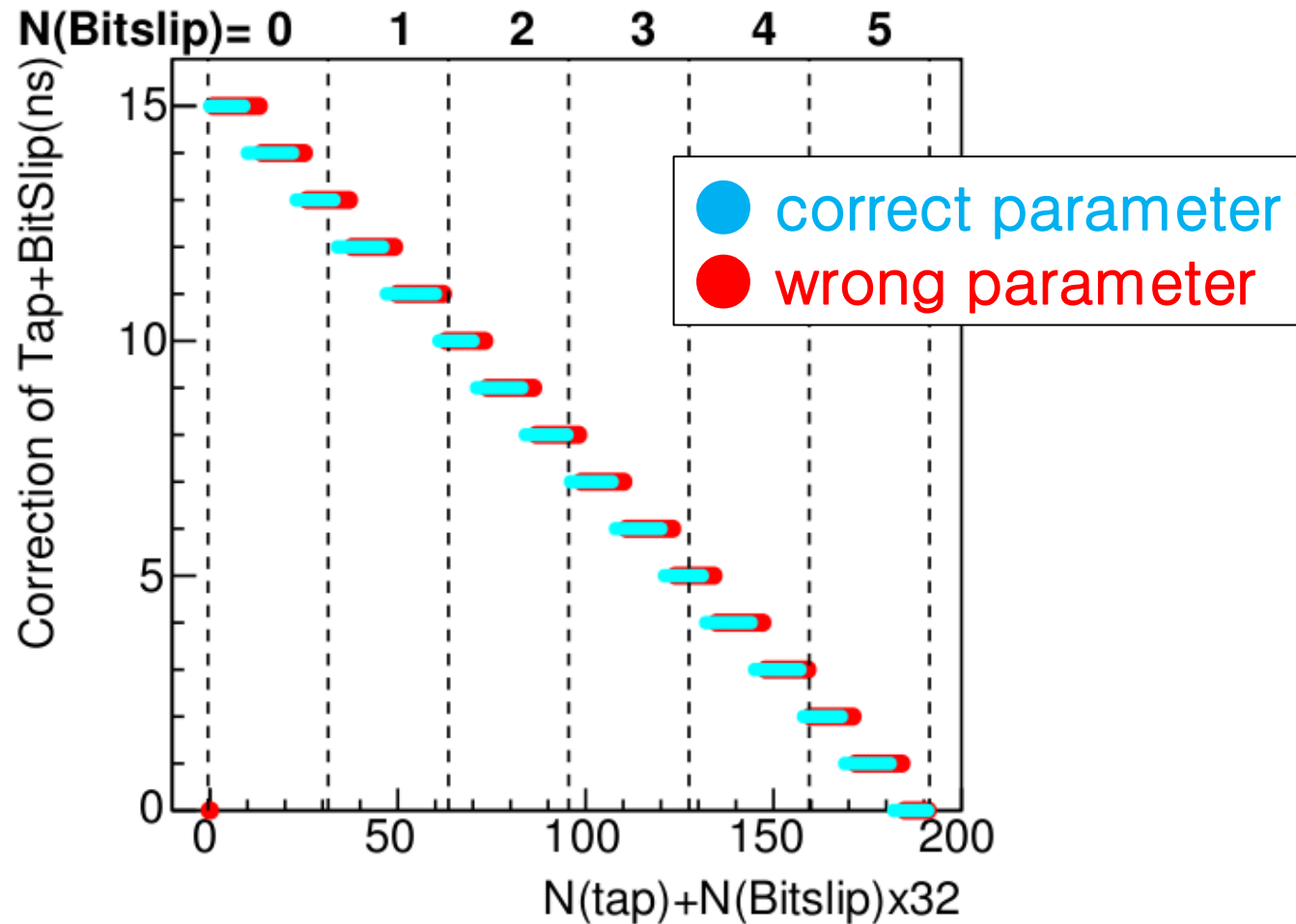
With wrong parameters, 1 or 15 ns TC timing shift happened whenever FPGA was rebooted⋯

ECL test pulse

After correction of LUT for bitslip and tap
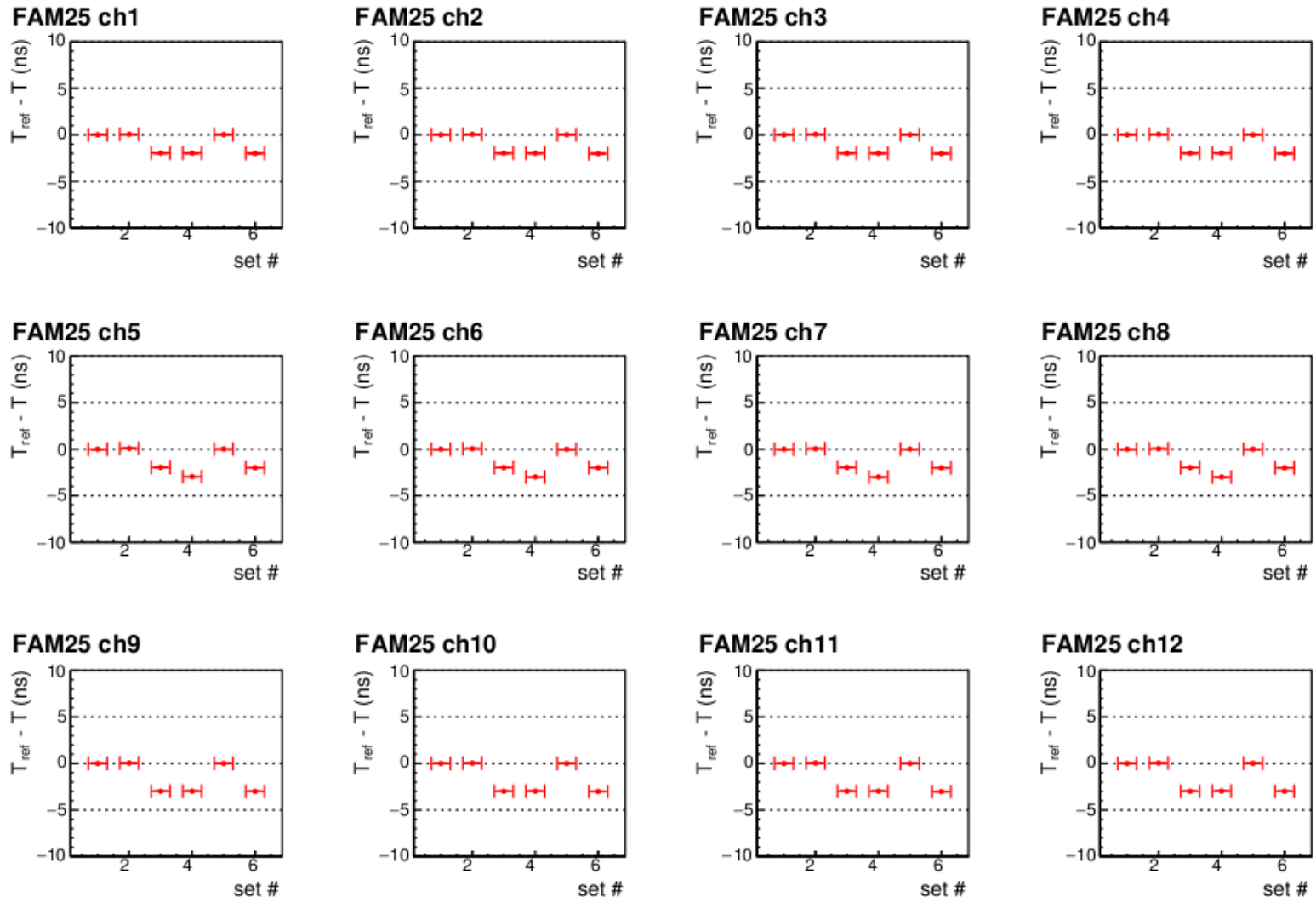
Clock of ADC data capture

(A) 384MHz clk
only w/ leading edge

(B) 192MHz clk with both
Leading/trailing edges

ADC data

Bit Clock – SDR, DCLK
Freq = 6 × Fs

Bit Clock – DDR, DCLK
Freq = 3 × Fs

In Byte-Wise Mode

Output Data DA0, DB0, DC0, DD0

| D5 (D0) | D4 (D1) | D3 (D2) | D2 (D3) | D1 (D4) | D0 (D5) | D5 (D0) | D4 (D1) | D3 (D2) | D2 (D3) | D1 (D4) | D0 (D5) |

Output Data DA1, DB1, DC1, DD1

| D11 (D6) | D10 (D7) | D9 (D8) | D8 (D9) | D7 (D10) | D6 (D11) | D11 (D6) | D10 (D7) | D9 (D8) | D8 (D9) | D7 (D10) | D6 (D11) |

Data Rate = 6 × Fs
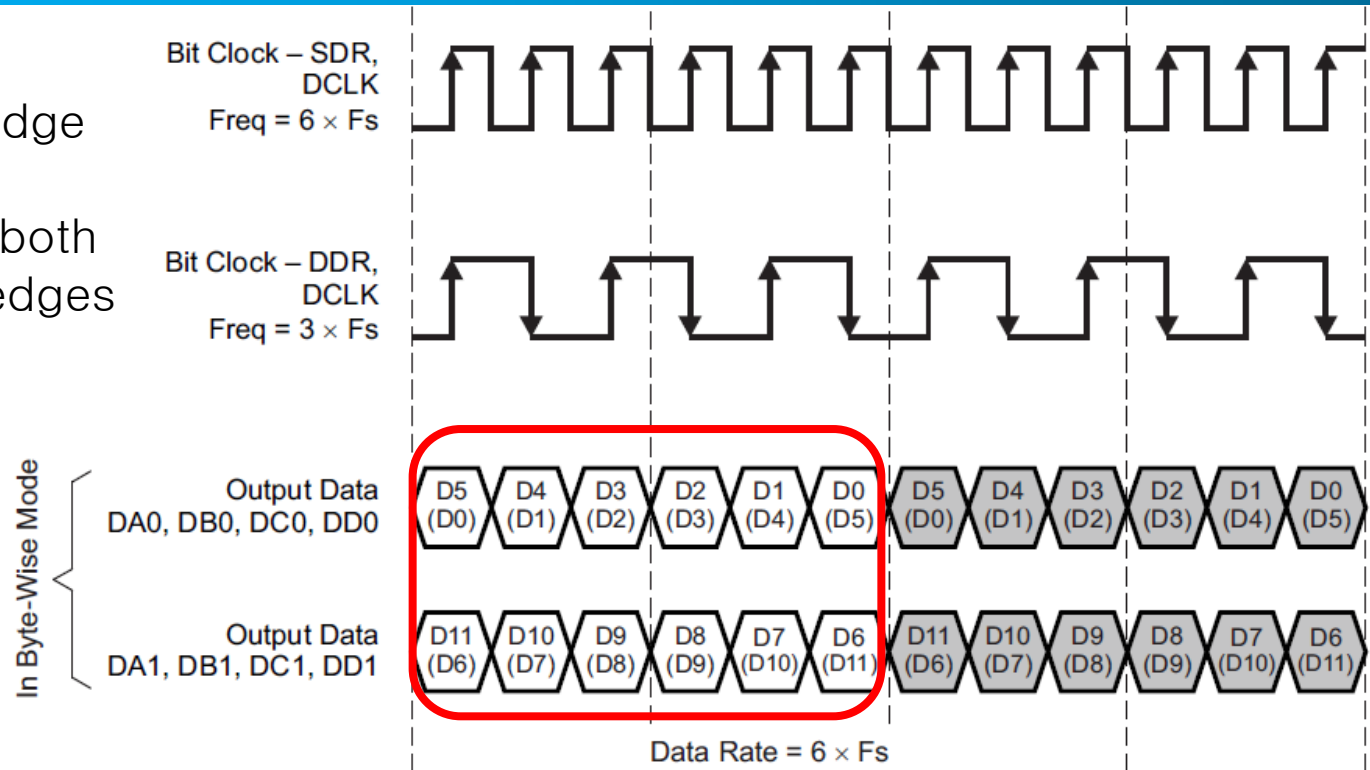
- In (B), leading edge captures odd # data, trailing captures even # data
  - Phase(0 or 180) of 192MHz is set arbitrary intentionally
  - This causes 3ns TC timing shift whenever FPGA is rebooted.
- Changed to (A) from (B) to avoid 3ns timing shift

auto-reboot function in MCU

FTSW
127MHz

RJ45 → CLK generator

127MHz → FPGA 384, 256, 127, 64, 8 MHz

64MHz → 3 ADC

FPGA ↔ CPLD ↔ RJ45

CPLD ↔ MCU

RJ45 ↔ btrgctr0
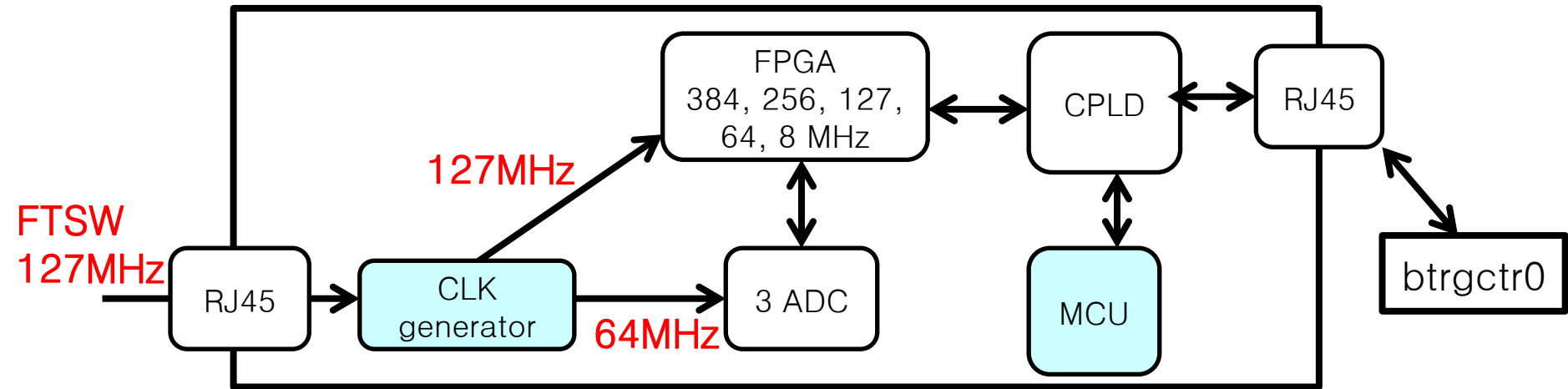
- Auto FGPA reboot function in MCU
  - when MCU detects unlocked clock (b2tt too !?),
  - it starts initialization of clock generator, and then reboot FPGA automatically.
- When FPGA reboot command is sent to MCU from btrgctr0 by user
  - (1) clock generator initialization, then (2) FGPA reboot
  - however, auto-reboot function detects clock down at (1), then
  - All are screwed up, input 127MHz and output 127, 64MHz not synchronized, then causes a few(?) ns timing shift···
  - Excluded auto-reboot function from MCU.
  - (wondering how FAM were working well so far···)

ECL test pulse

After fixing MCU and ADC data capture logic
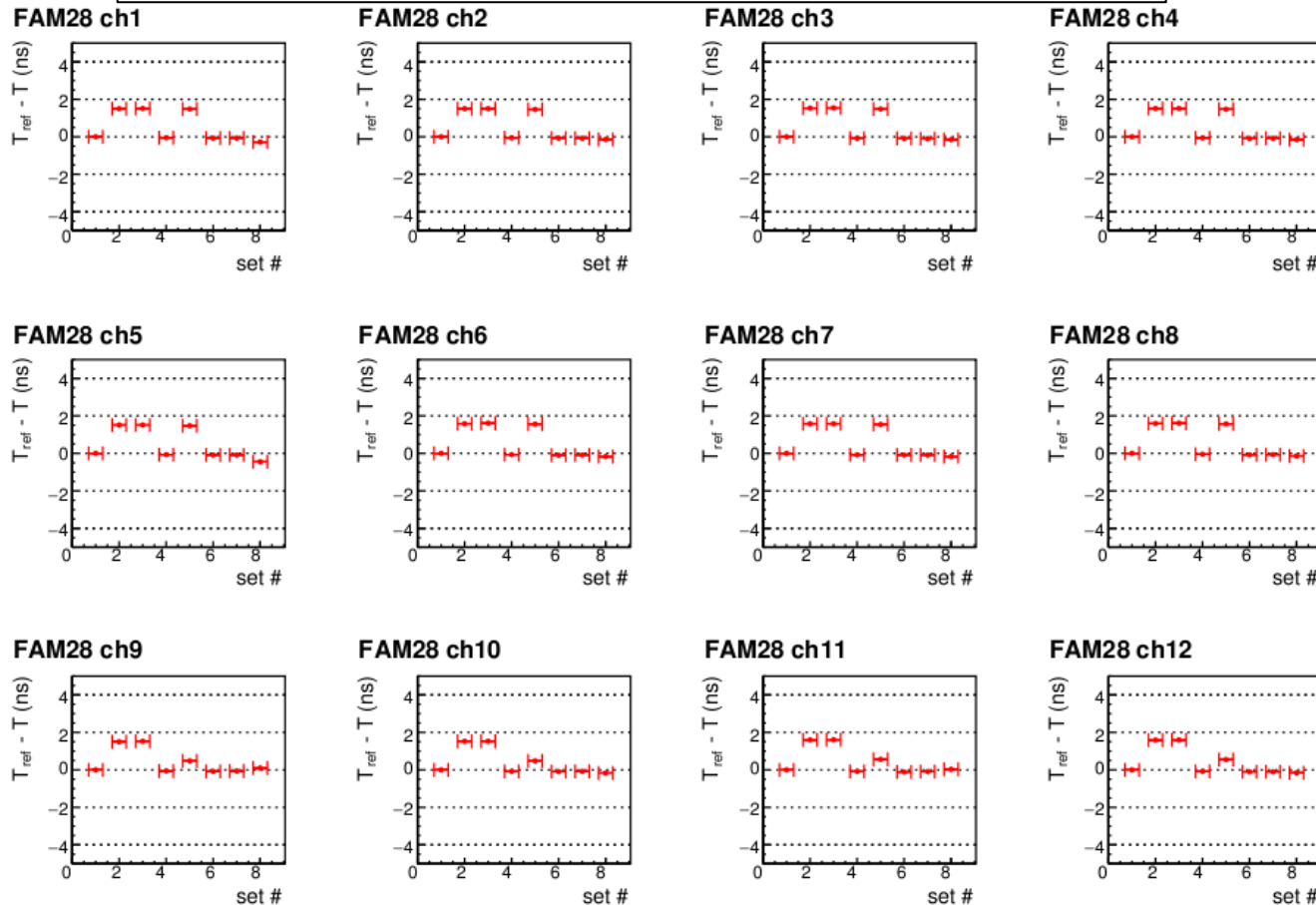
- 2ns timing shift ? Not 1ns shift ?
  - Plan to check again after fixing 4peak timing plot to 1peak
- TC timing calibration is possible now (from exp8 run 551)

TC timing bias by fitter

- **(very old)** simulation show fitter produces a bias on timing, which has dependences on input energy and noise level.
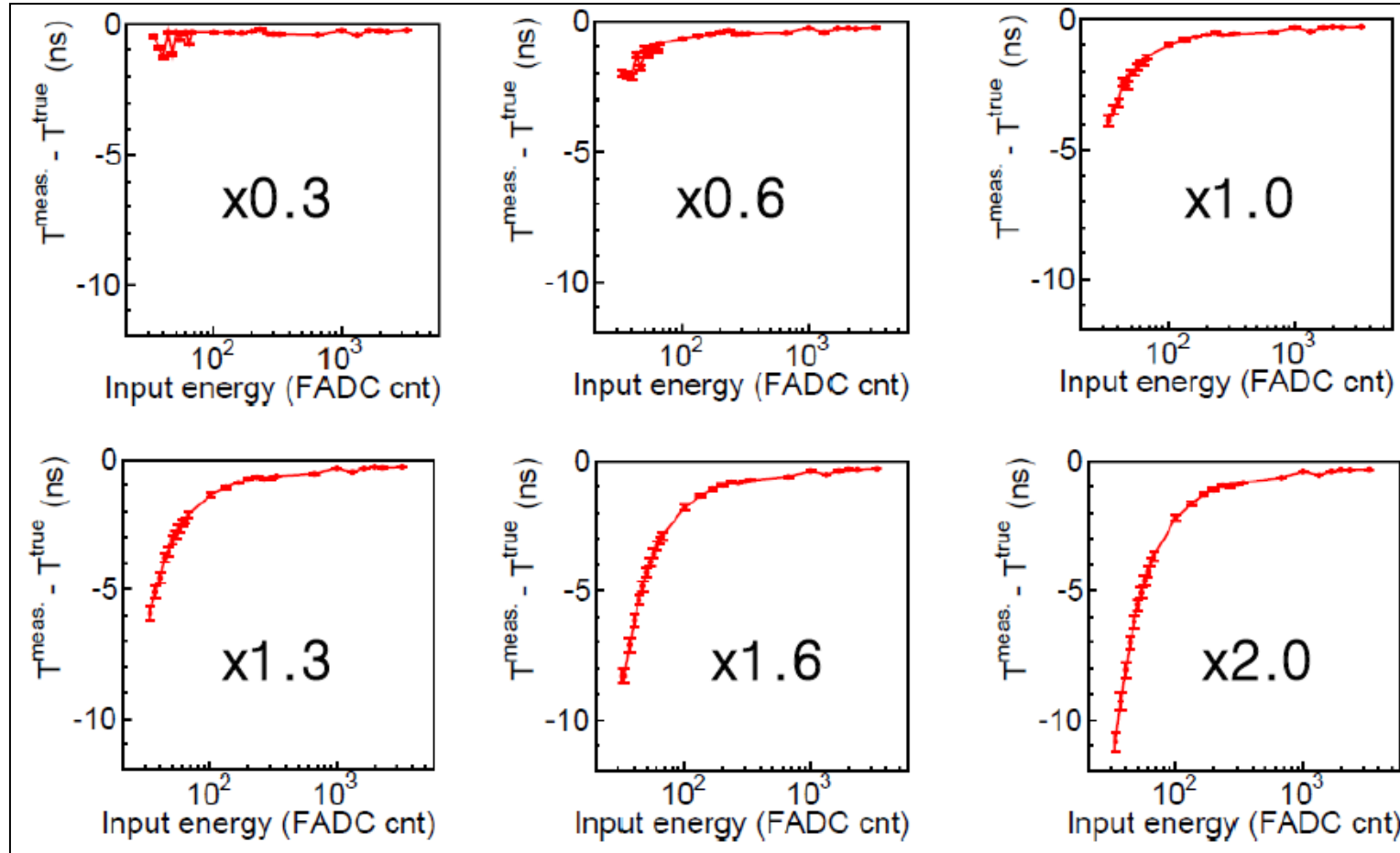
- No update on firmware yet (since priority was low)

Study with offline eventT0

- (Thanks to Ewan and Nils for your supports)
- TC timing and event timing using only exp. 7.
- Use only eventT0 decided by CDC
- Bhabha, hadron, mumu skim
  - No additional cut, except for:
  - TC E^{max}<60ADC~300MeV for mumu skim
- Note that 1 ADC = ~5.25MeV

- After run551 of exp8, 3 problems in FAM fixed
  - Waiting for the cdst…

Study with offline eventT0
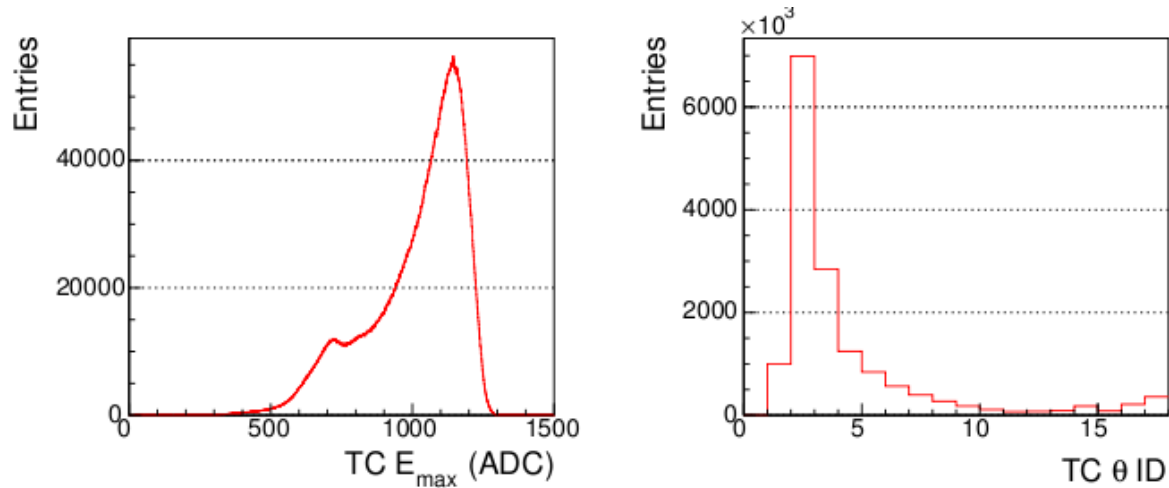
hlt_bhabha
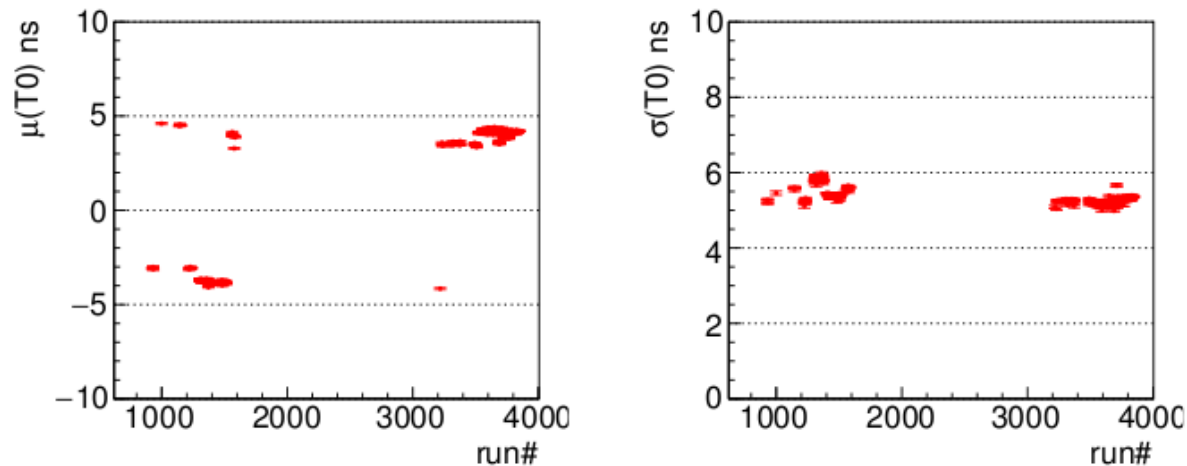
8ns timing shift is cased by GDL+FTSW (probably)

Study with offline eventT0

Study with offline eventT0

<60ADC
~300MeV

TC E$_{max}$ (ADC)

TC θ ID

hlt_mumu_2trk

μ(T0) ns

σ(T0) ns

run#

run#
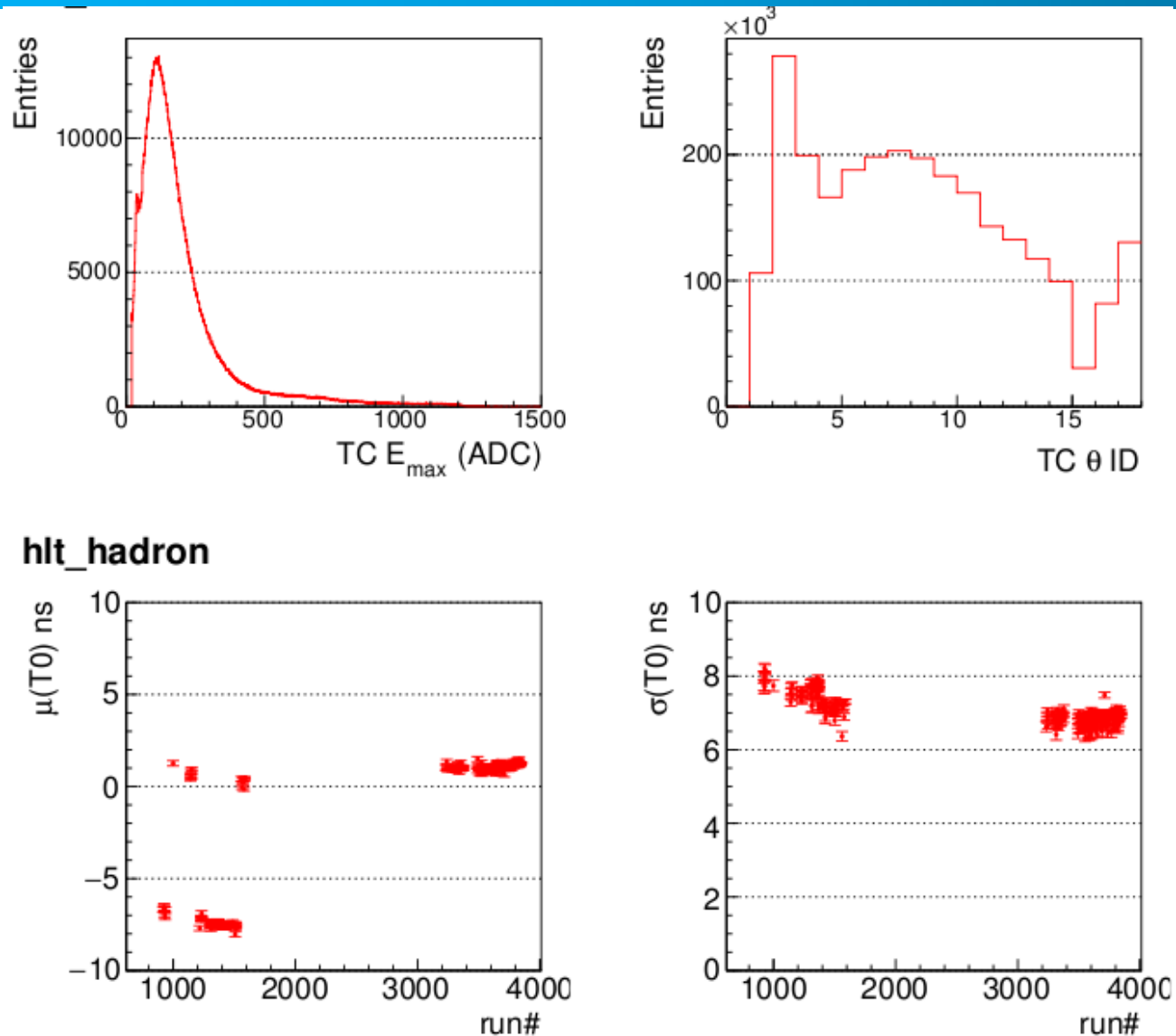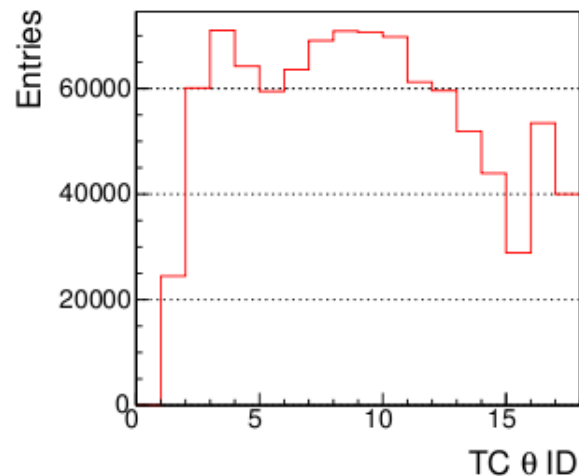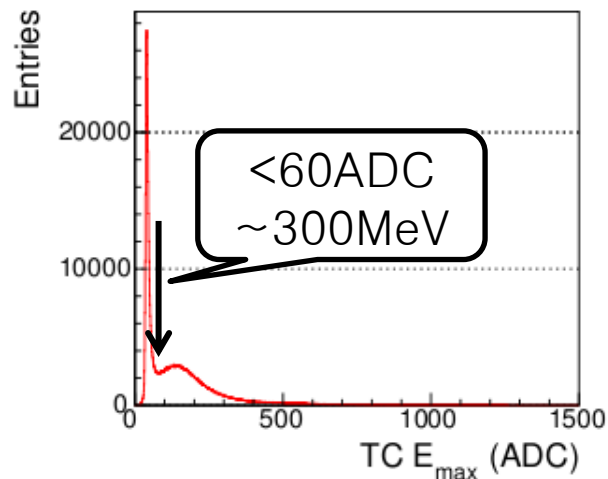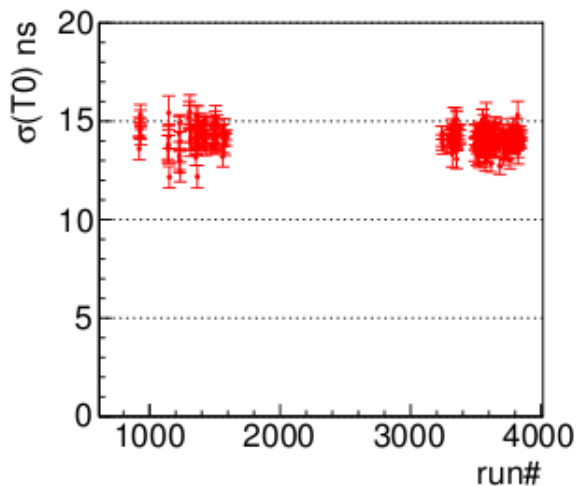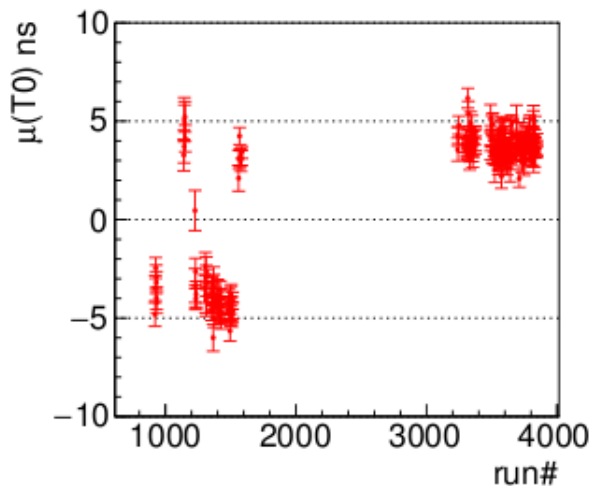
Why peak position is different from that of hadron skim ?

Study with offline eventT0
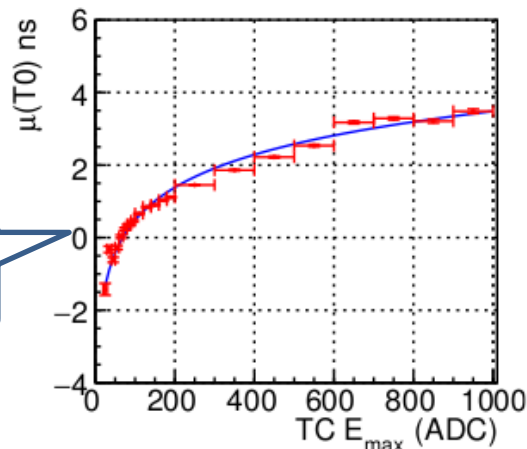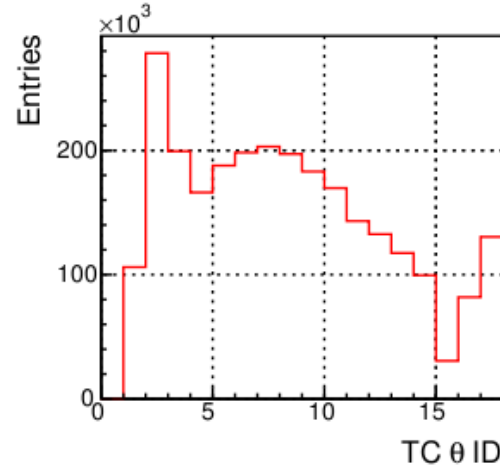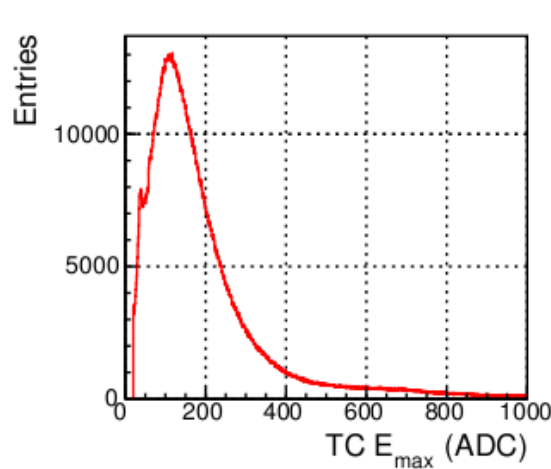
Probably, shown by Torben at last b2gm already
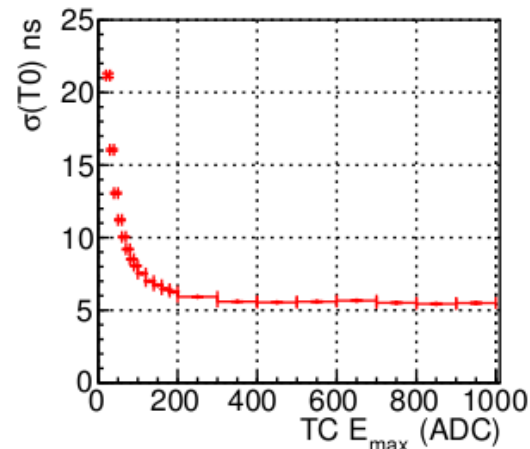
- Plan to update FAM firmware to apply timing correction by LUT.
- First, revisit simulator to find correlation between bias and noise level.

Large TC timing resolution

- Simulation shows TC timing resolution is around **1ns** for Bhabha sample
- Off line eventT0 shows around 5ns. Why ?

eventT0 for Bhabha skim when TC126 is most energetic in an event
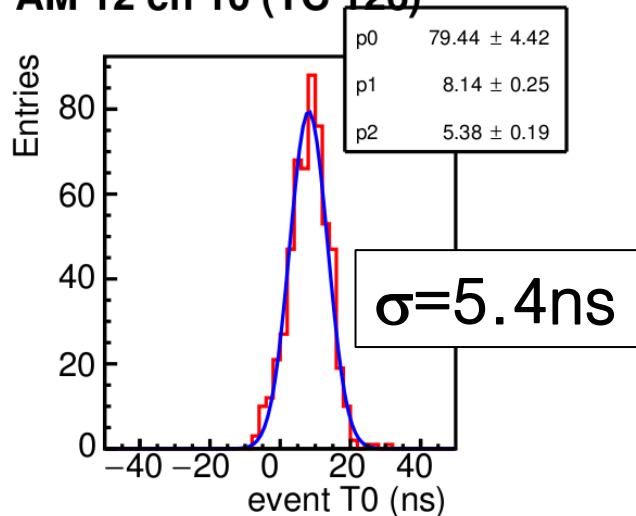
Single ch test pulse run ch1 to 16
Diff = T(chX) − T(ch1)

FAM 12 ch 10 (TC 126)

p0	79.44 ± 4.42
p1	8.14 ± 0.25
p2	5.38 ± 0.19

σ=5.4ns

FAM12 ch10
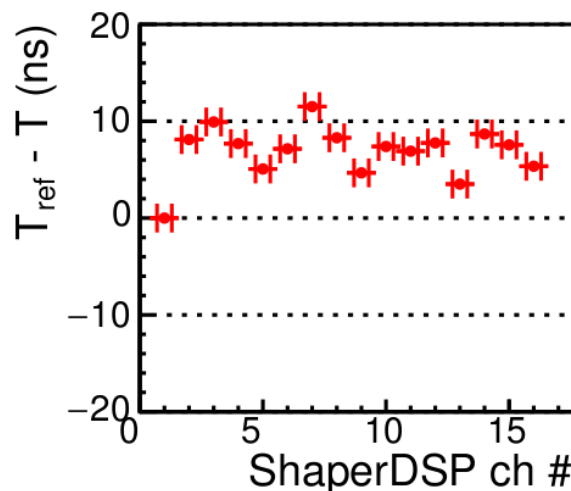
- Timing differences btw 16ch in one TC are not negligible
- Plan to check timing variation using beam data, and
- Plan to compare timing differences with ECL time calibration constants
- Anyway, no way to avoid in trigger level.
- Need to update tsim-ecl to take into account this effect⋯

Large TC timing resolution